

FIG. 1

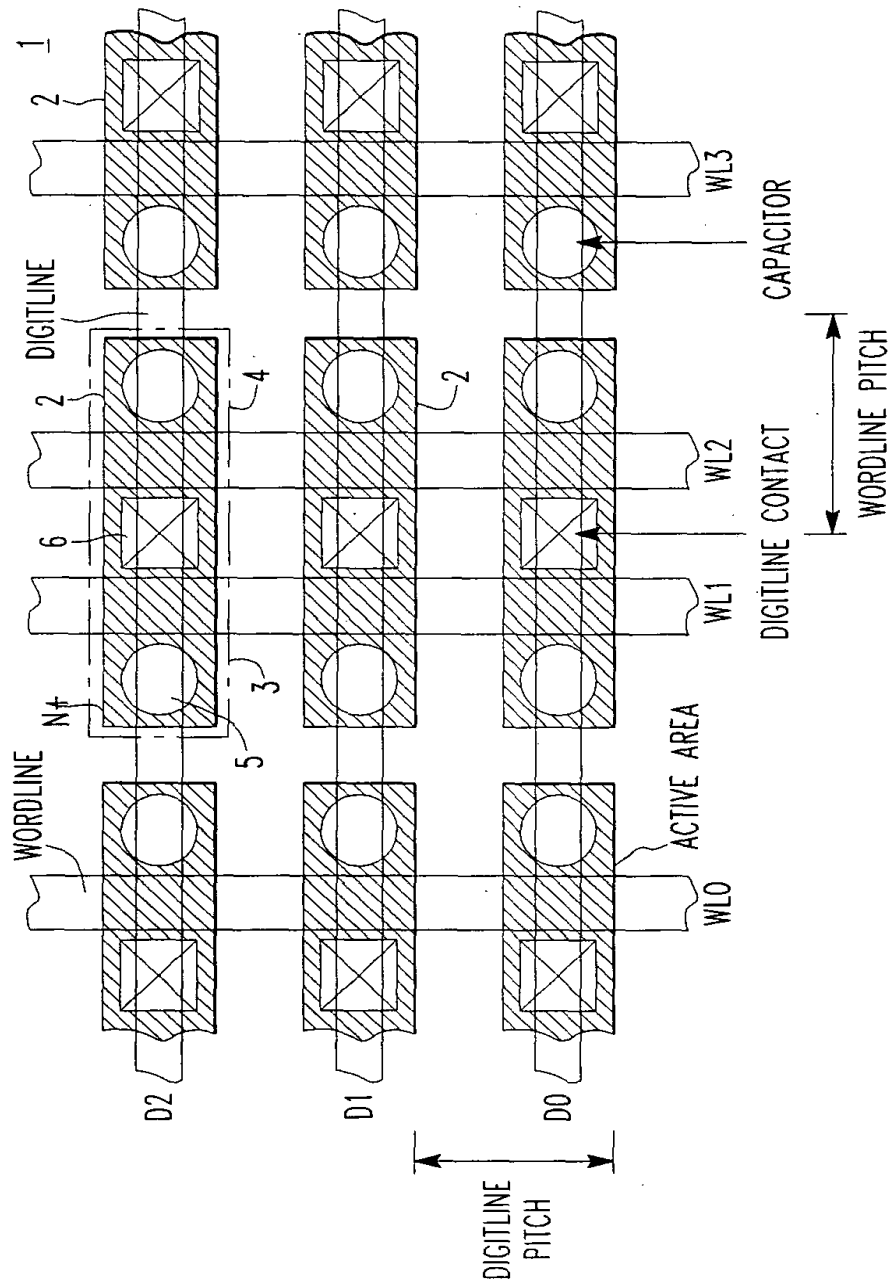


FIG. 1

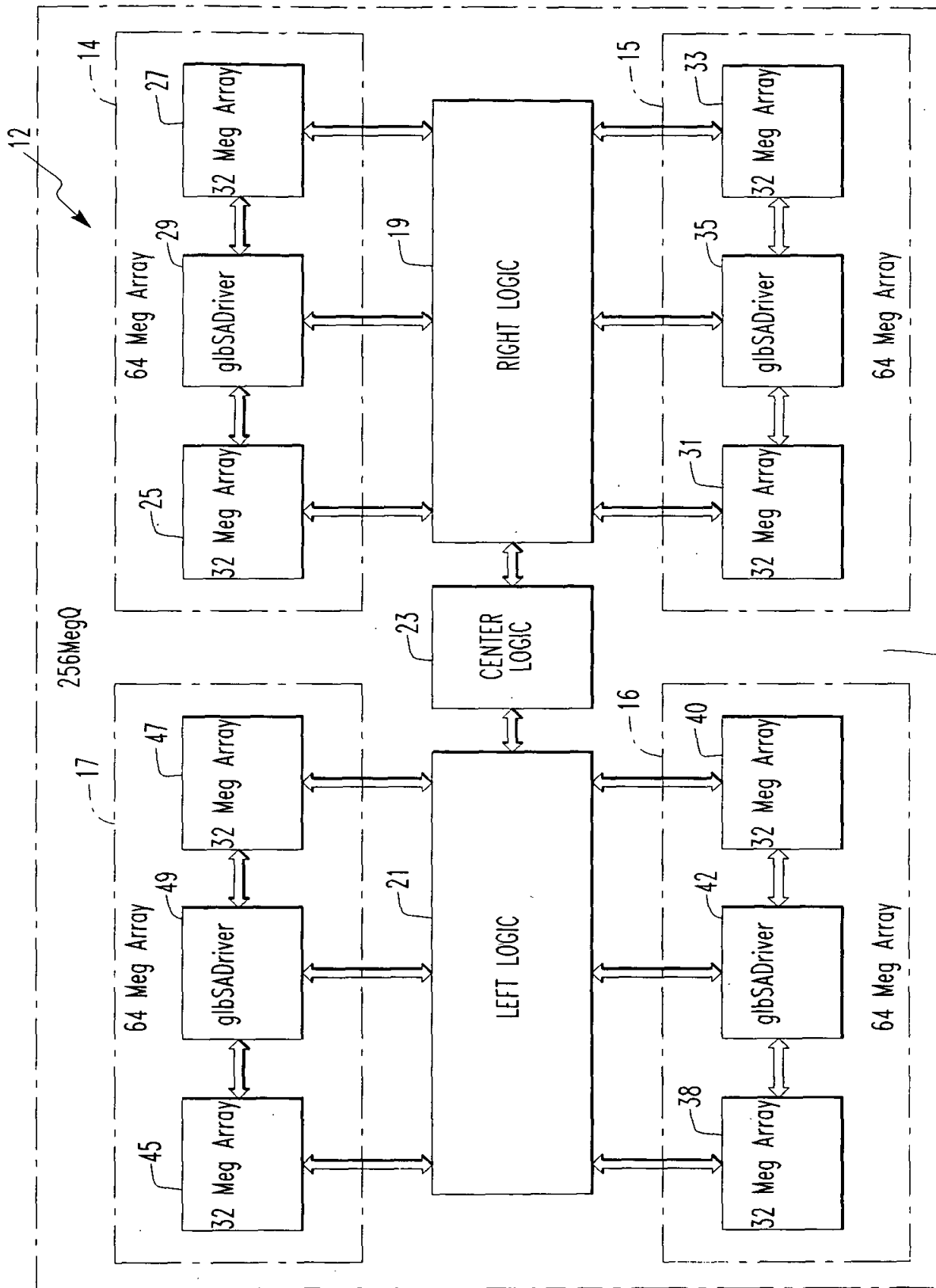


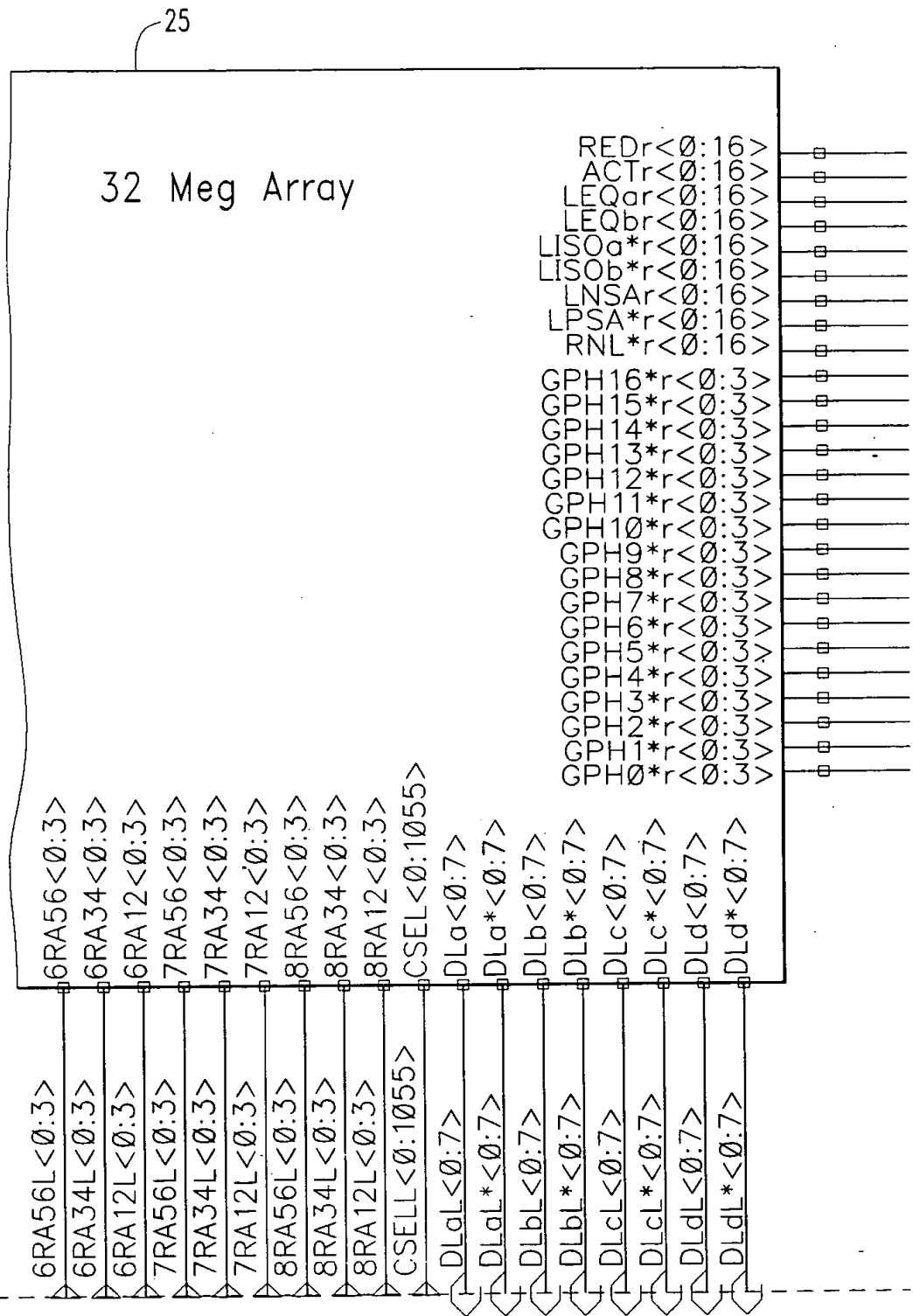
FIG. 2

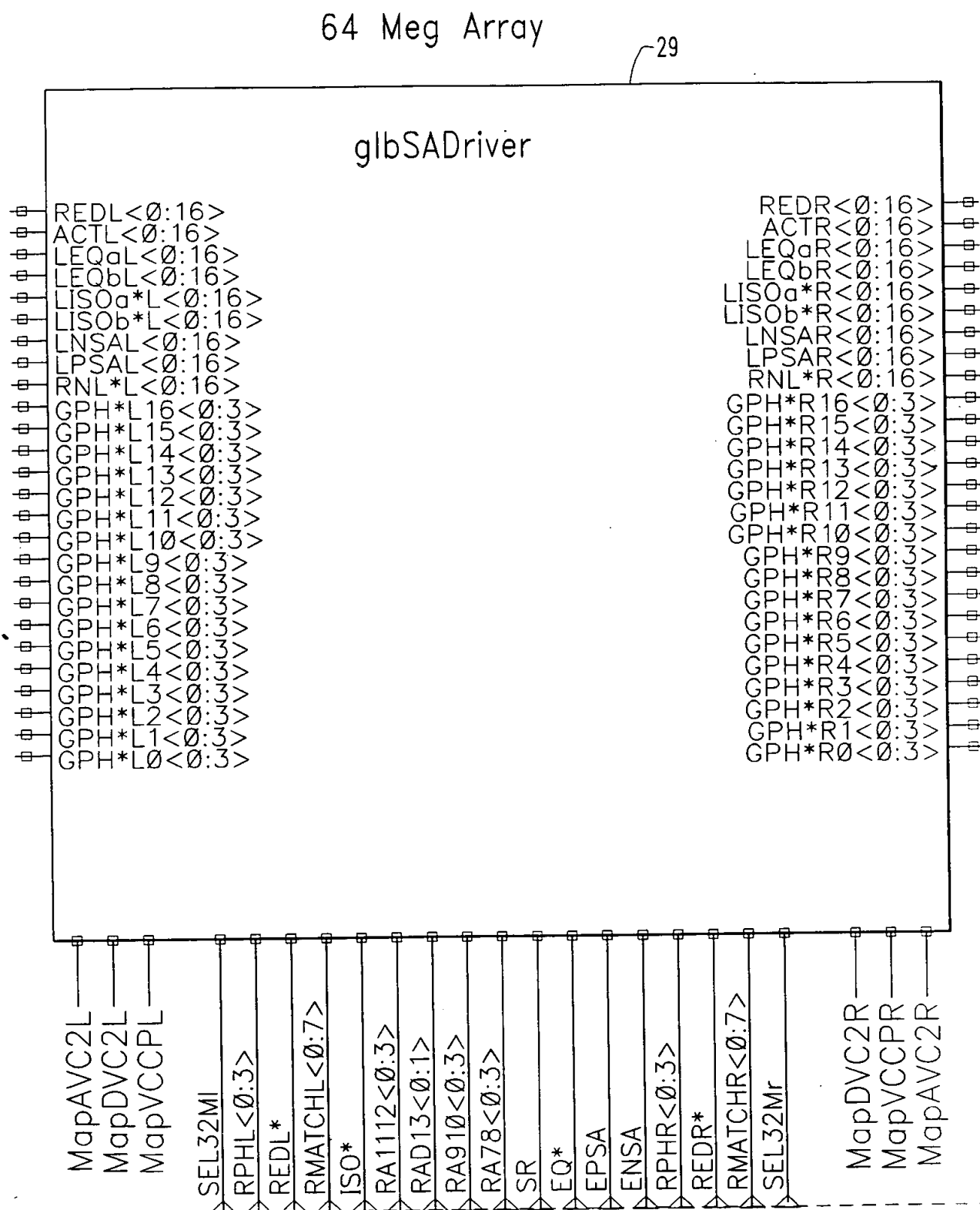
Figure 1 is a block diagram of a 32 Meg Array. The array is a large rectangular block with various inputs and outputs. The inputs are labeled as follows: MapVCCA, VCCA, MapVCCPL, MapDVC2L, MapAVC2L, and SEL32M* (n). The outputs are labeled as follows: SEL32ML* and SEL32M* (n). The array is divided into four sections: 0RA56<0:3>, 0RA34<0:3>, 0RA12<0:3>, and 1RA56<0:3>. The array is also labeled 32 Meg Array.

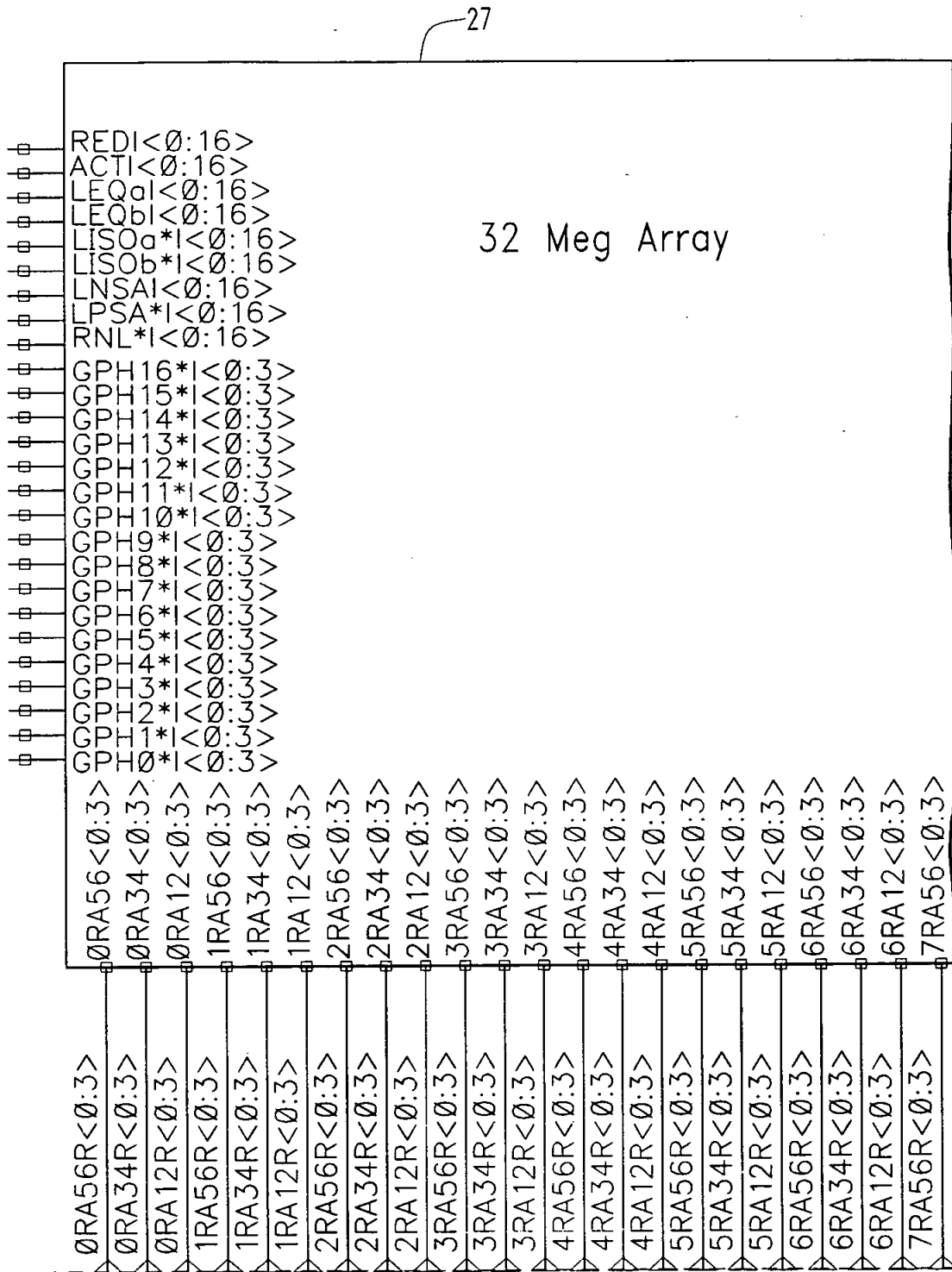
FIG. 3B

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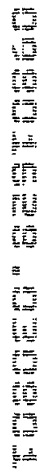
FIG. 3B is a block diagram of a 32 Meg Array.







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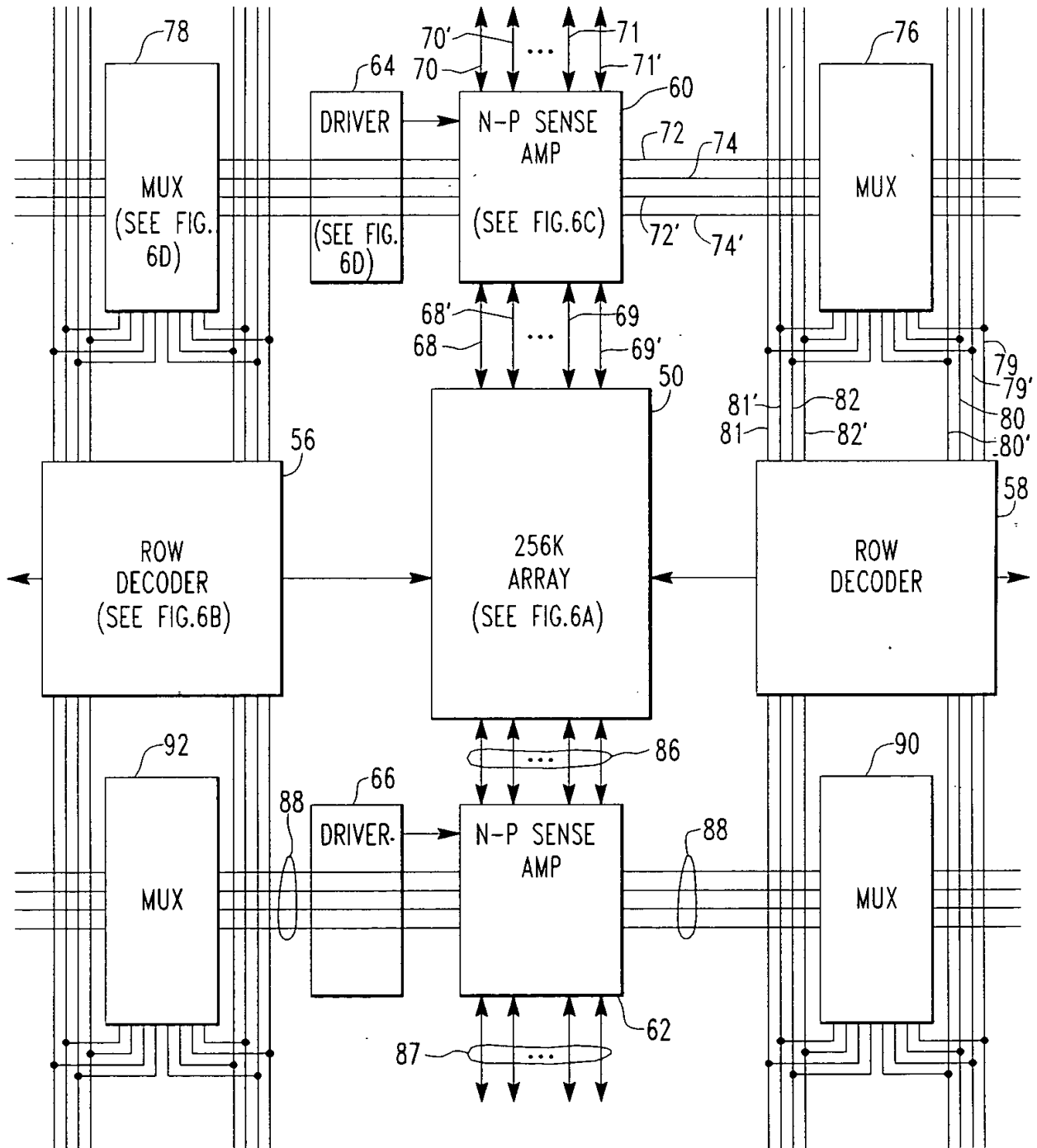


FIG. 5

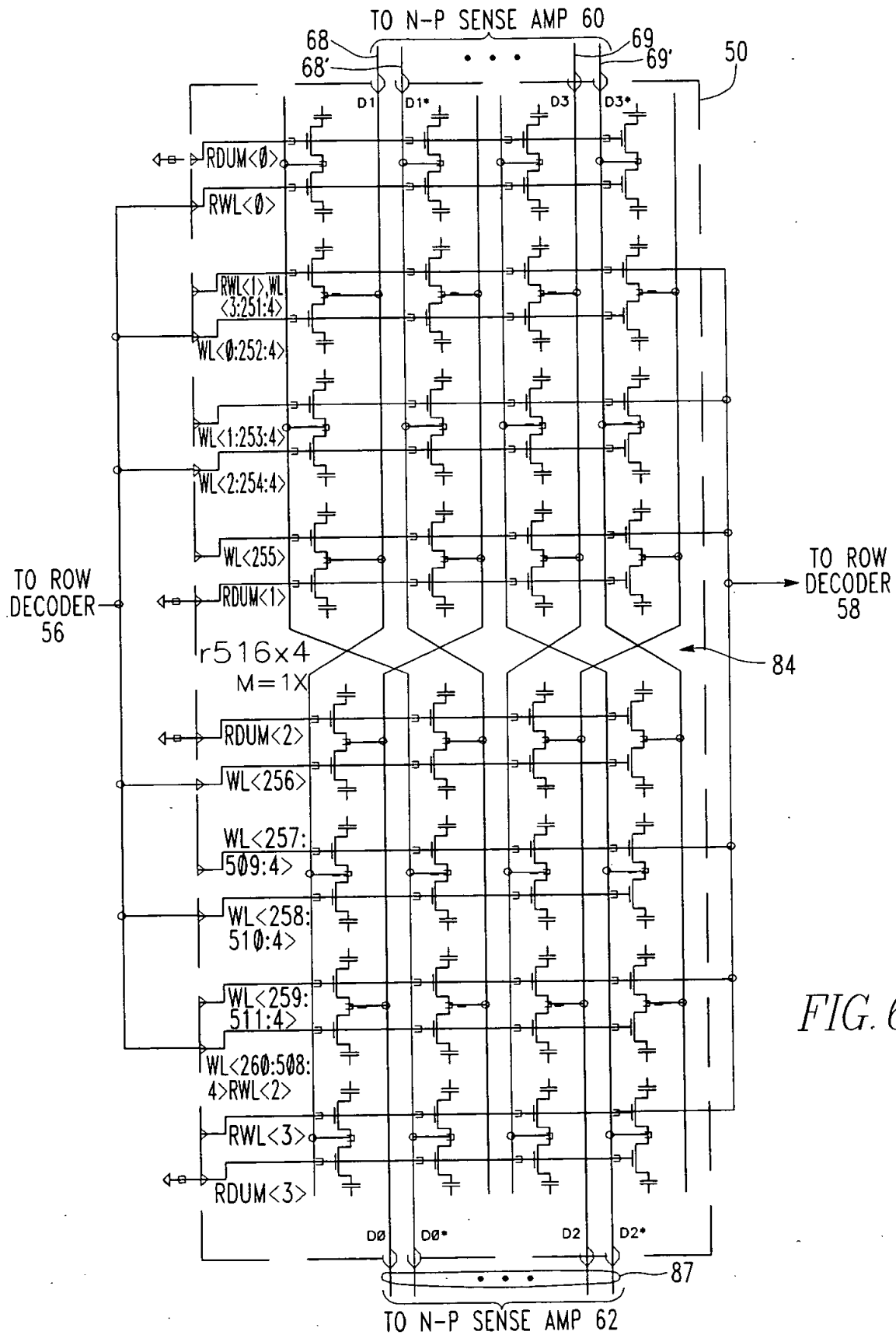
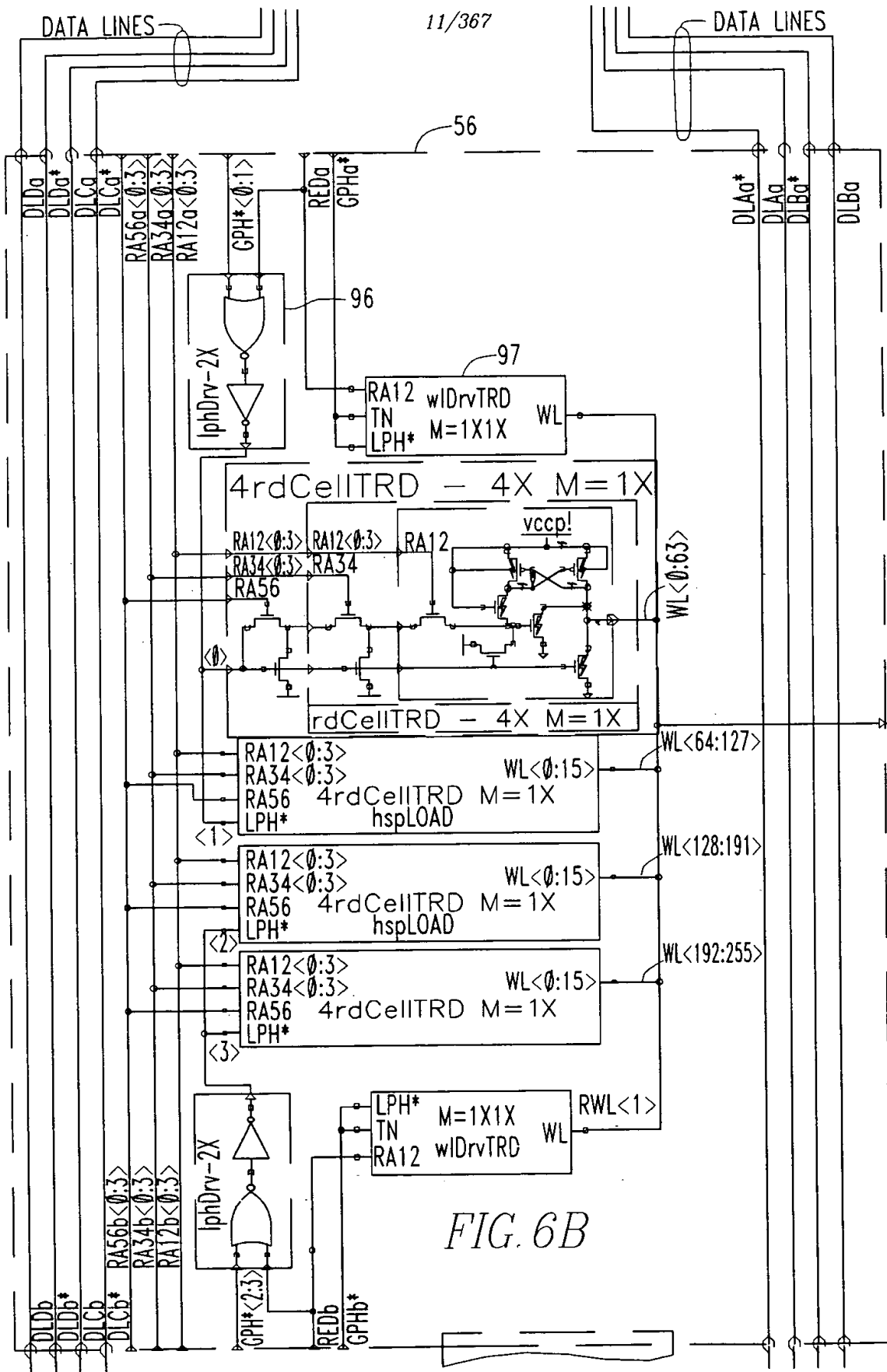


FIG. 6A



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Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:

CA01* D1(even) D2(odd)

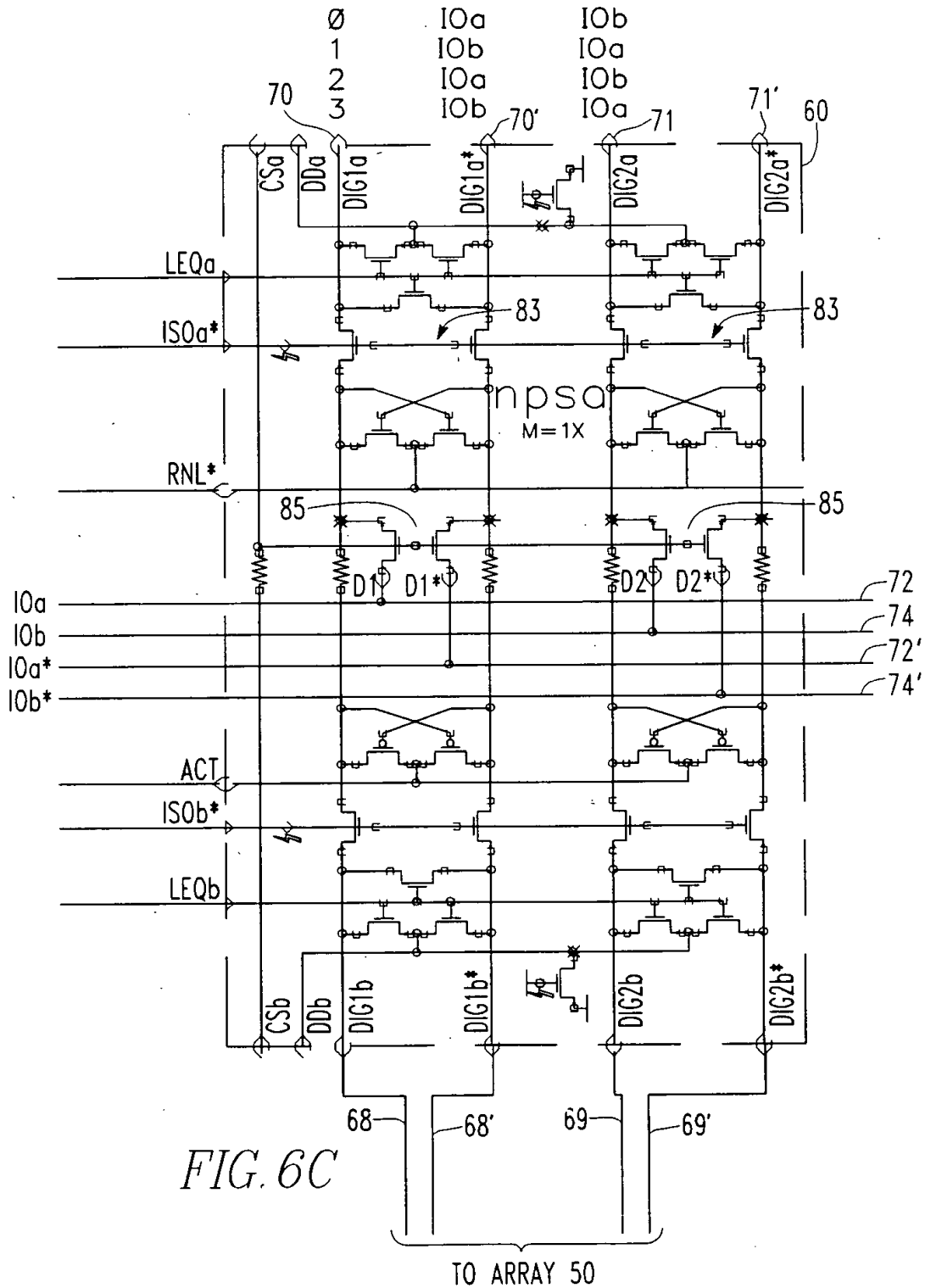


FIG. 6C

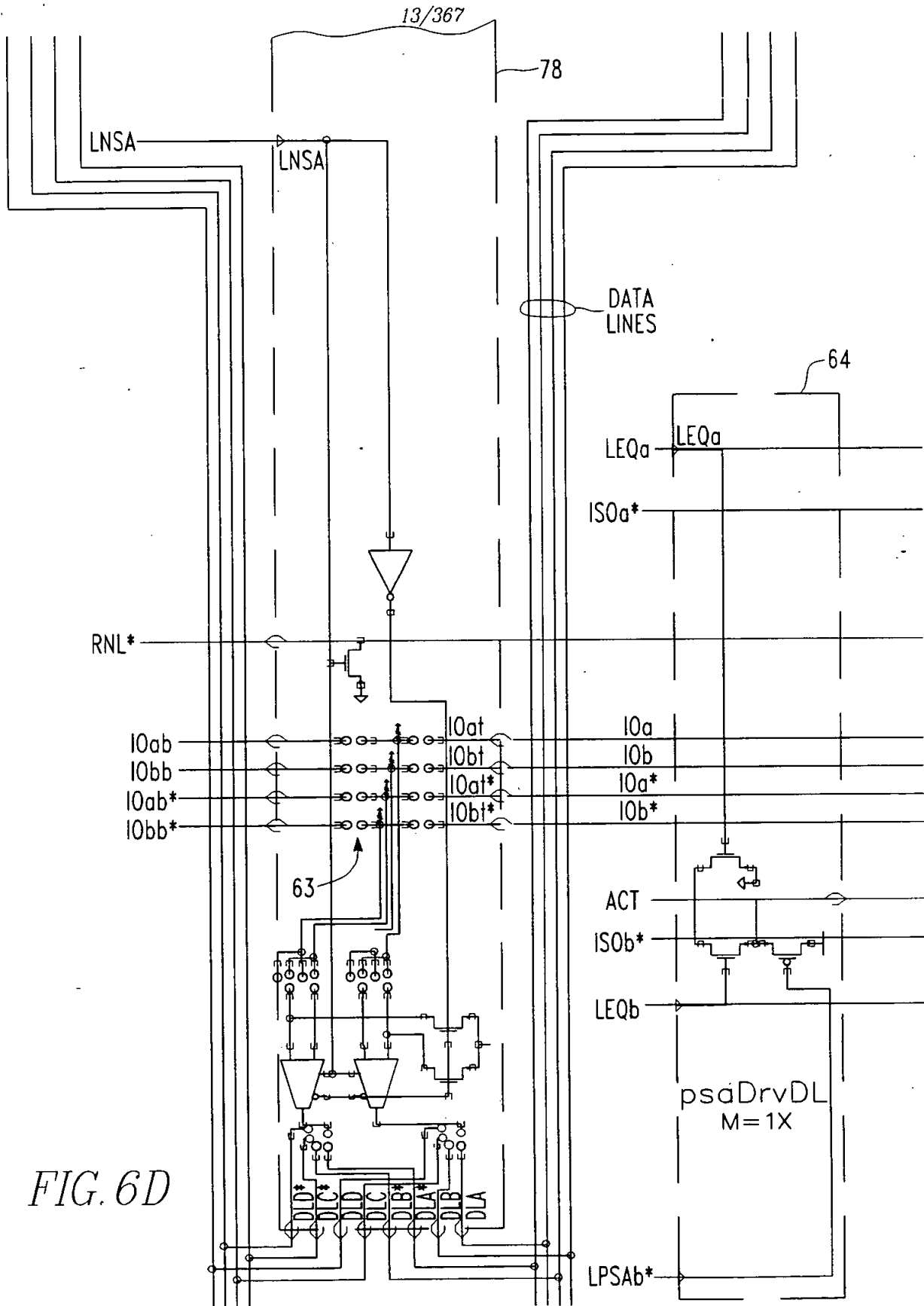
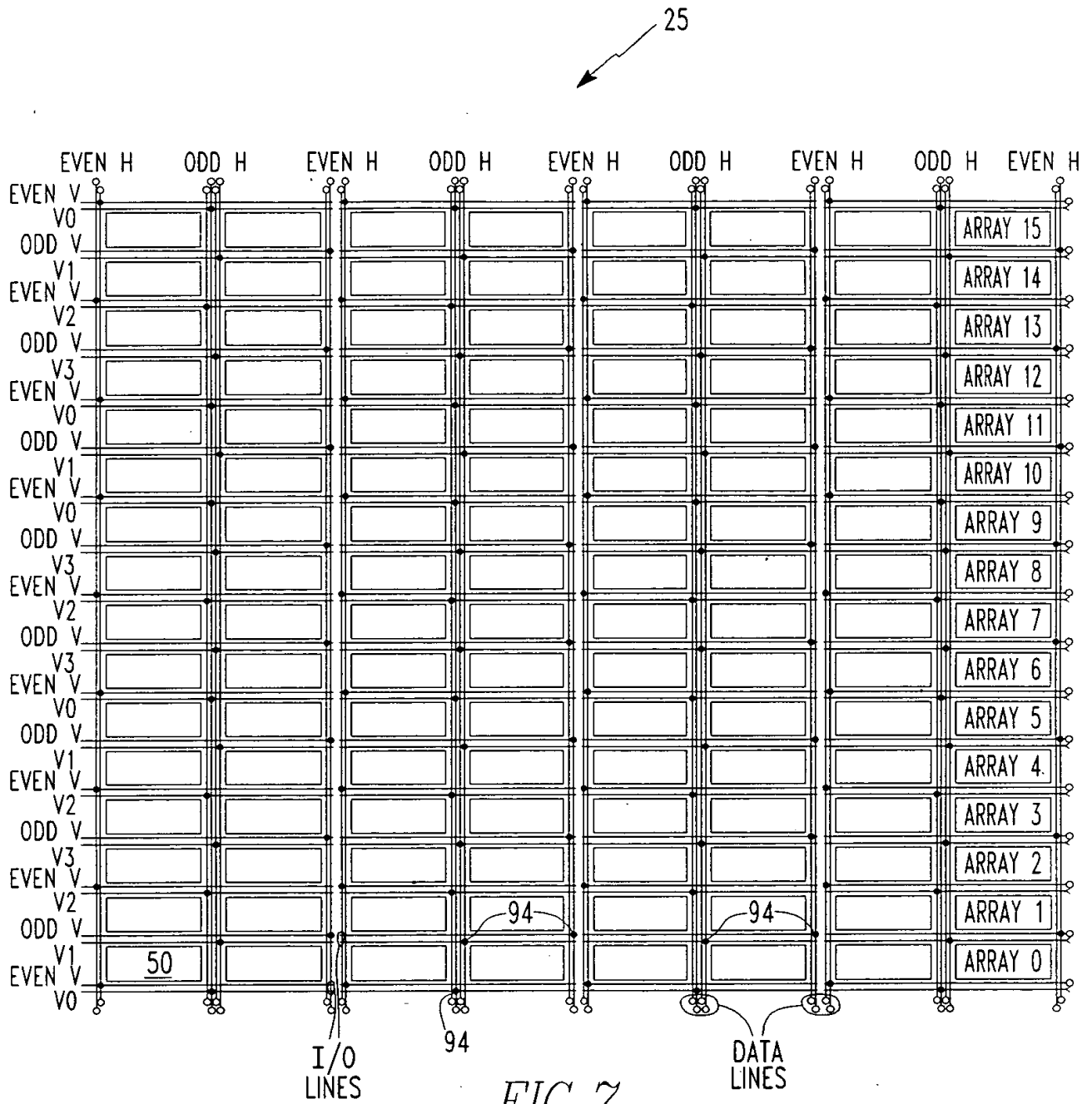


FIG. 6D



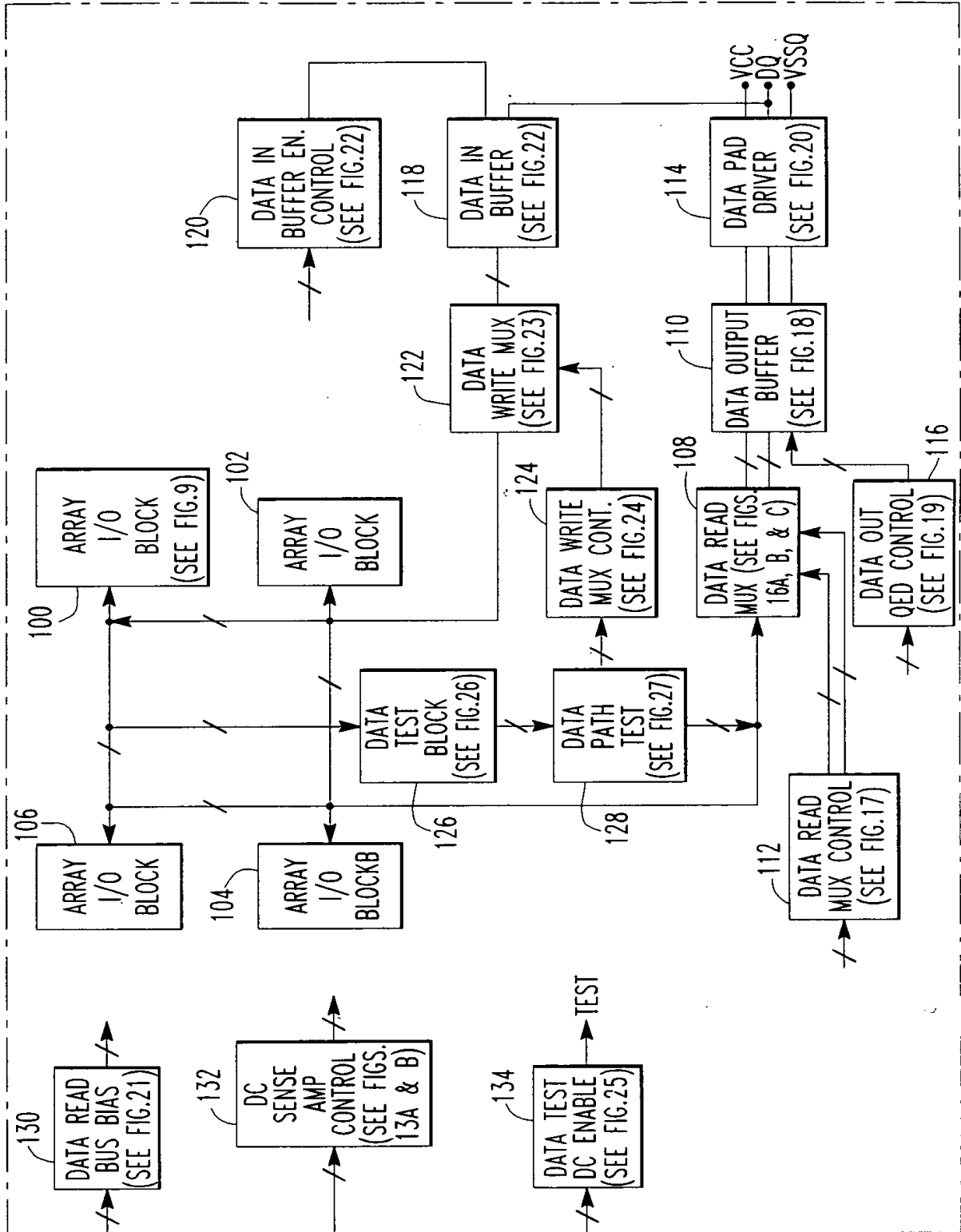


FIG. 8

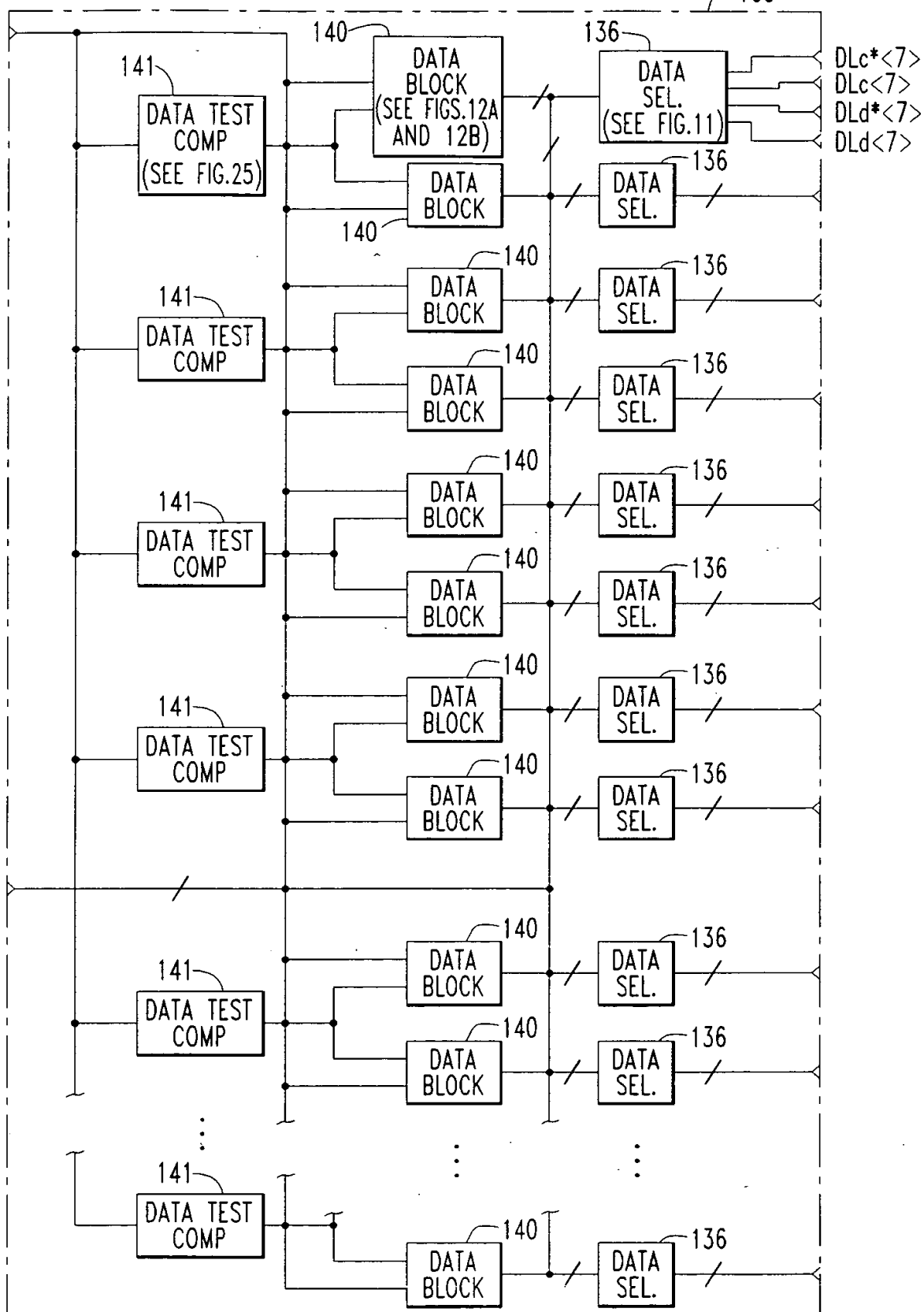


FIG. 9

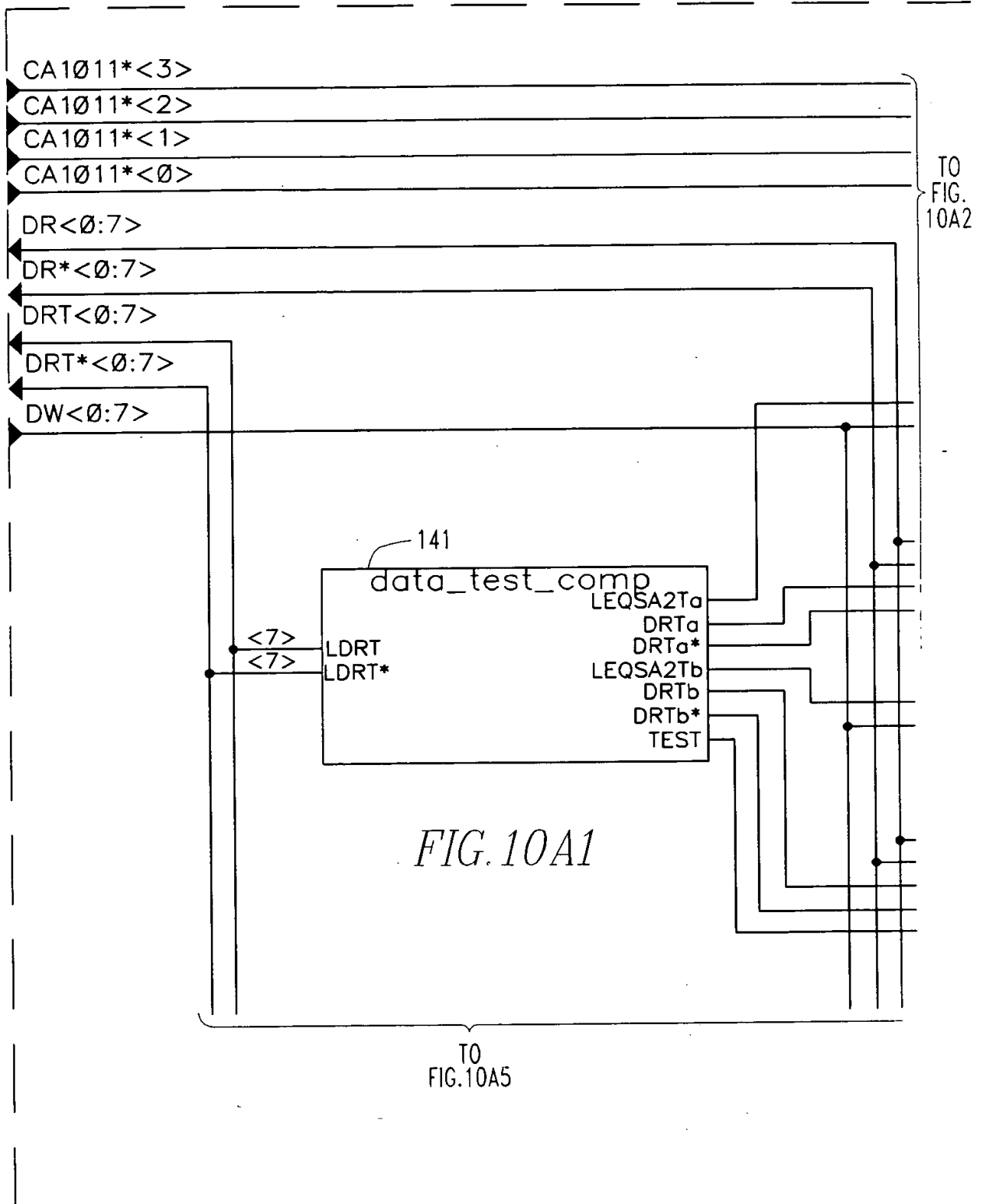


FIG. 10A2

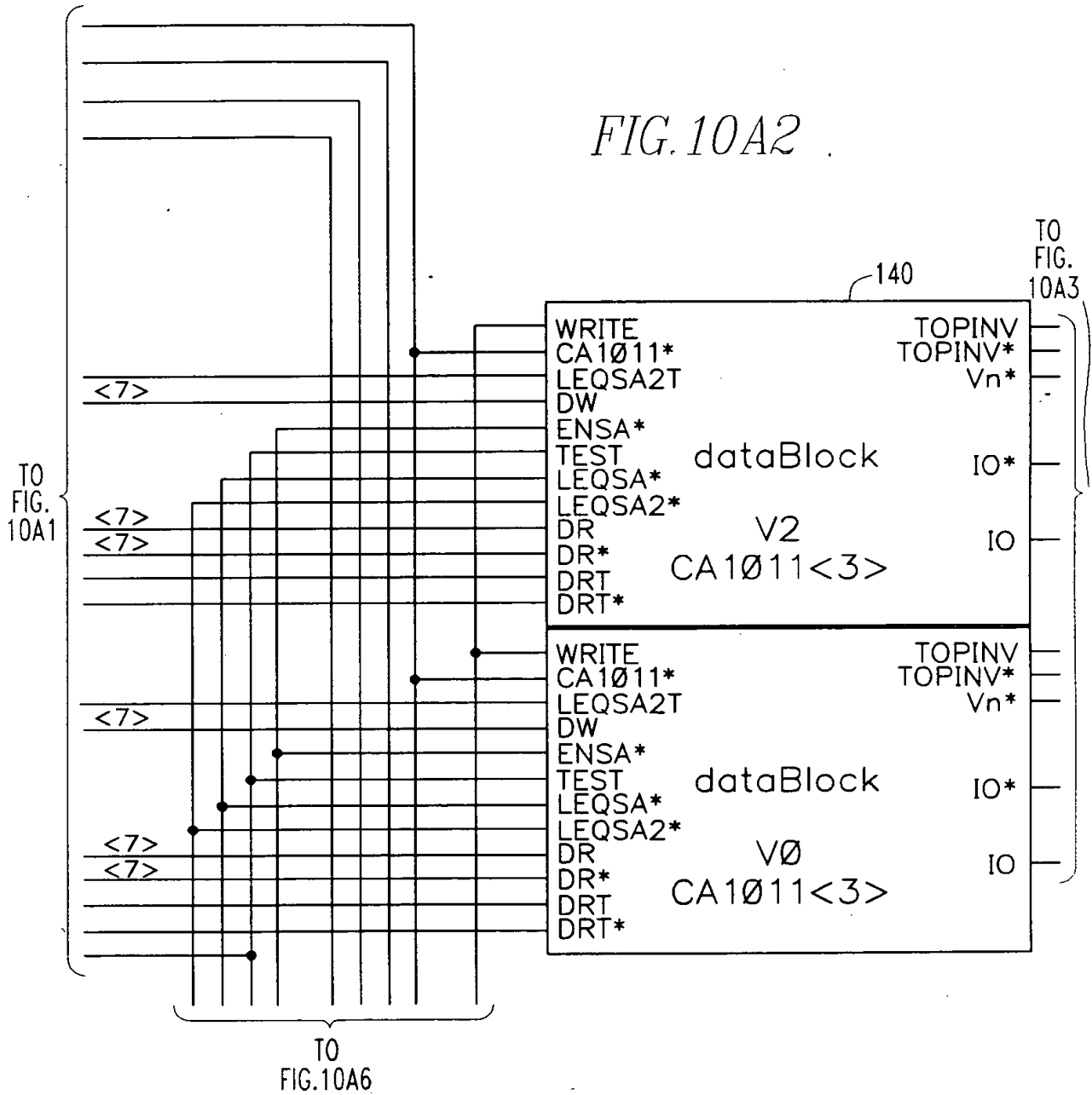
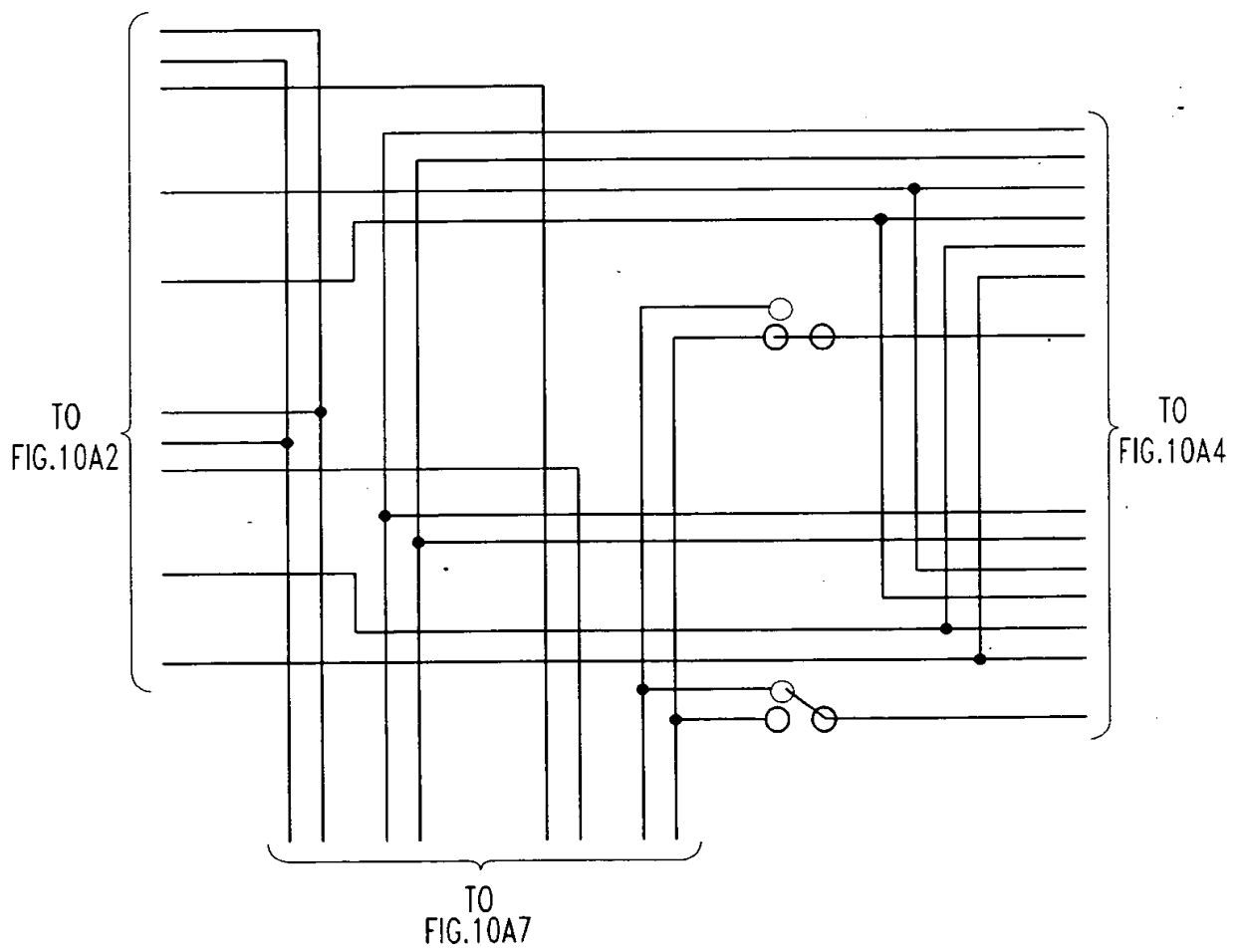


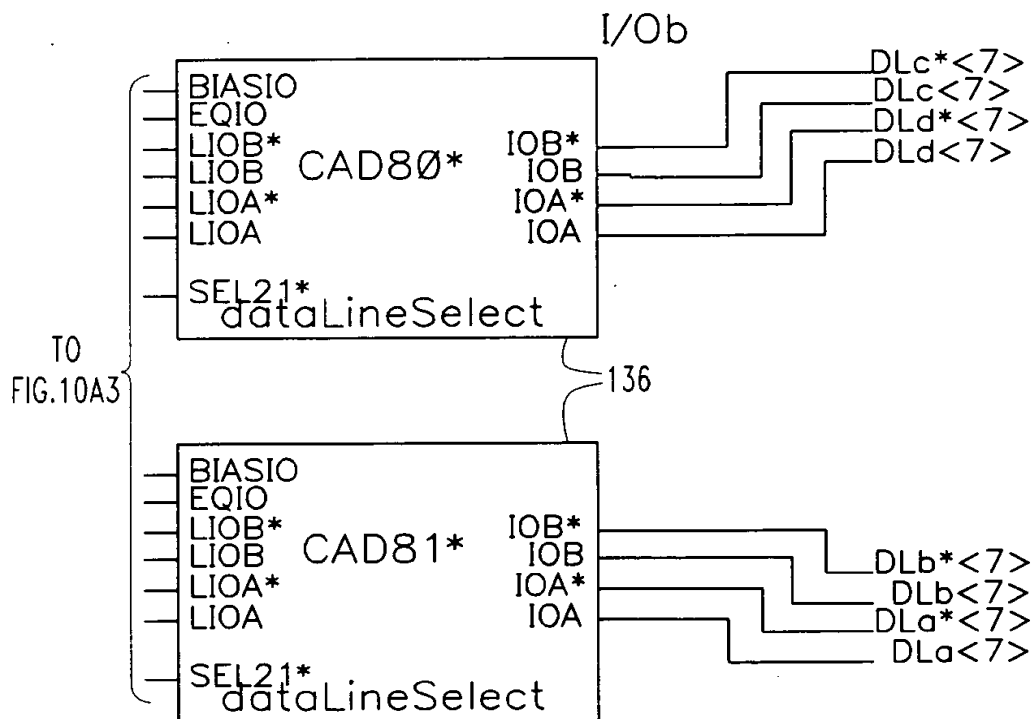
FIG. 10A3

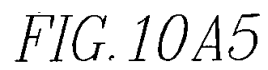


arrayIOBlock

100

FIG. 10A4





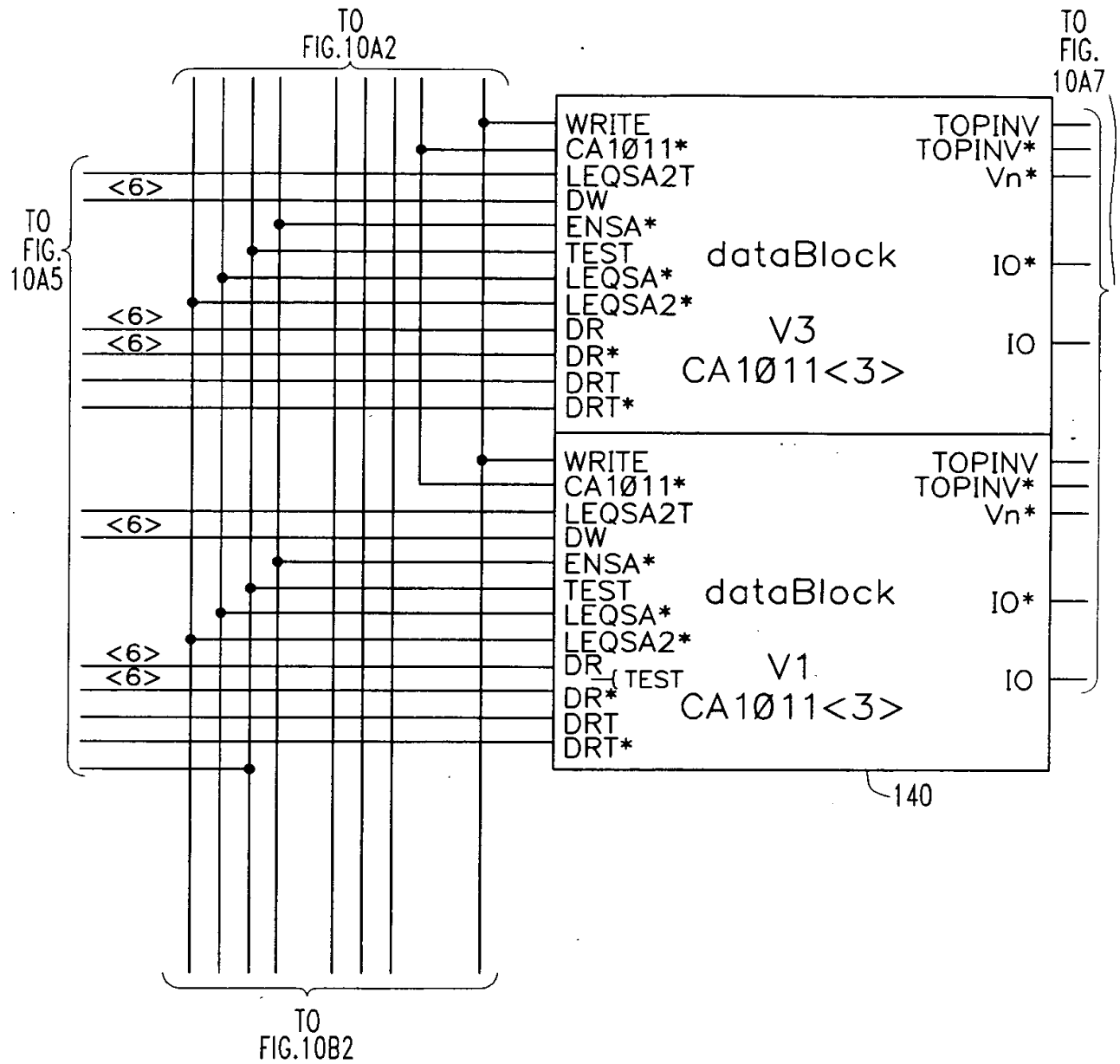


FIG. 10A6

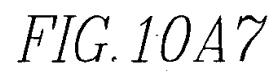


FIG. 10A7

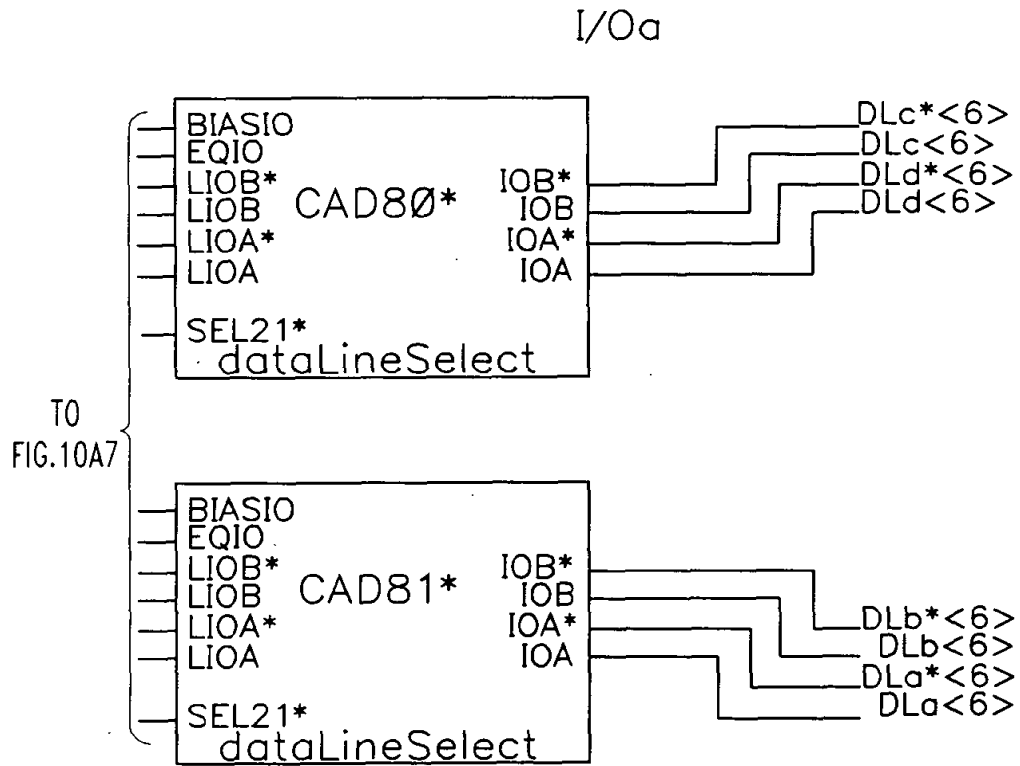


FIG.10A8

FIG. 10B1

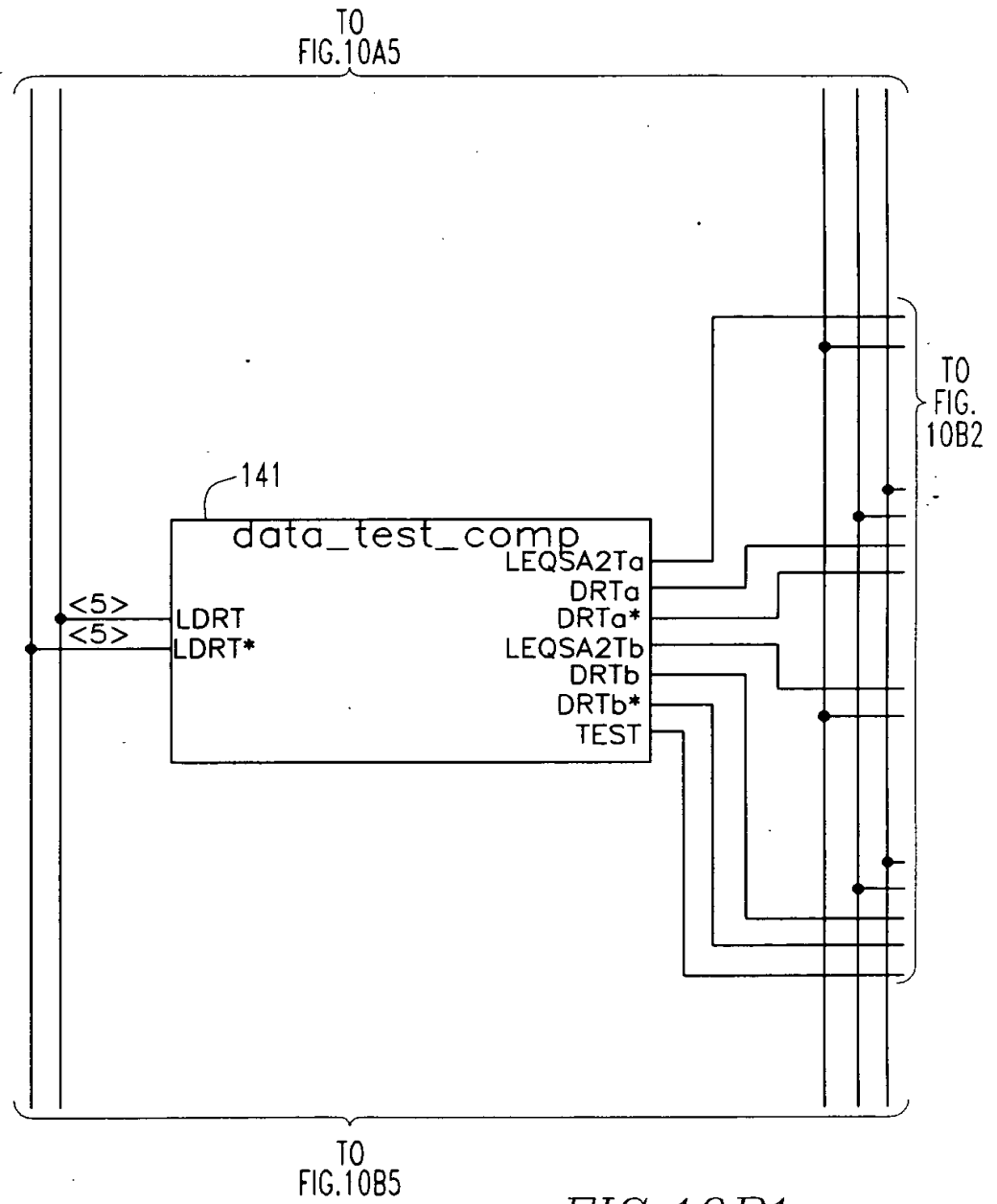


FIG. 10B1

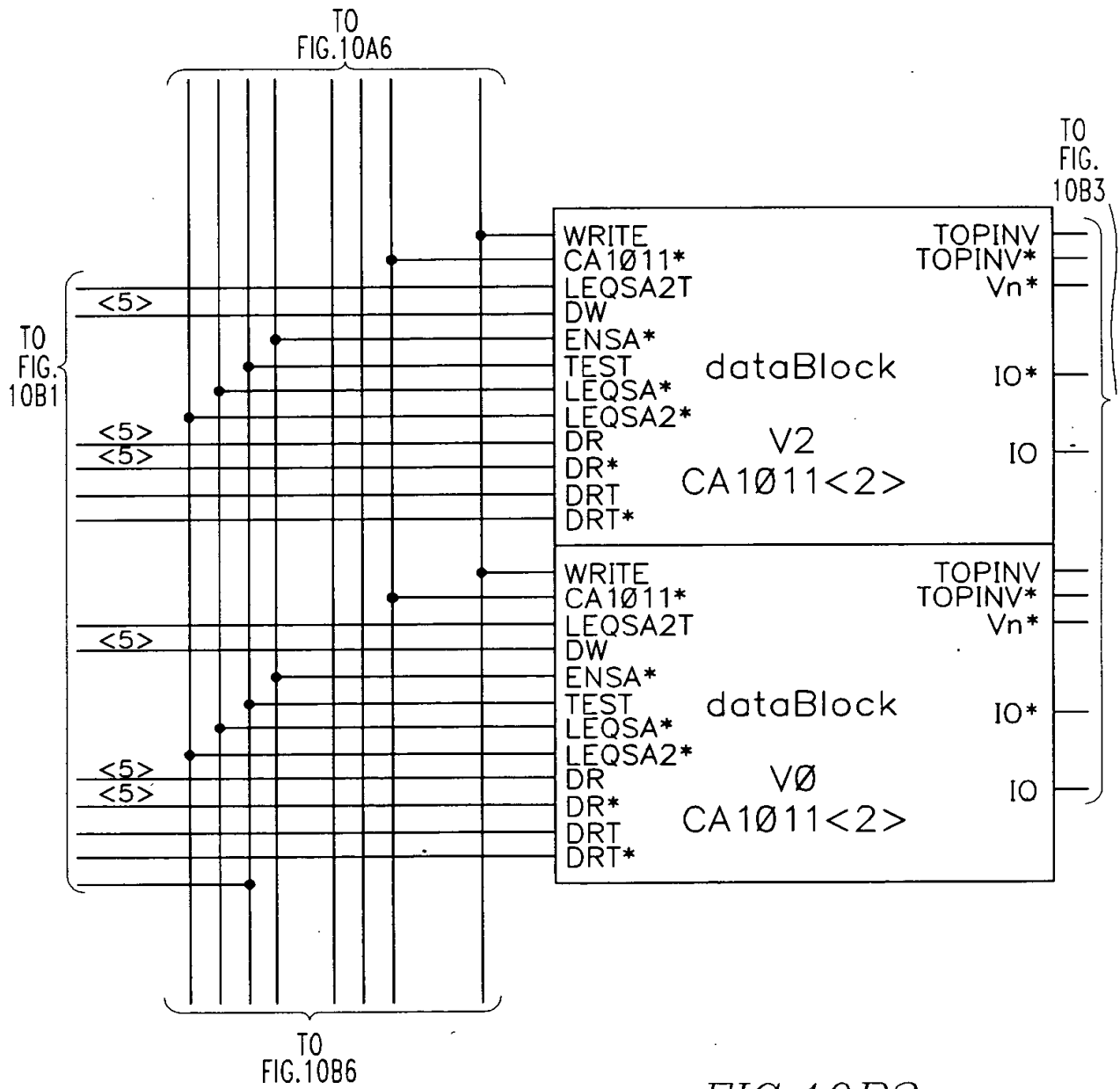


FIG. 10B2

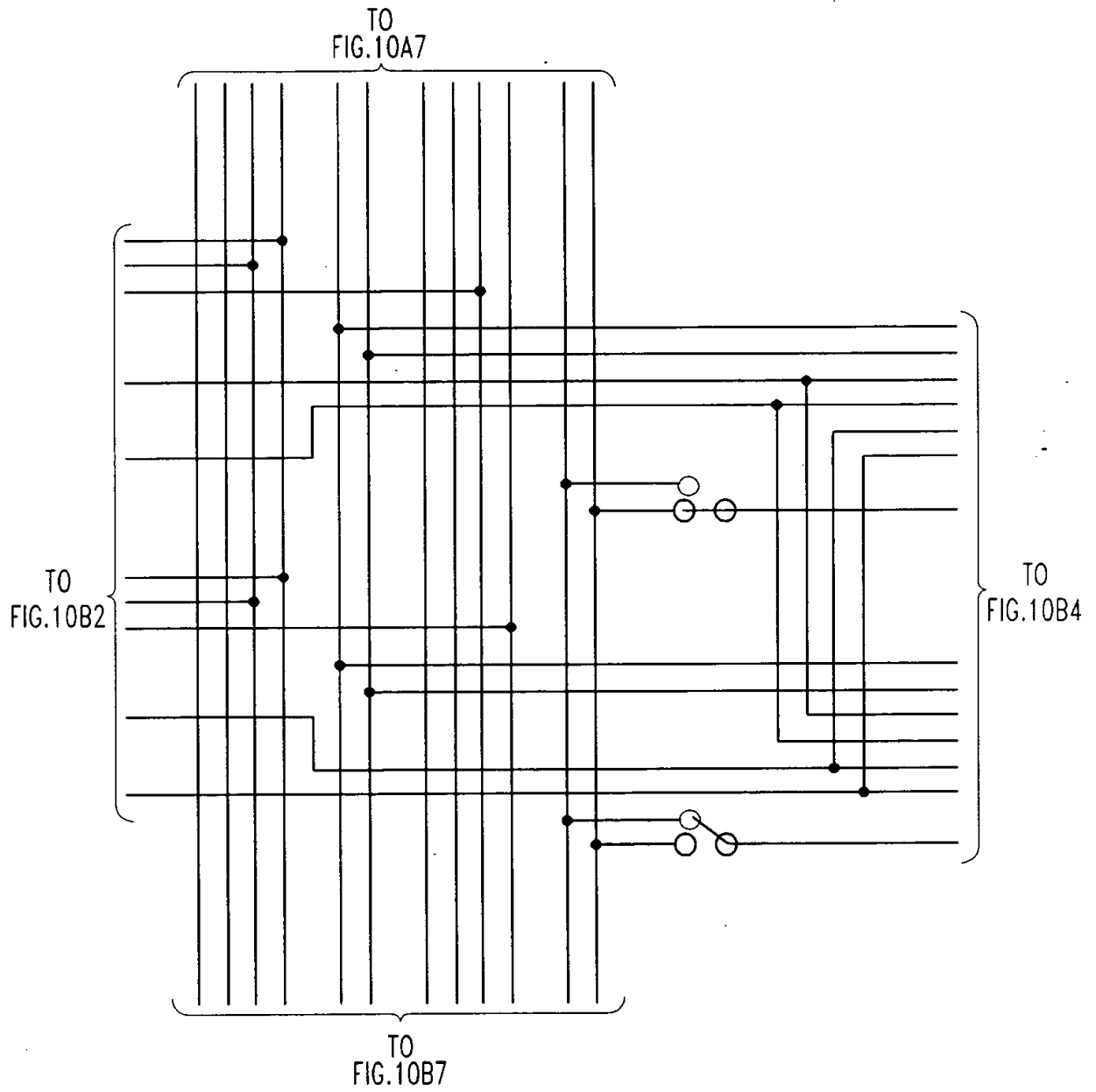


FIG. 10B3

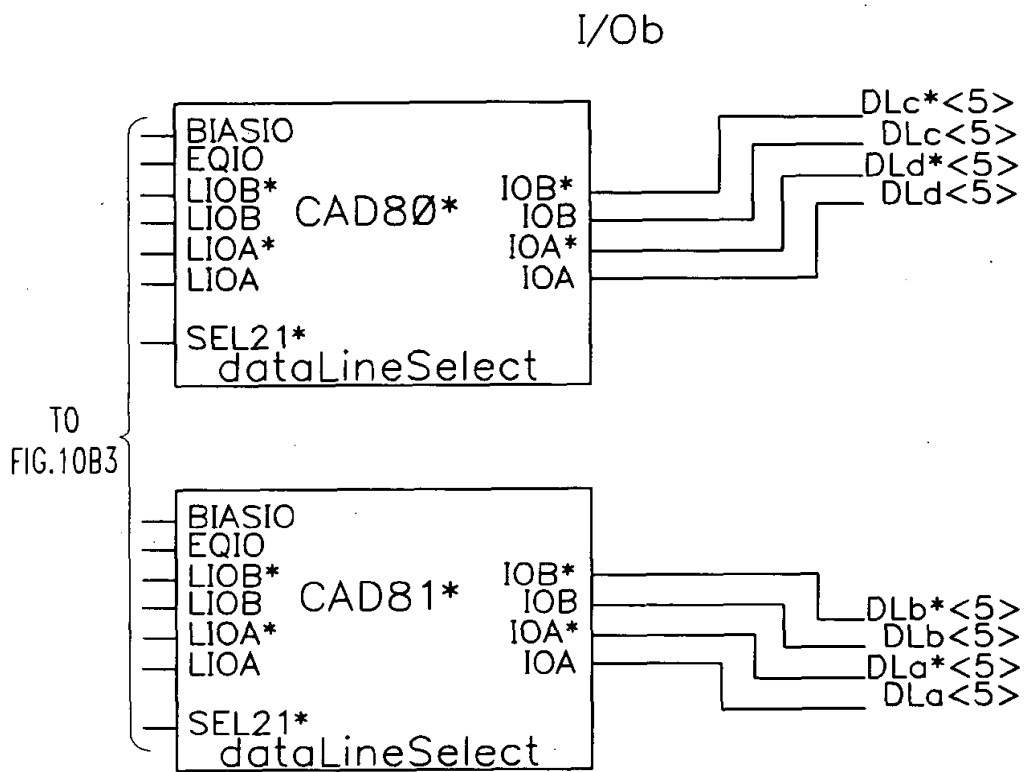


FIG.10B4

FIG. 10B5

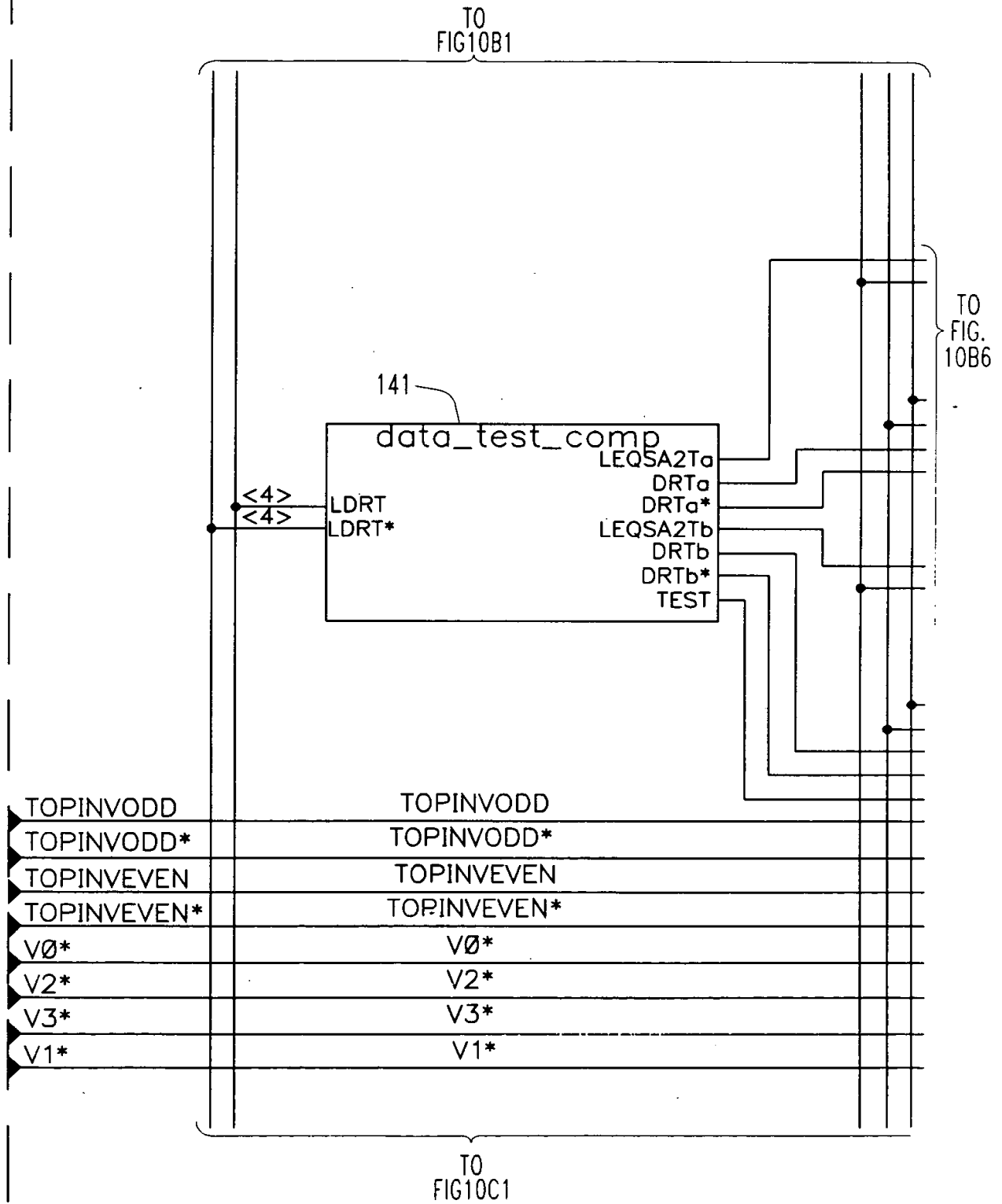


FIG. 10B6

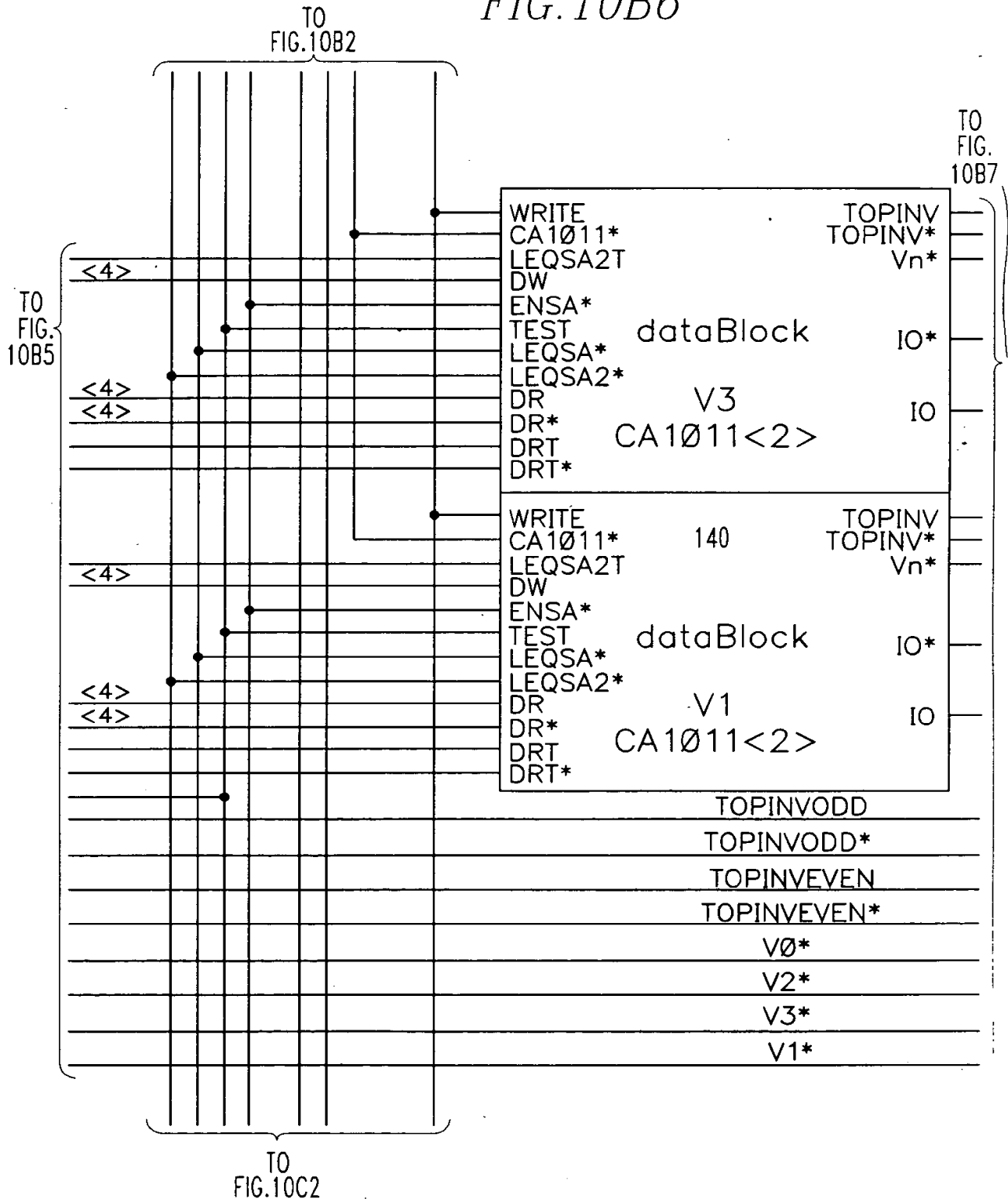


FIG. 10B7

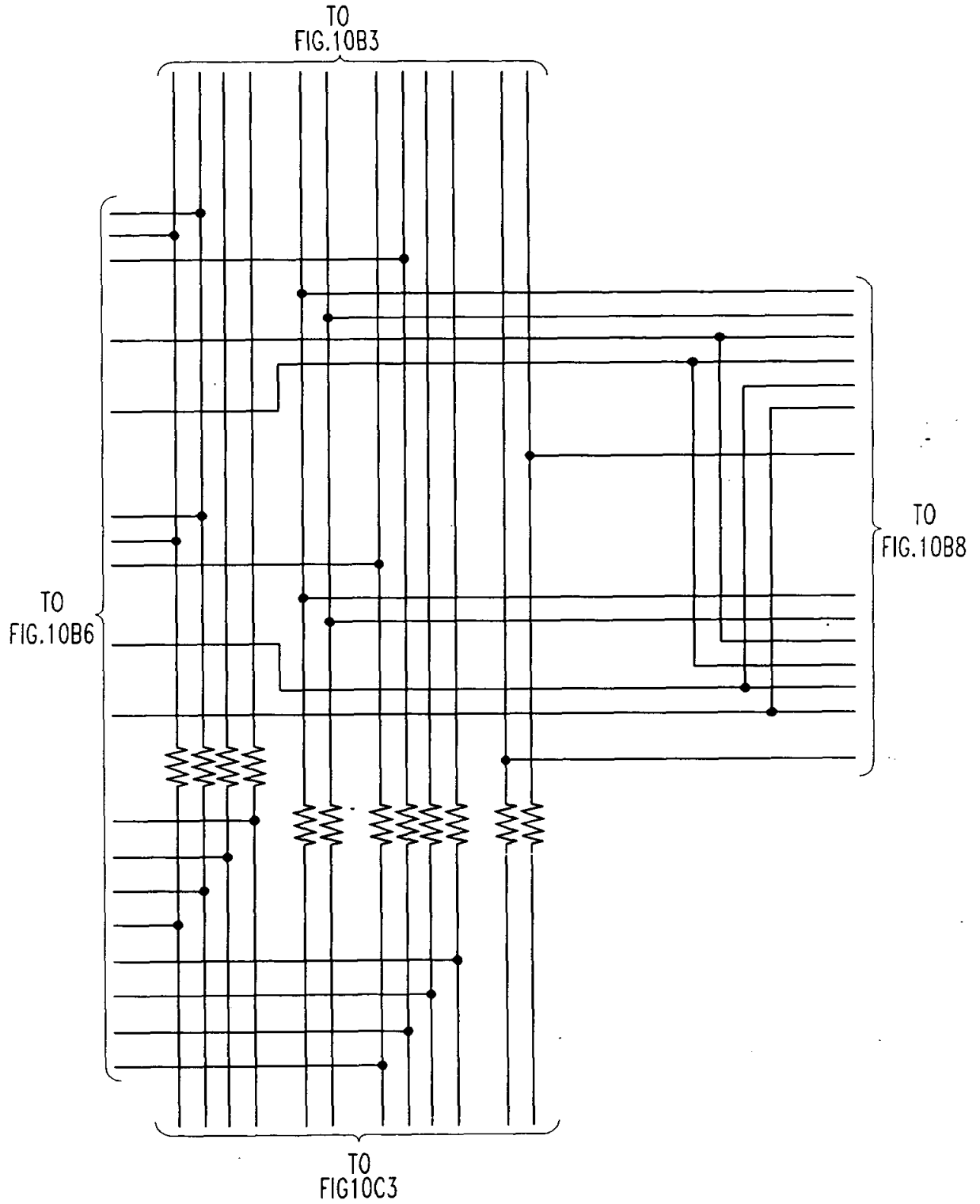
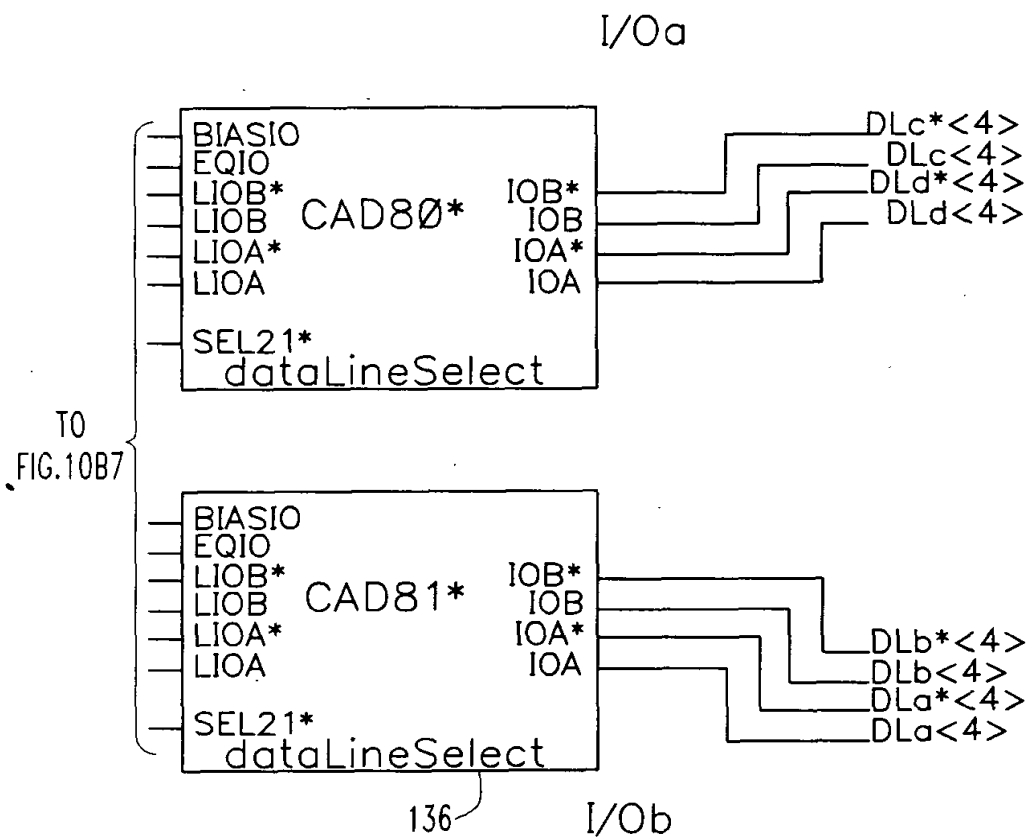


FIG. 10B8



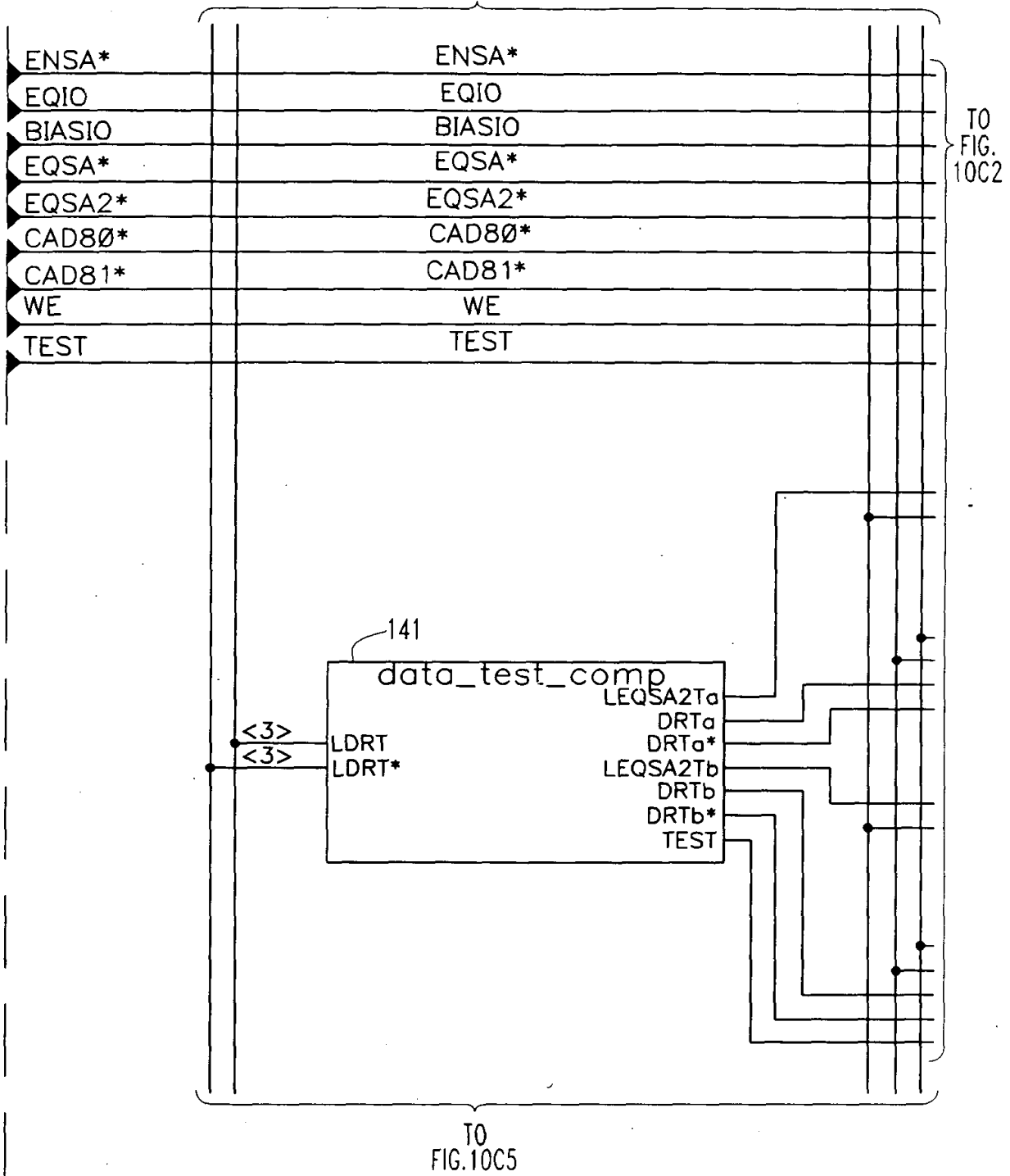
TO
FIG.10B5

FIG.10C1

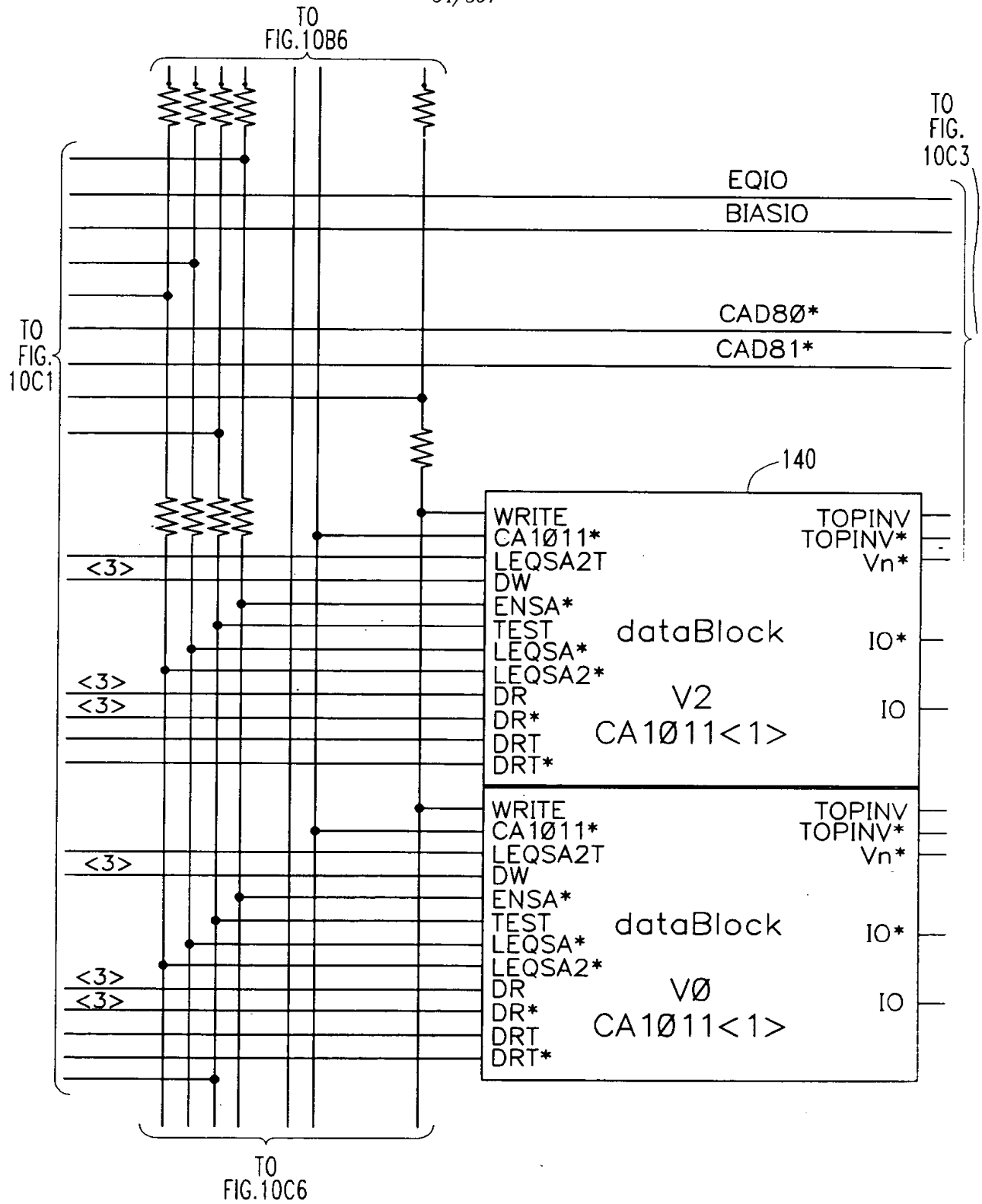


FIG. 10C2

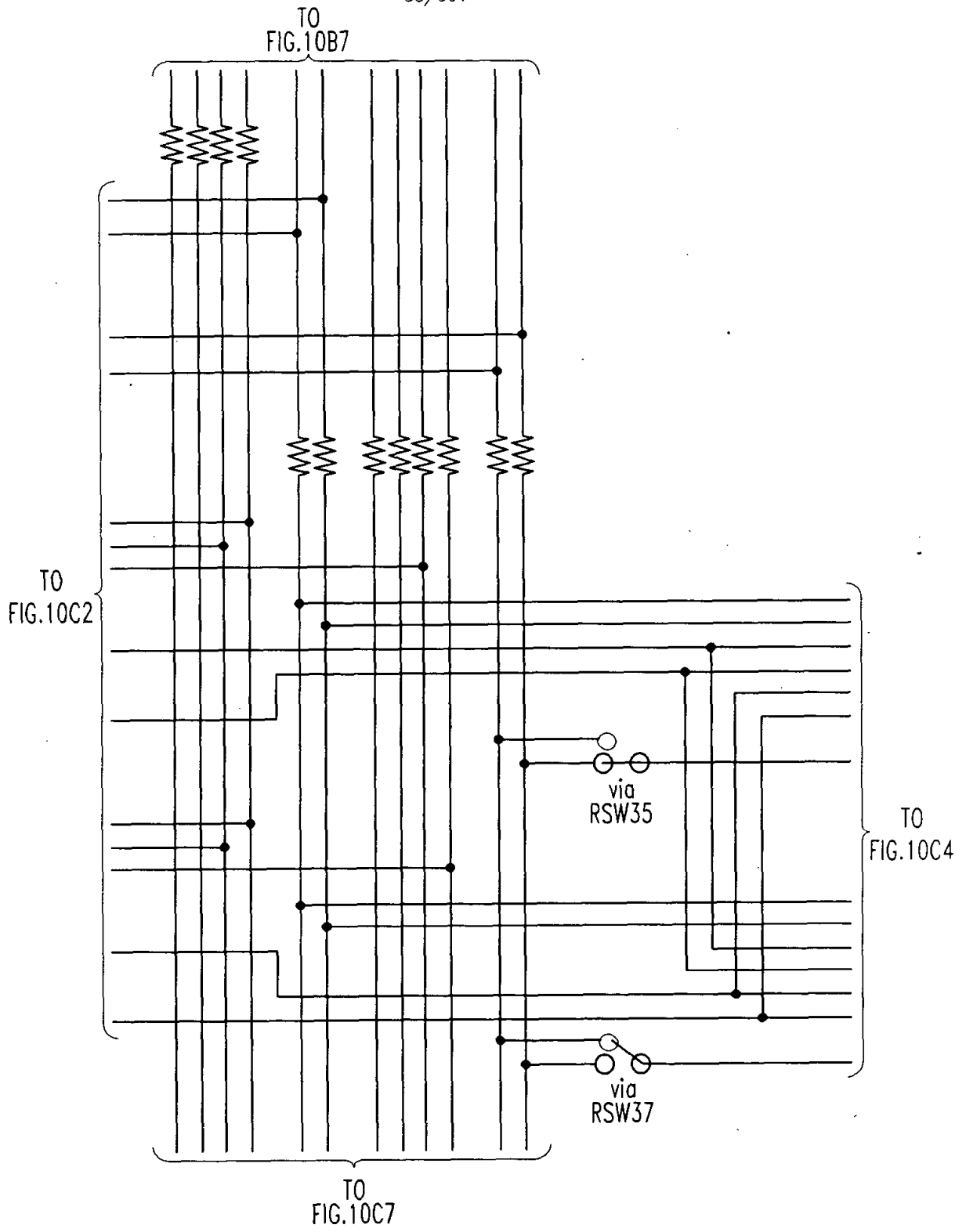
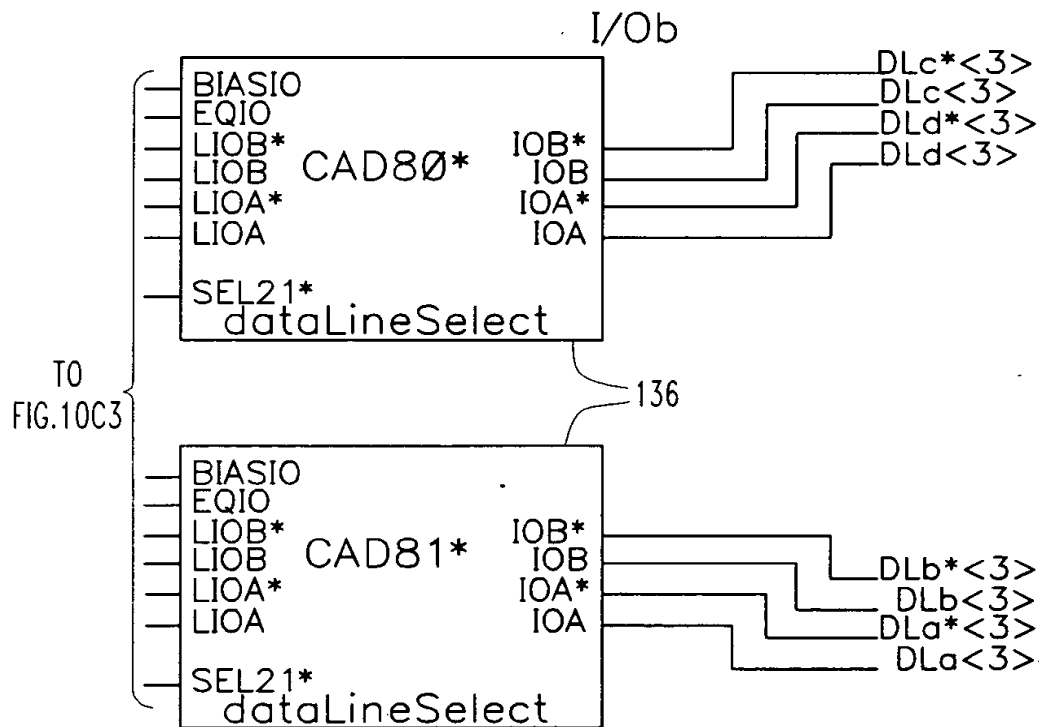


FIG. 10C3

0000459 00001

FIG. 10C4



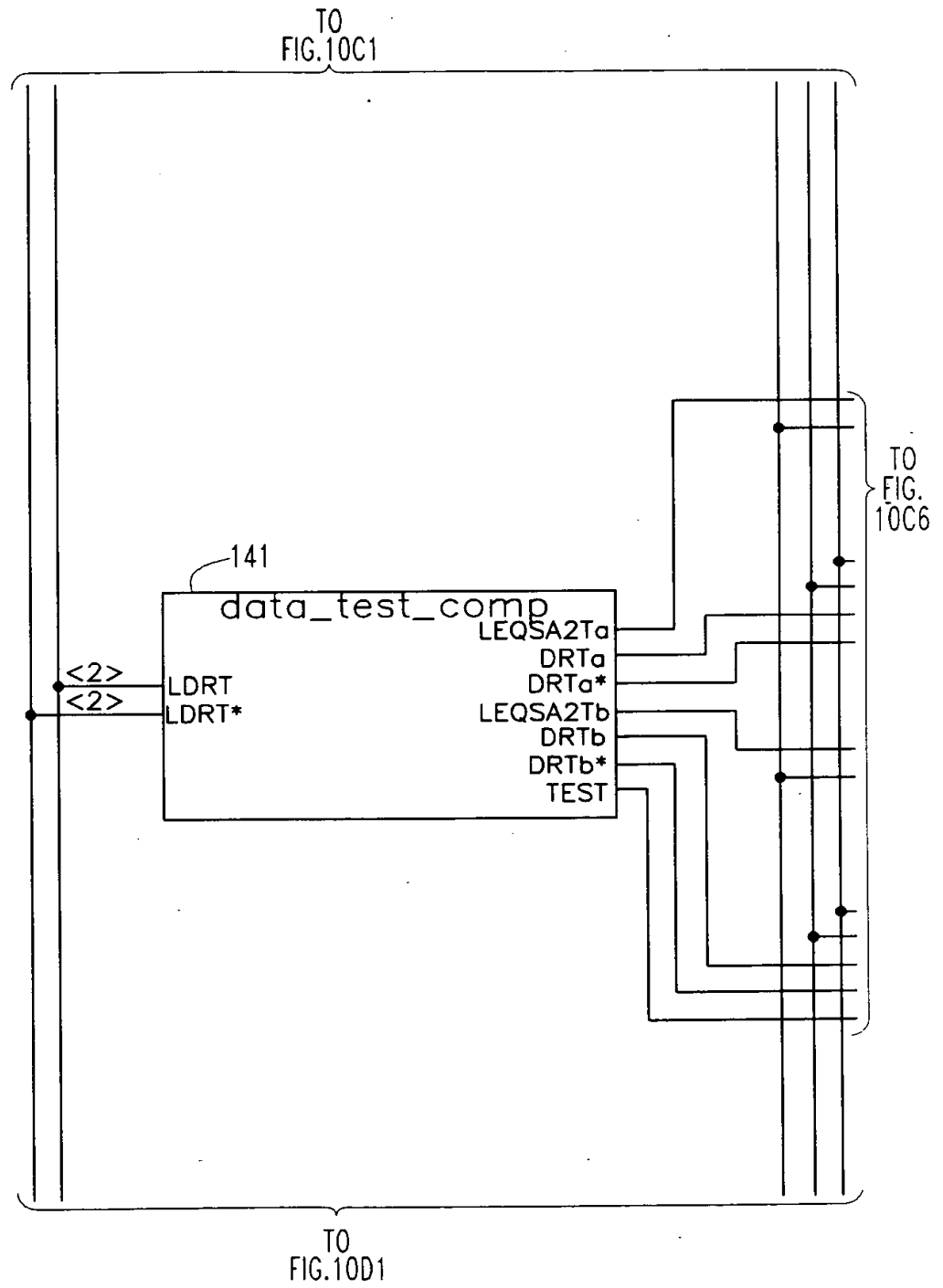


FIG.10C5

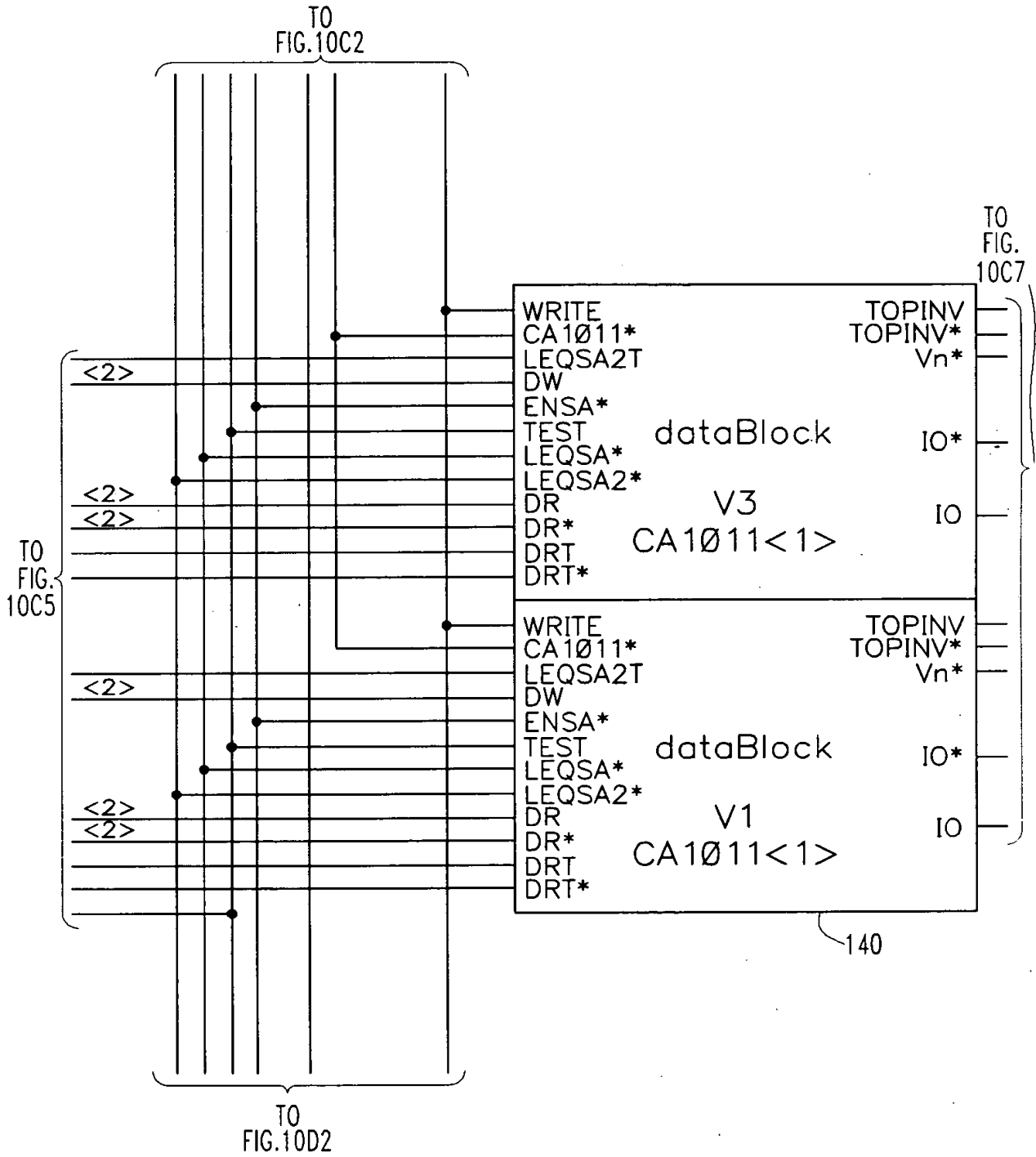


FIG. 10C6

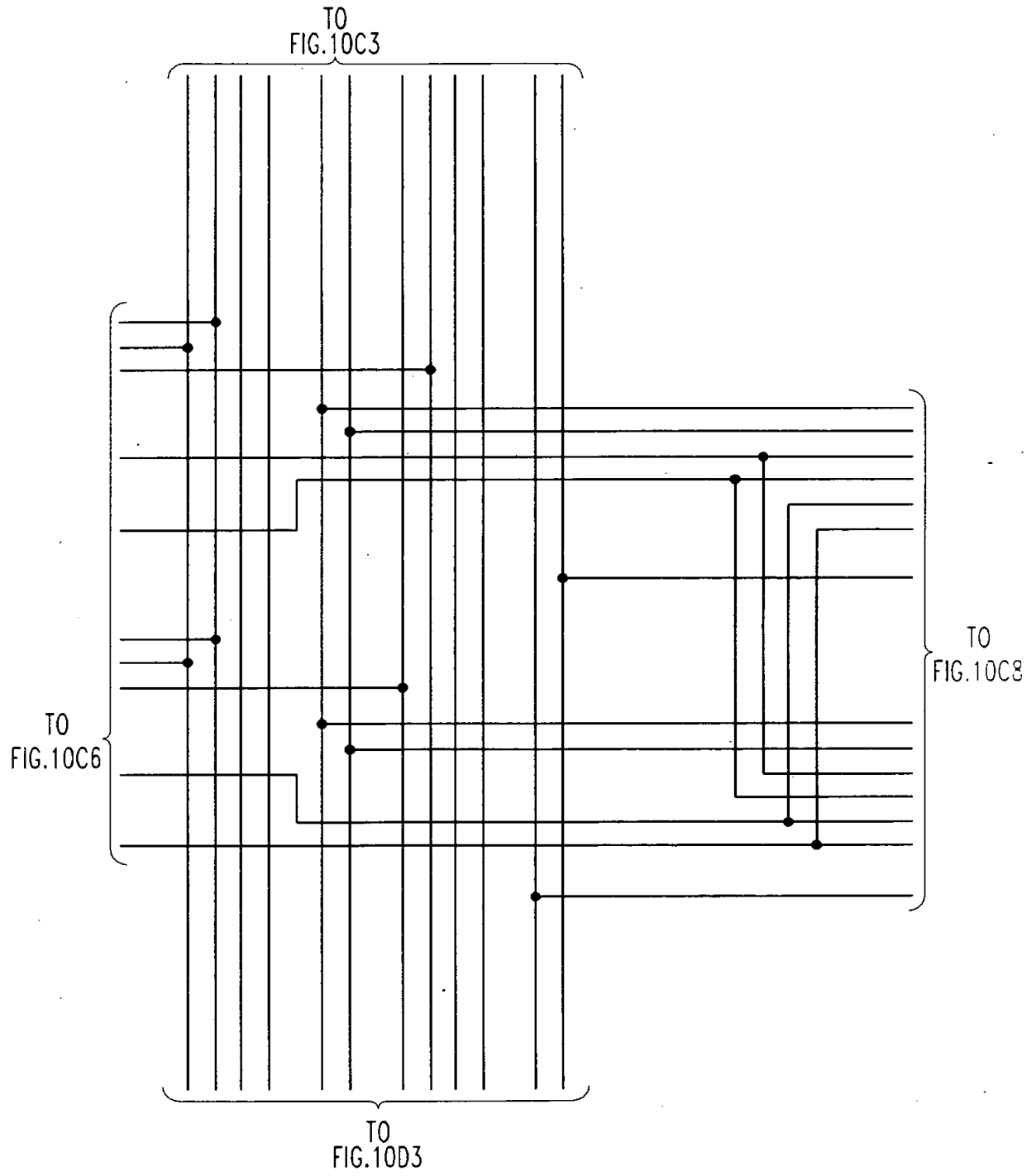


FIG.10C7

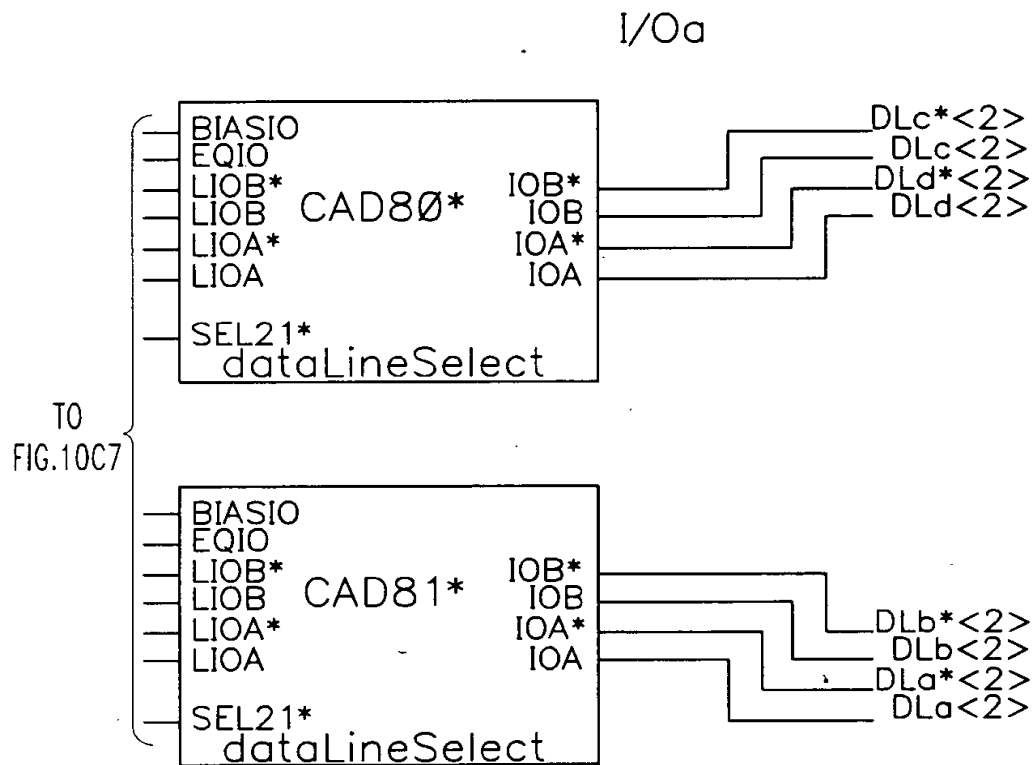


FIG.10C8

FIG. 10D1

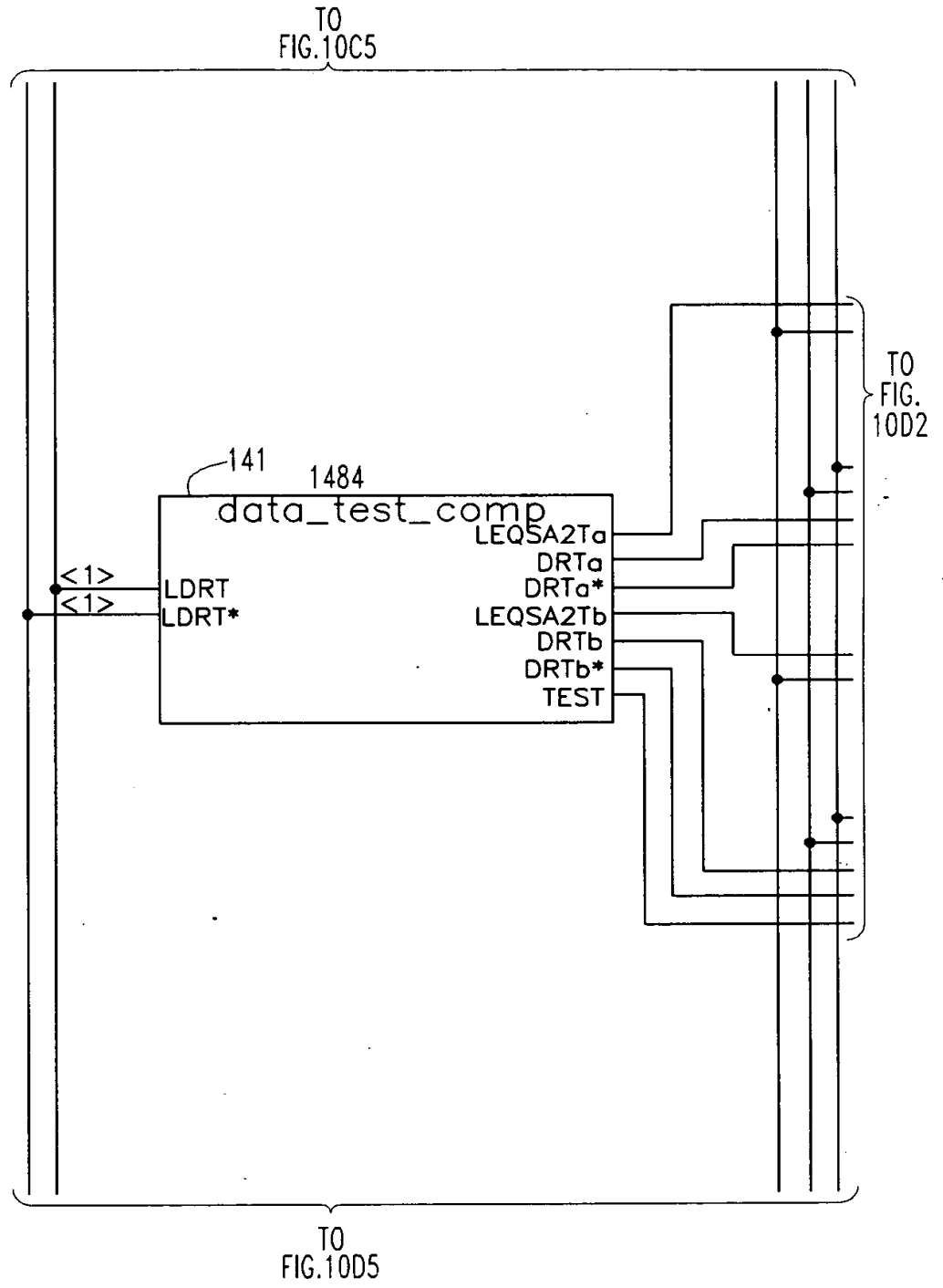


FIG. 10D1

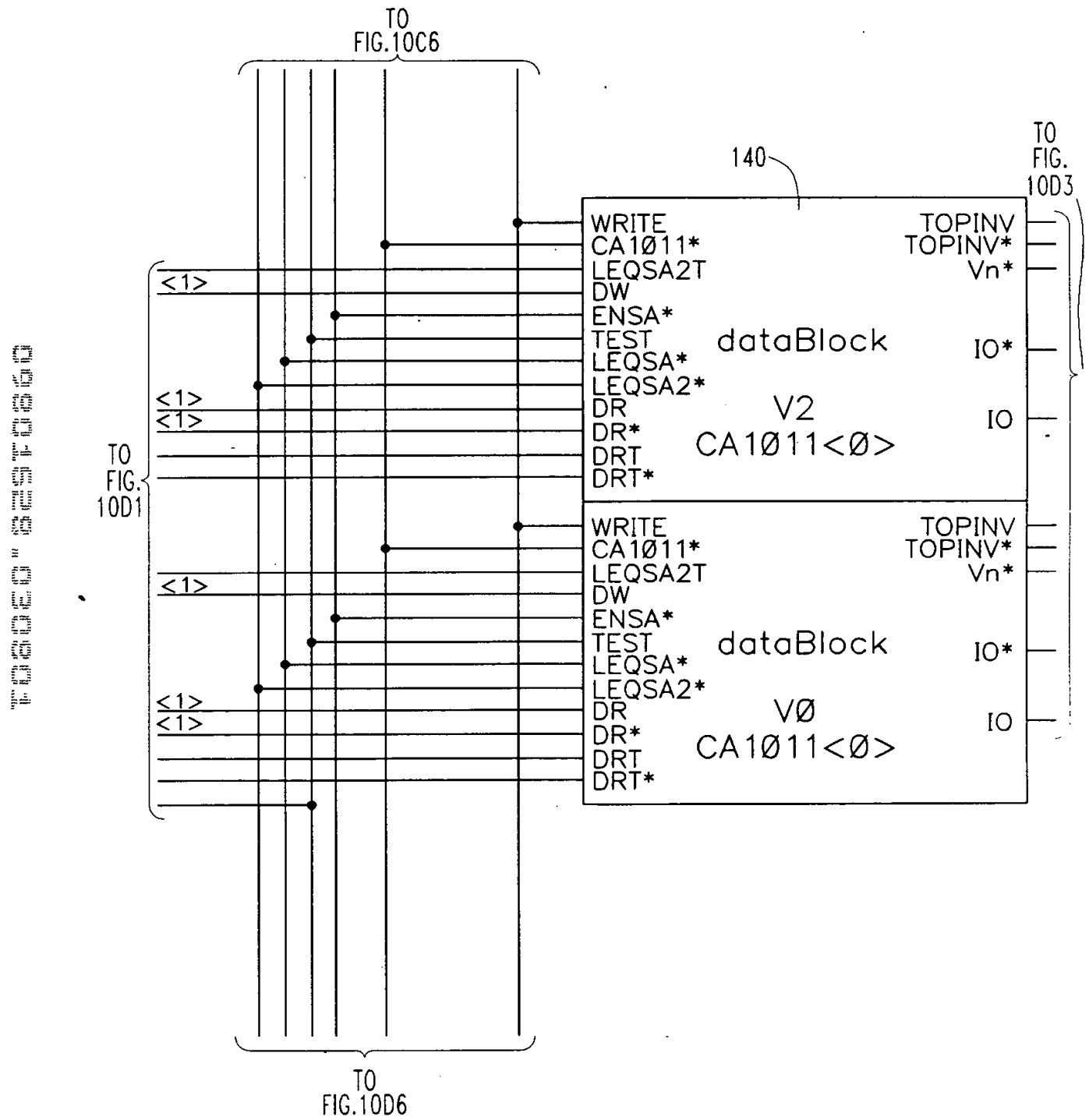


FIG. 10D2

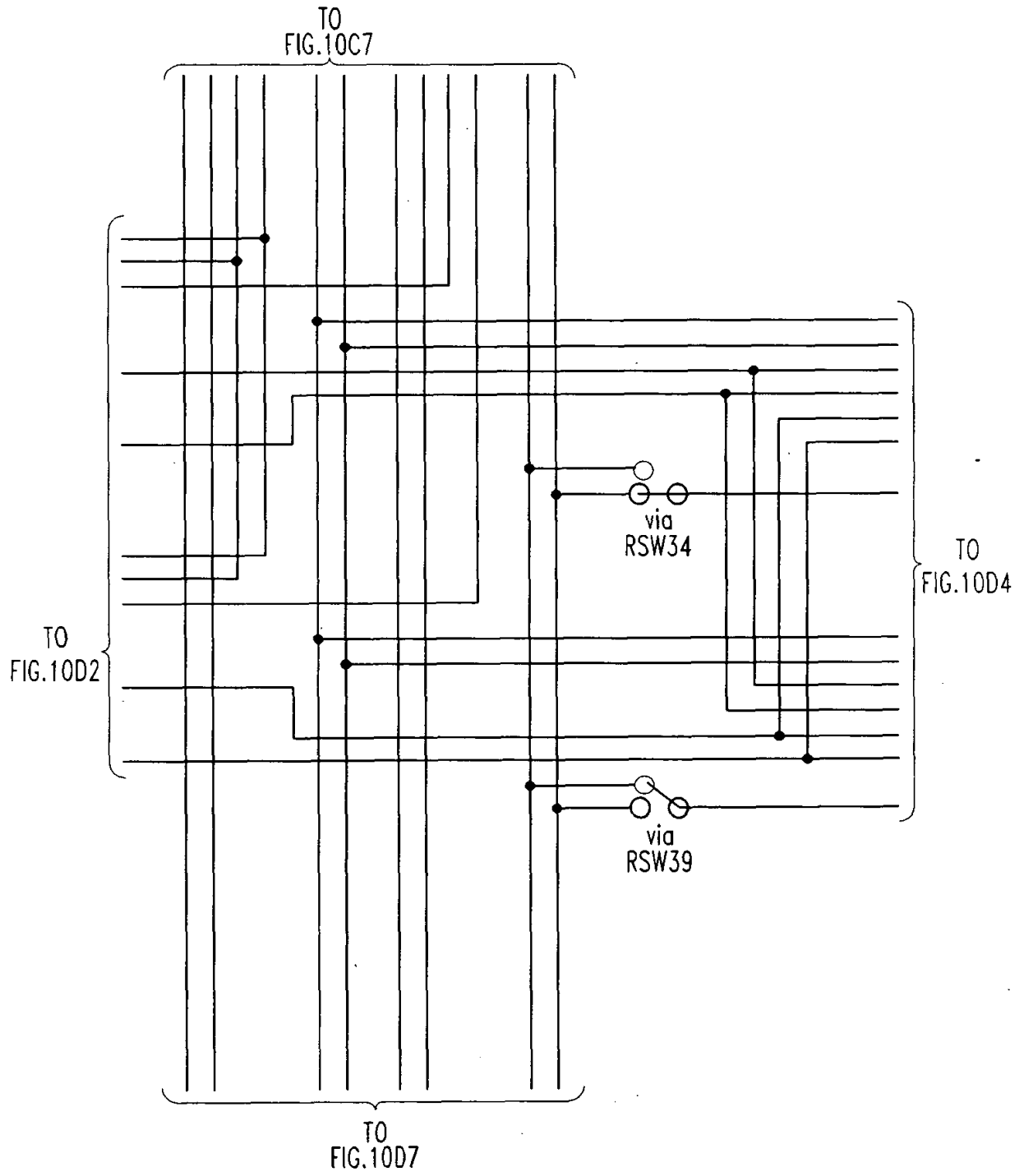


FIG. 10D3

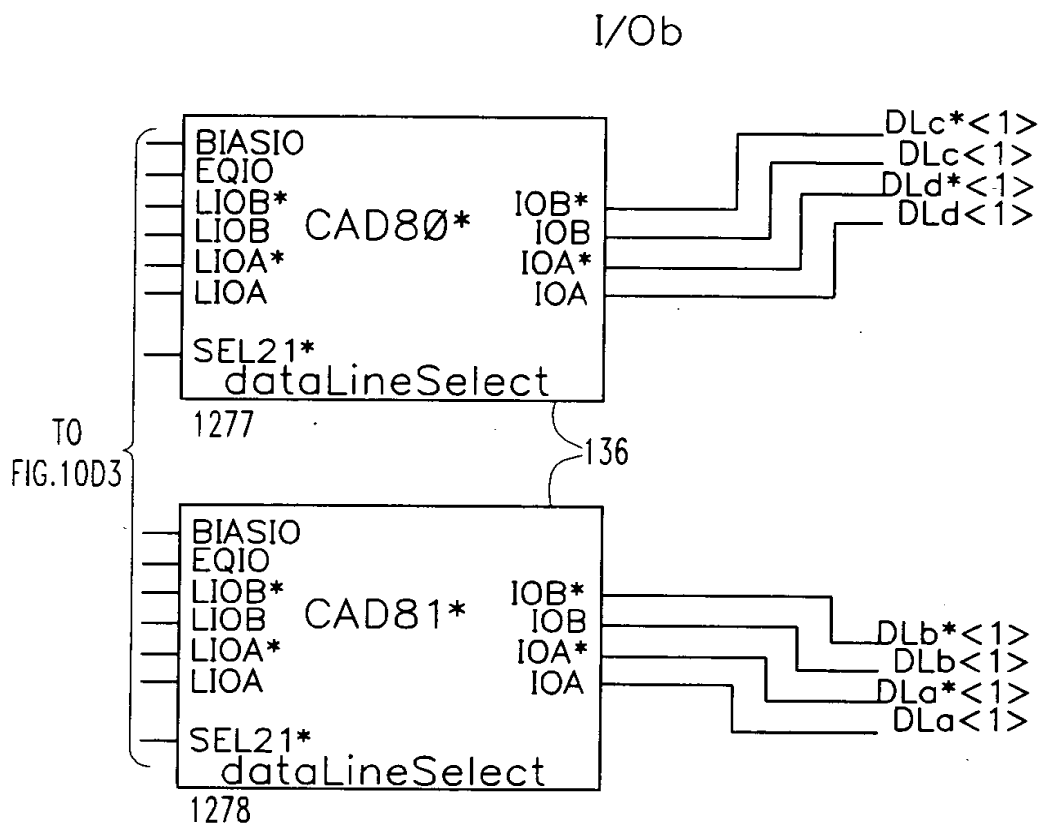


FIG. 10D4

FIG. 10D5

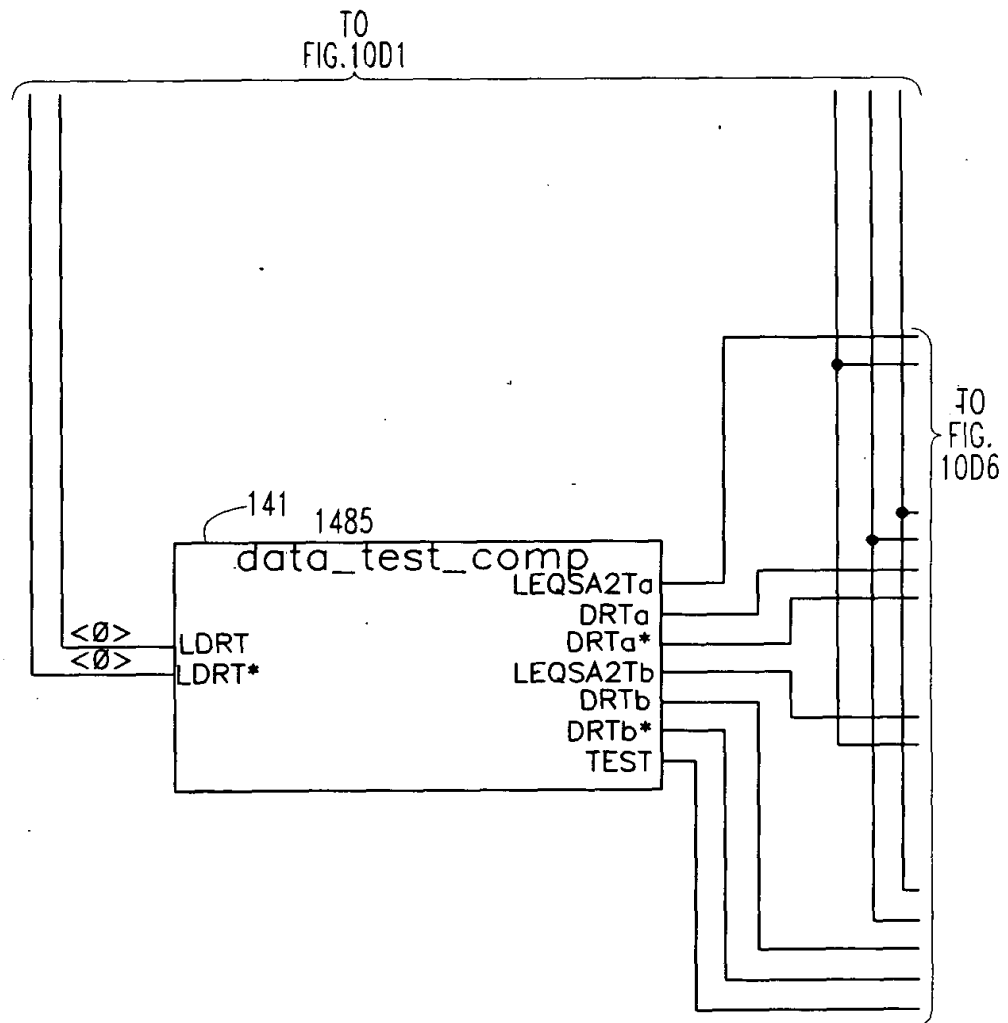


FIG. 10D5

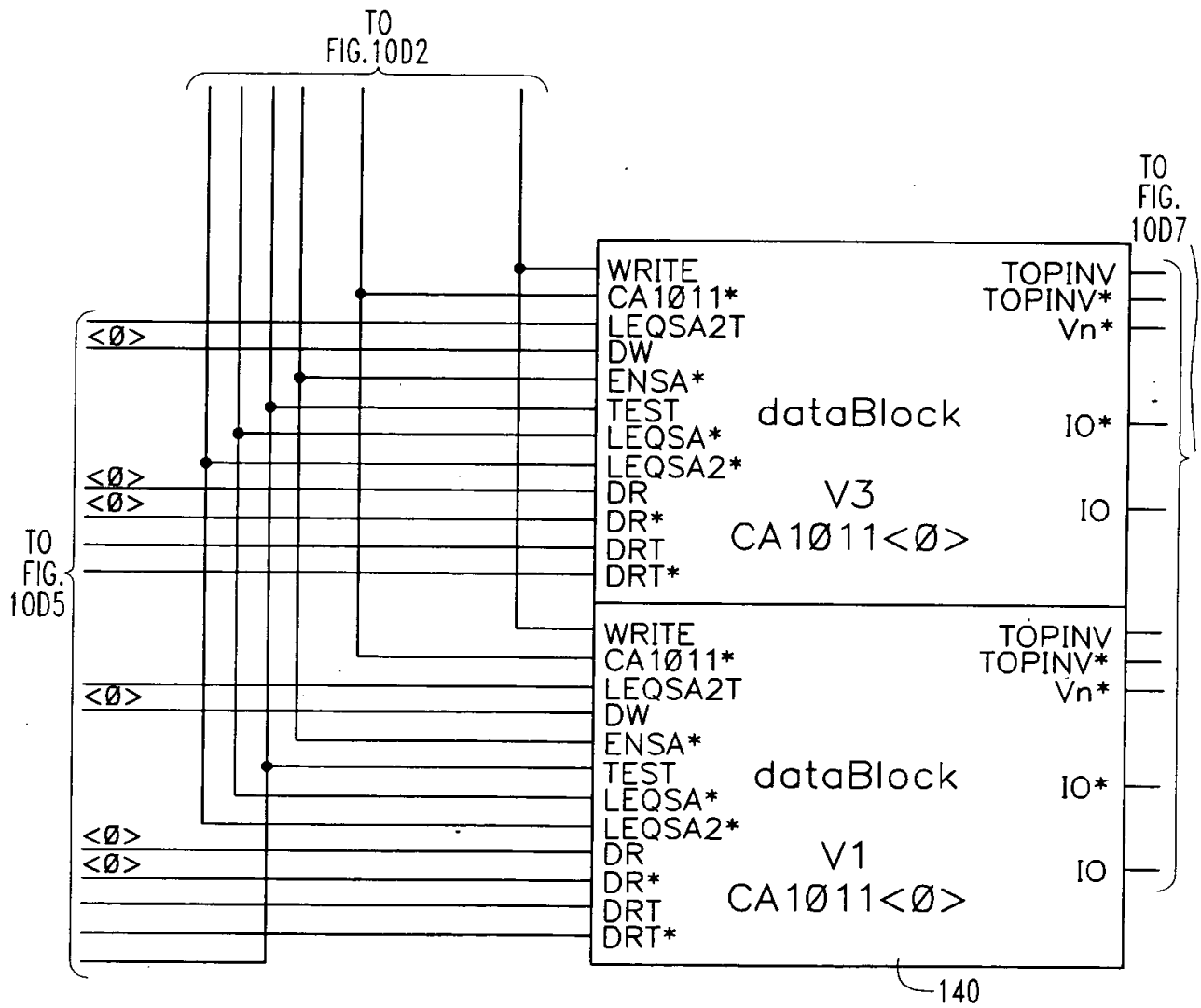


FIG. 10D6

FIG. 10D7

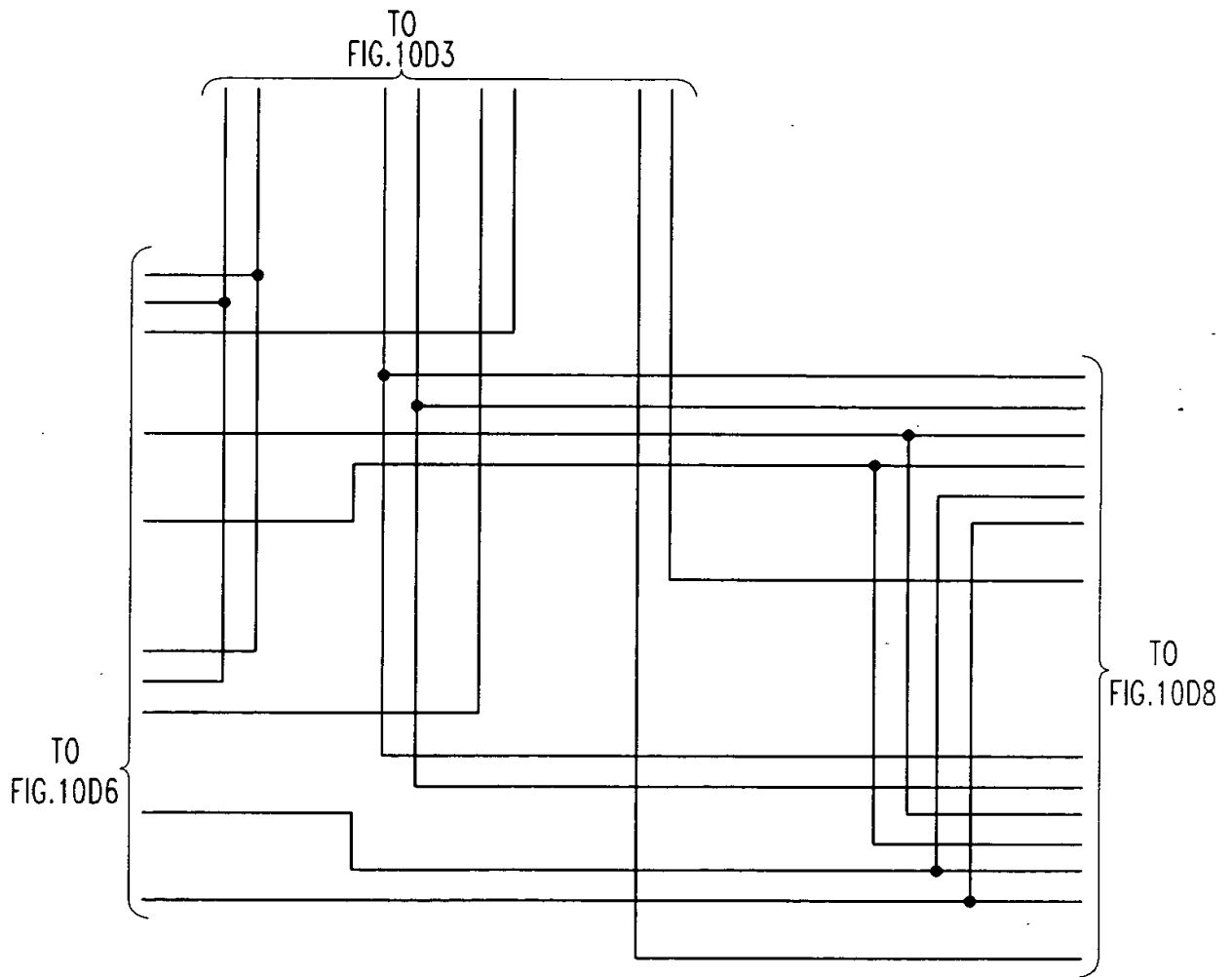


FIG. 10D7

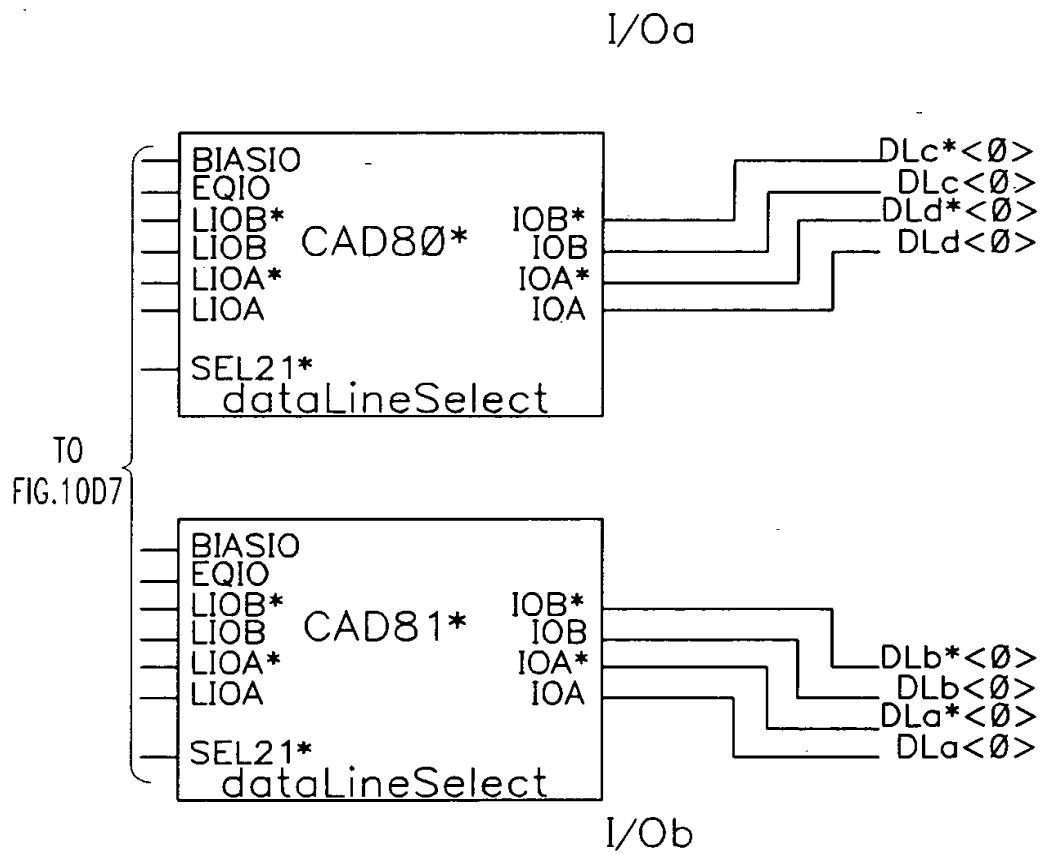


FIG.10D8

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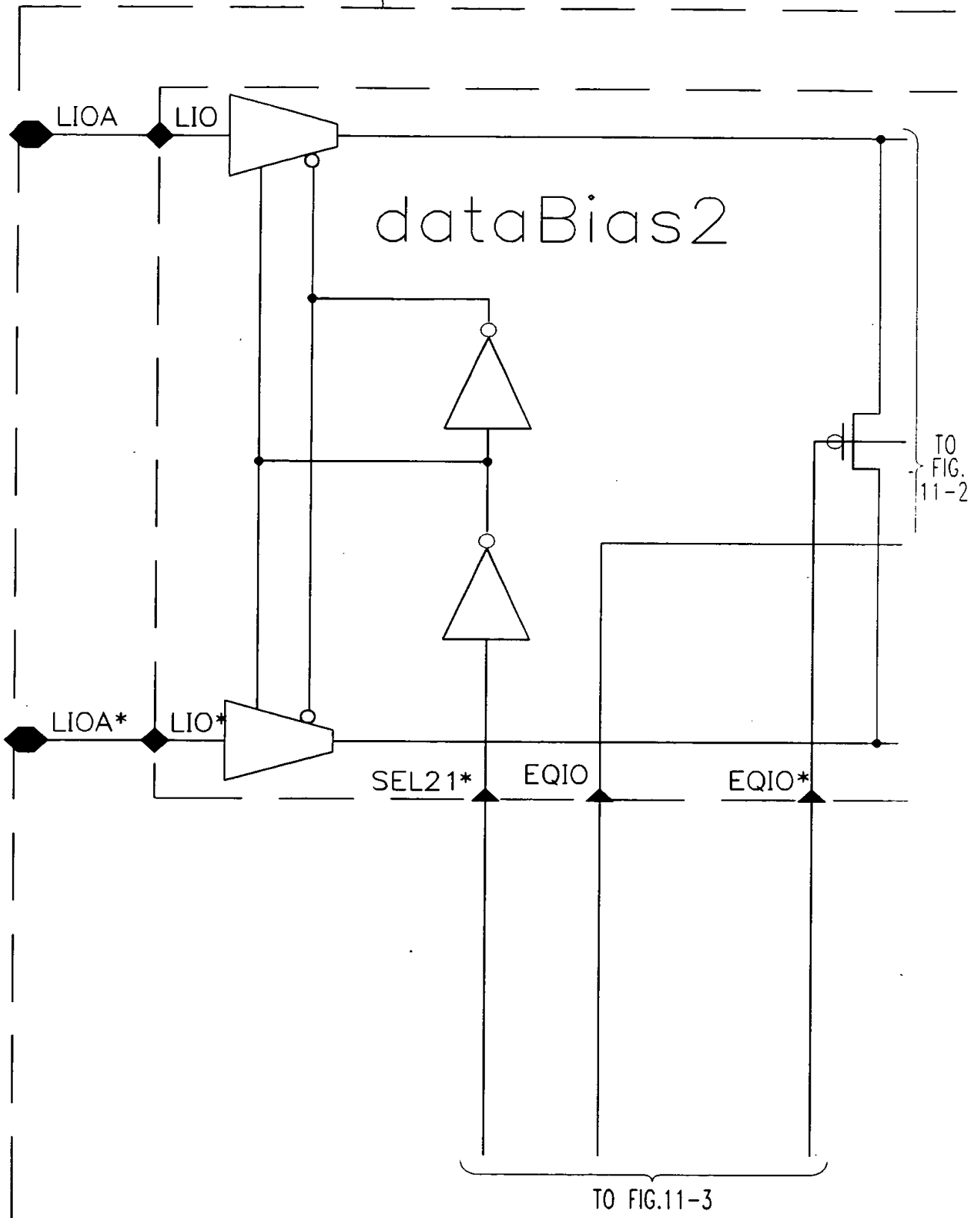
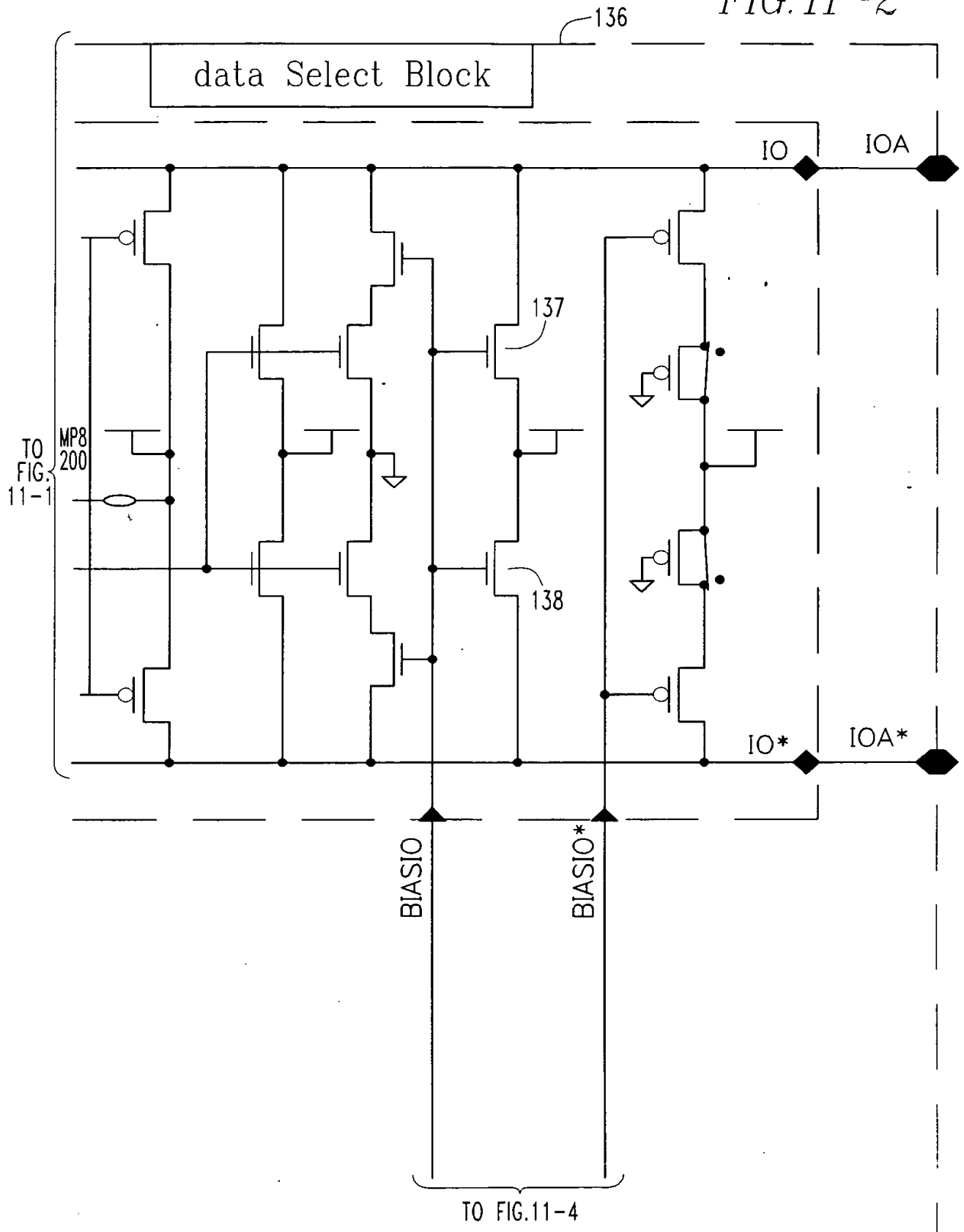


FIG. 11-2



TO FIG. 11-1

TO FIG. 11-4

FIG. 11-4

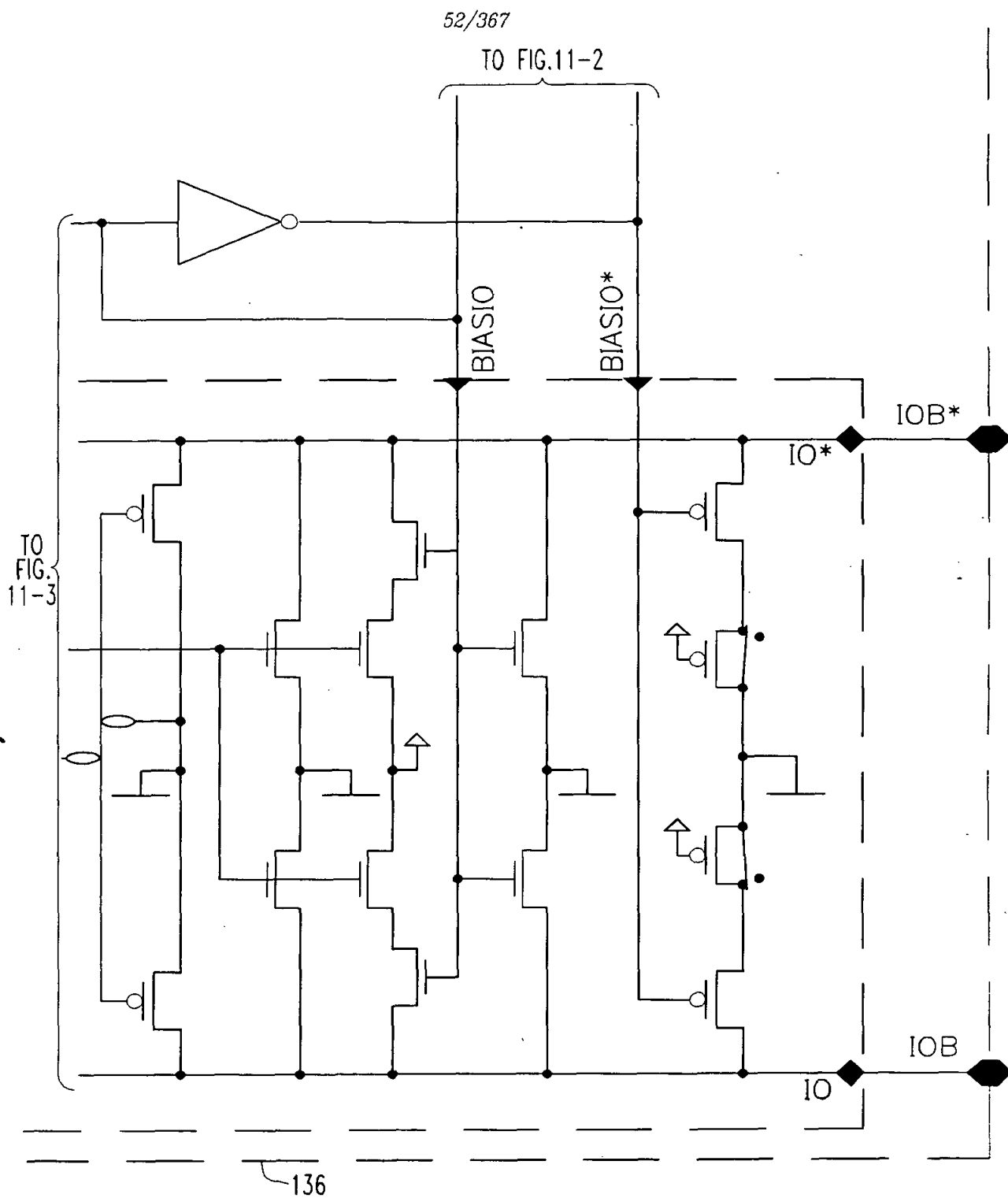


FIG. 11-4

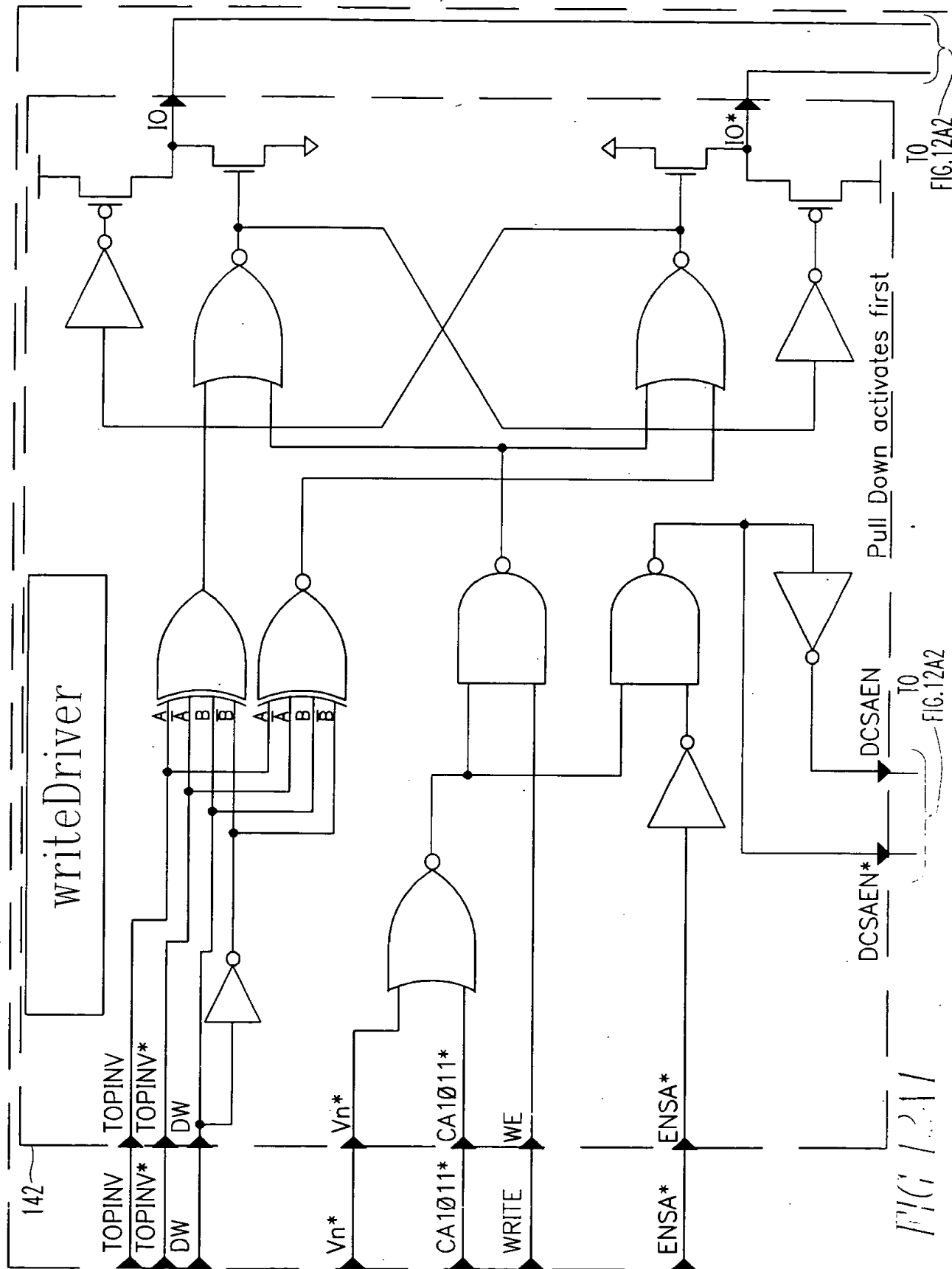


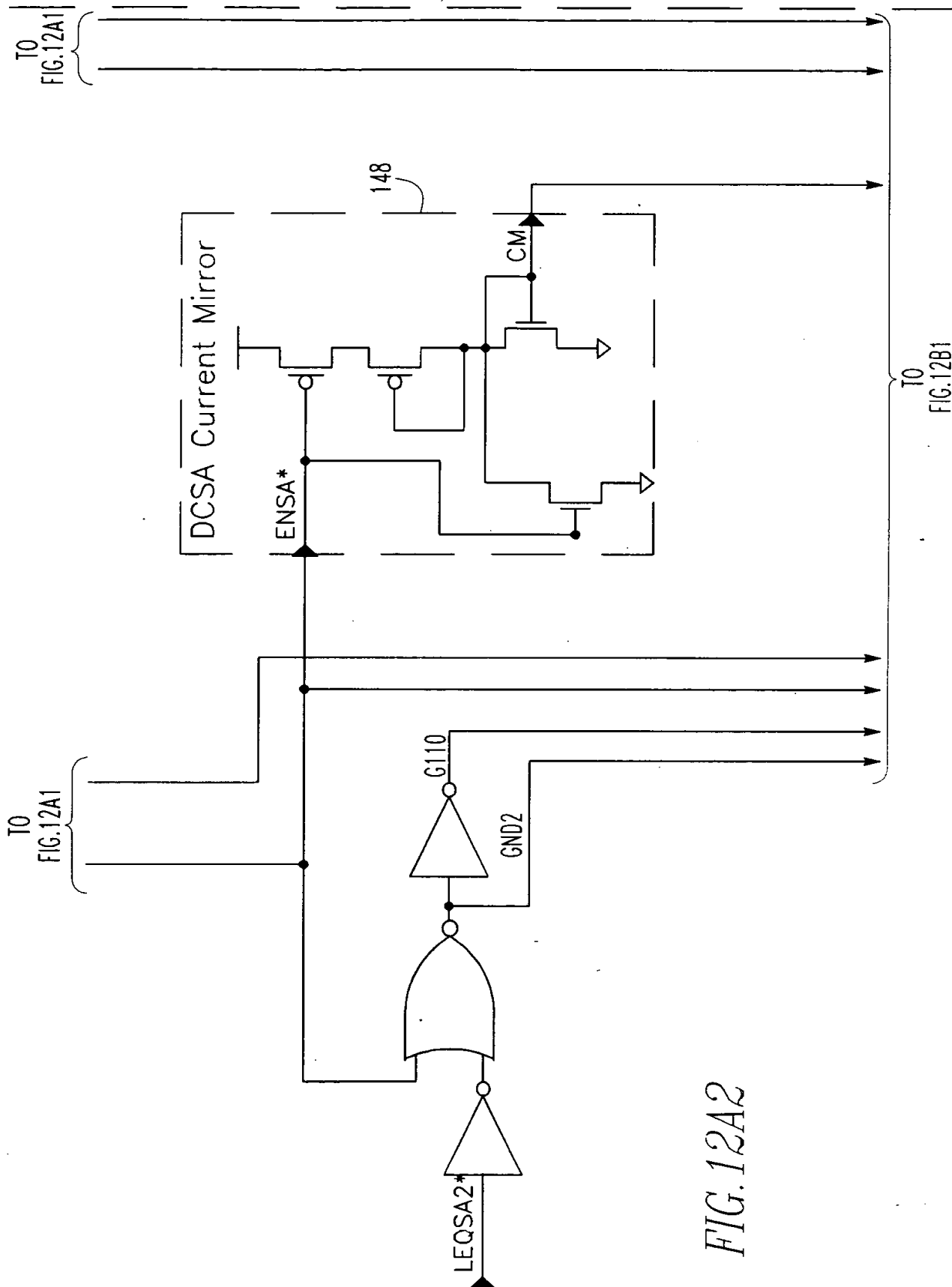
FIG 12A1

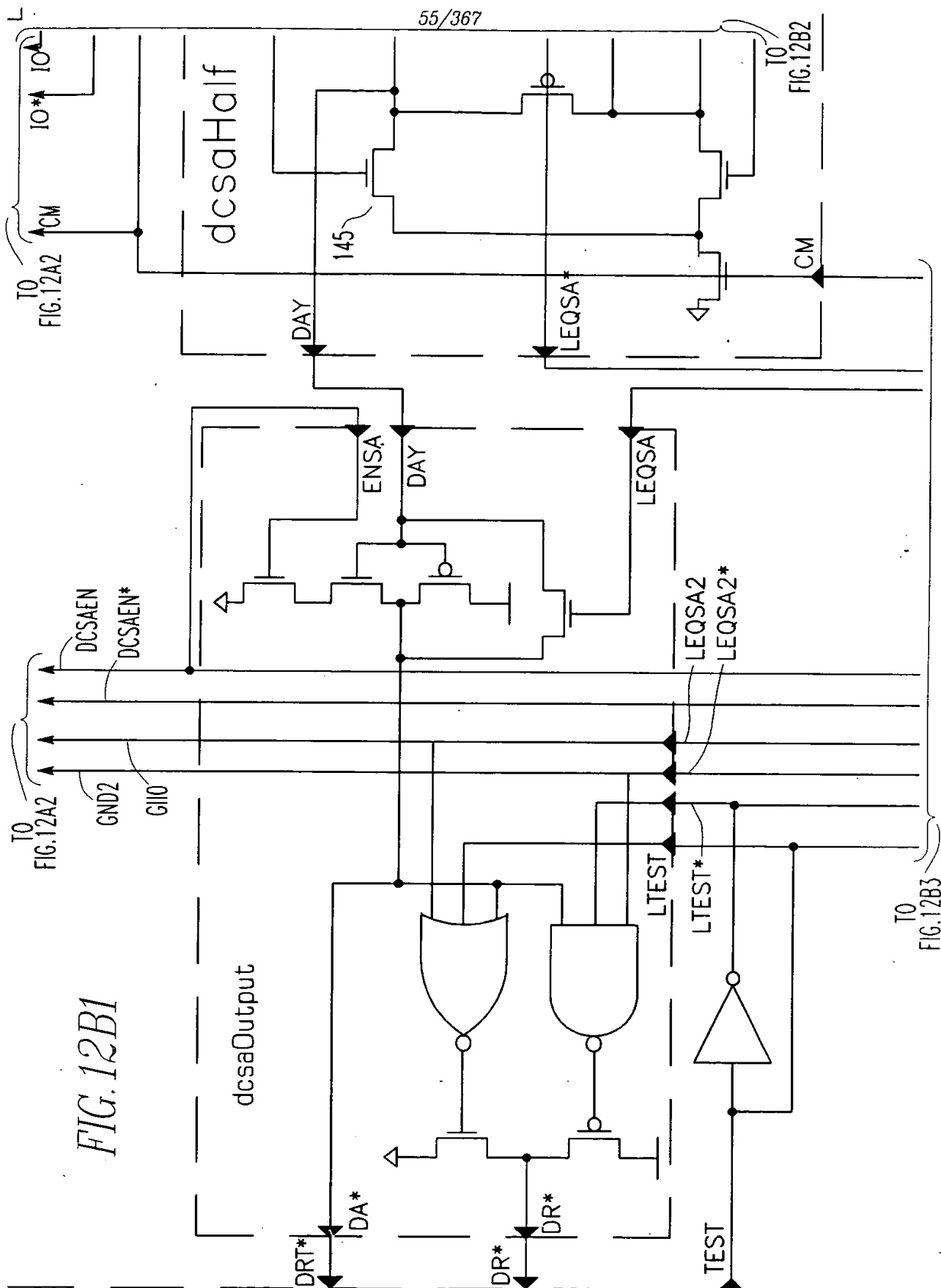
Pull Down activates first

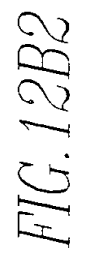
DCSAEN*

DCSAEN

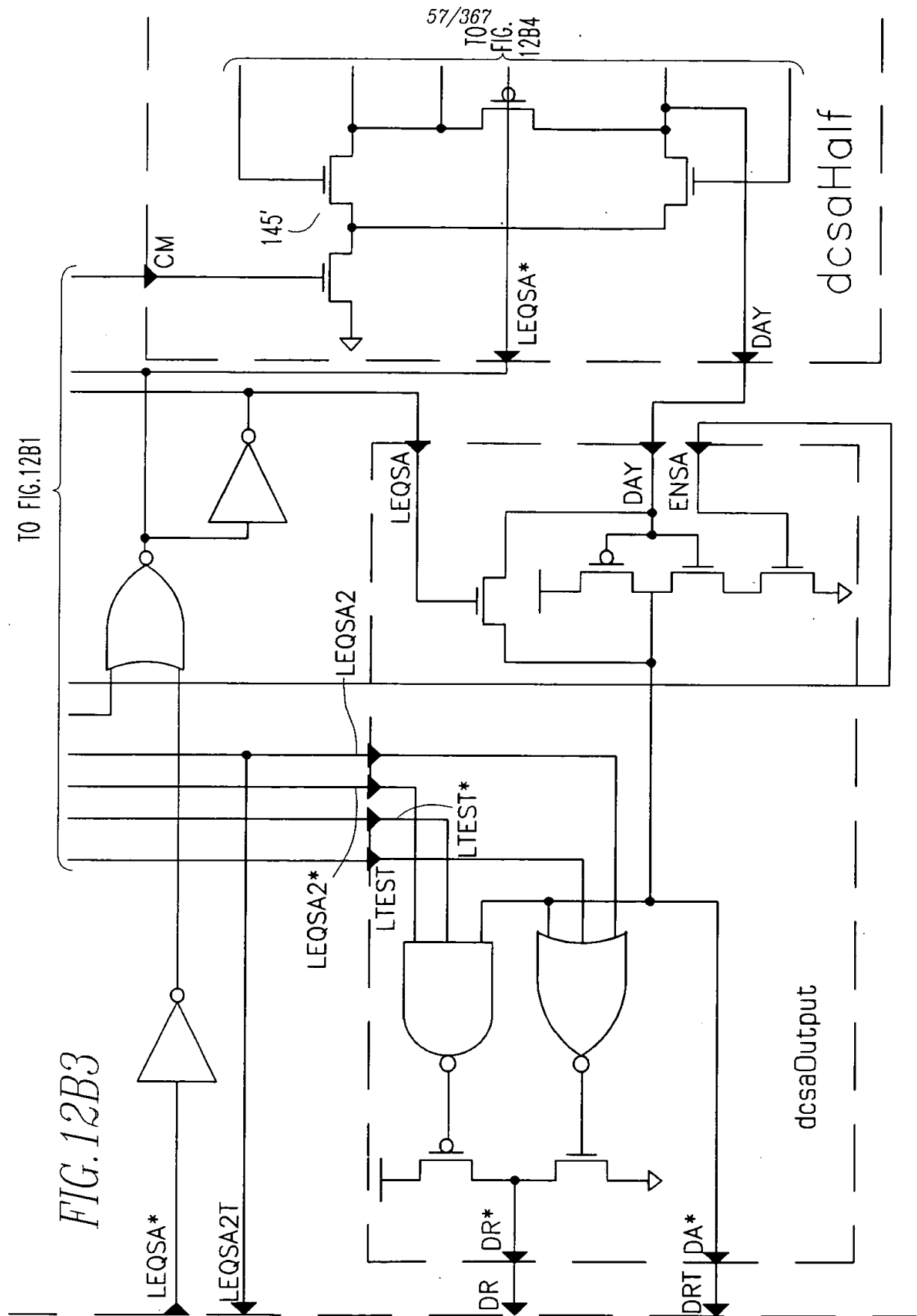
FIG.12A2







TO FIG. 12B4.



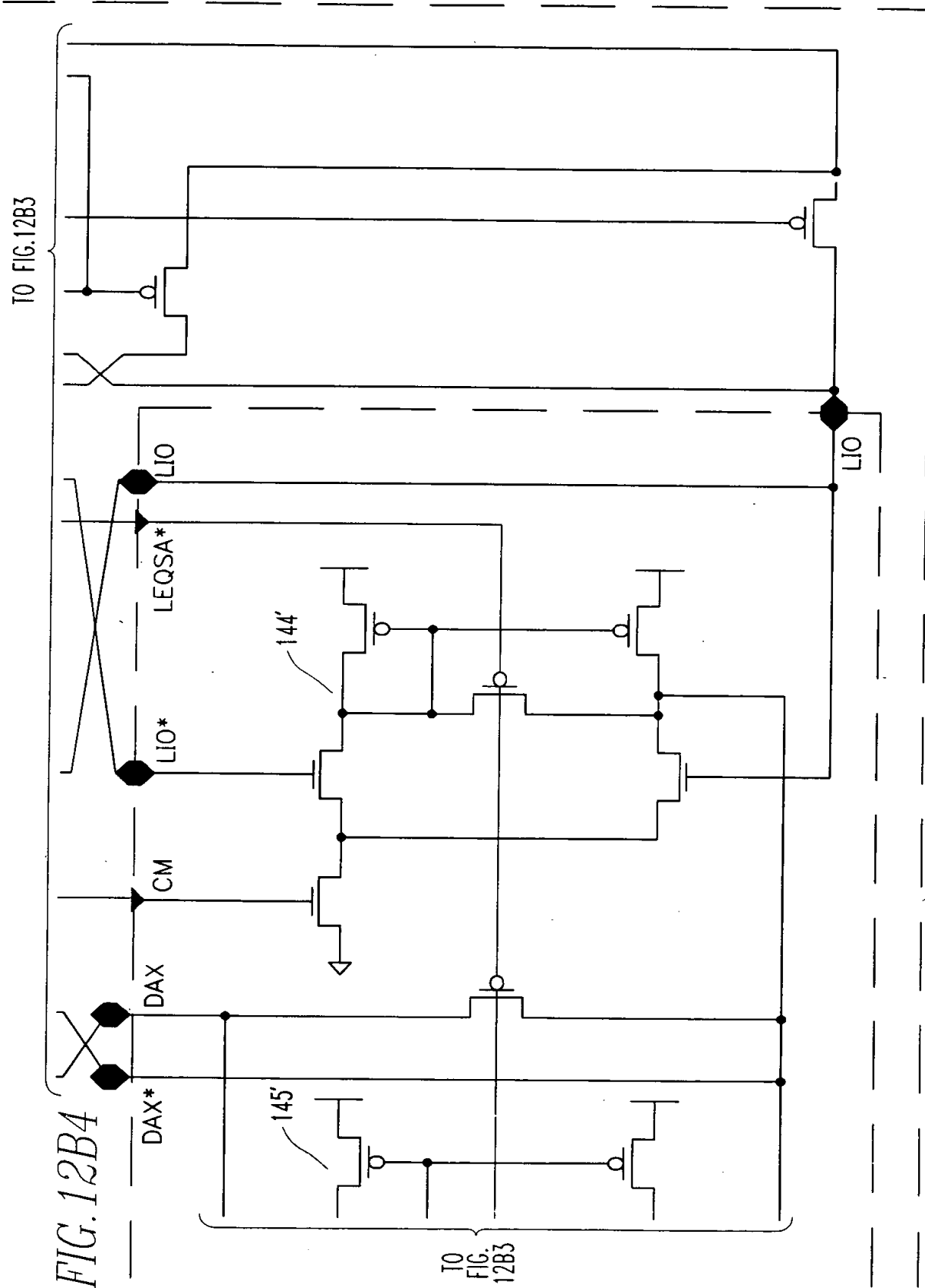


FIG. 13A

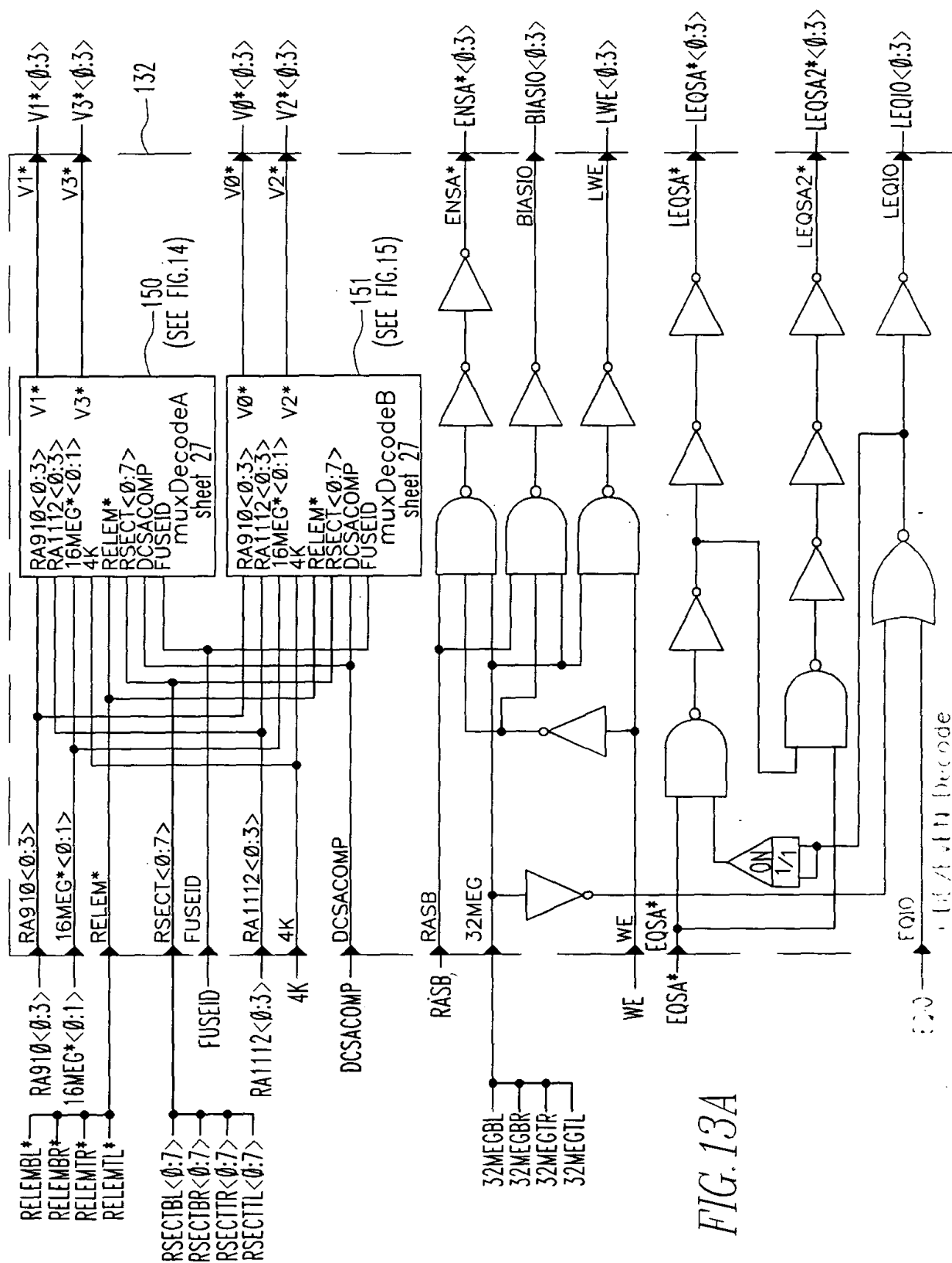


FIG. 13A

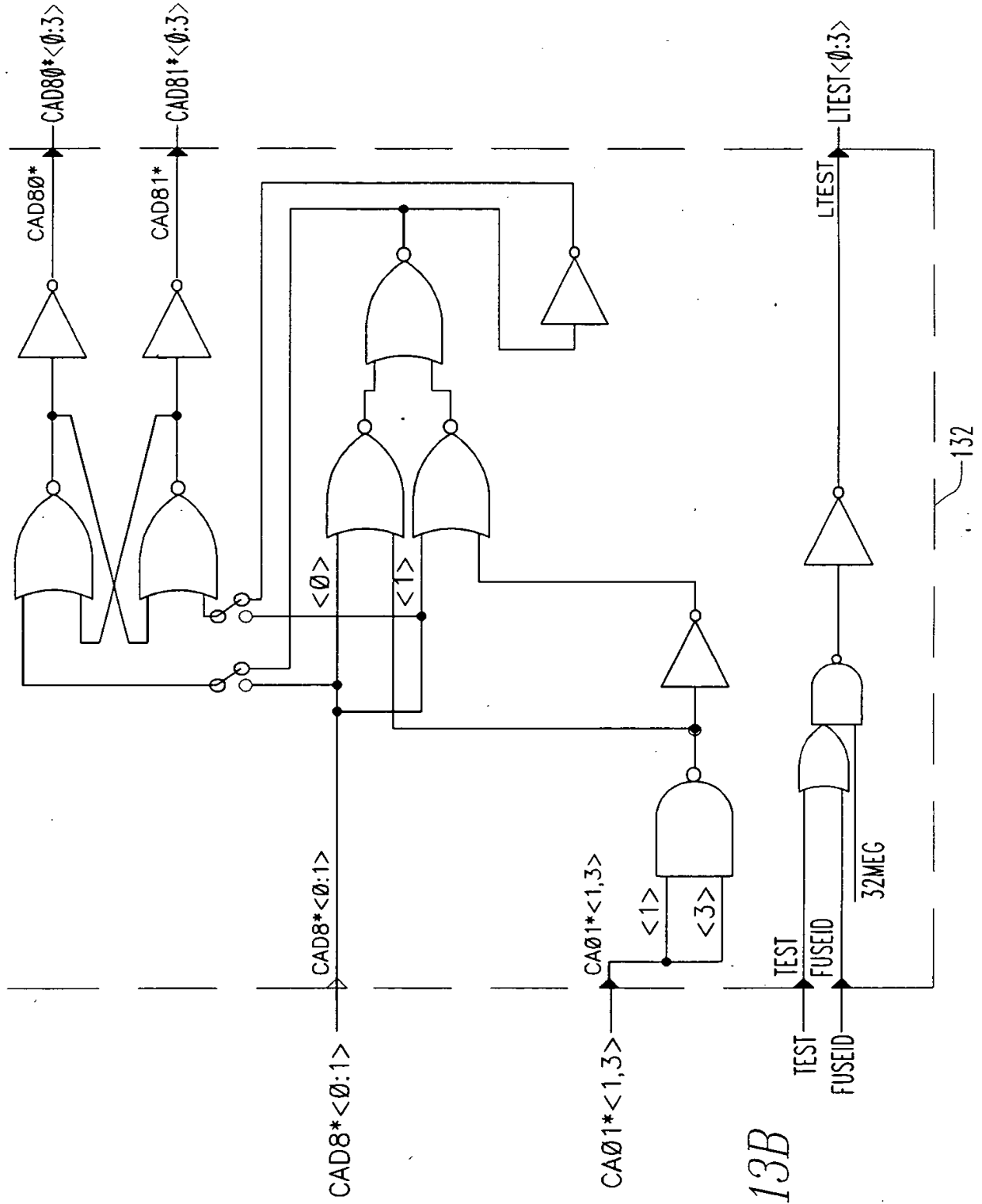


FIG. 13B

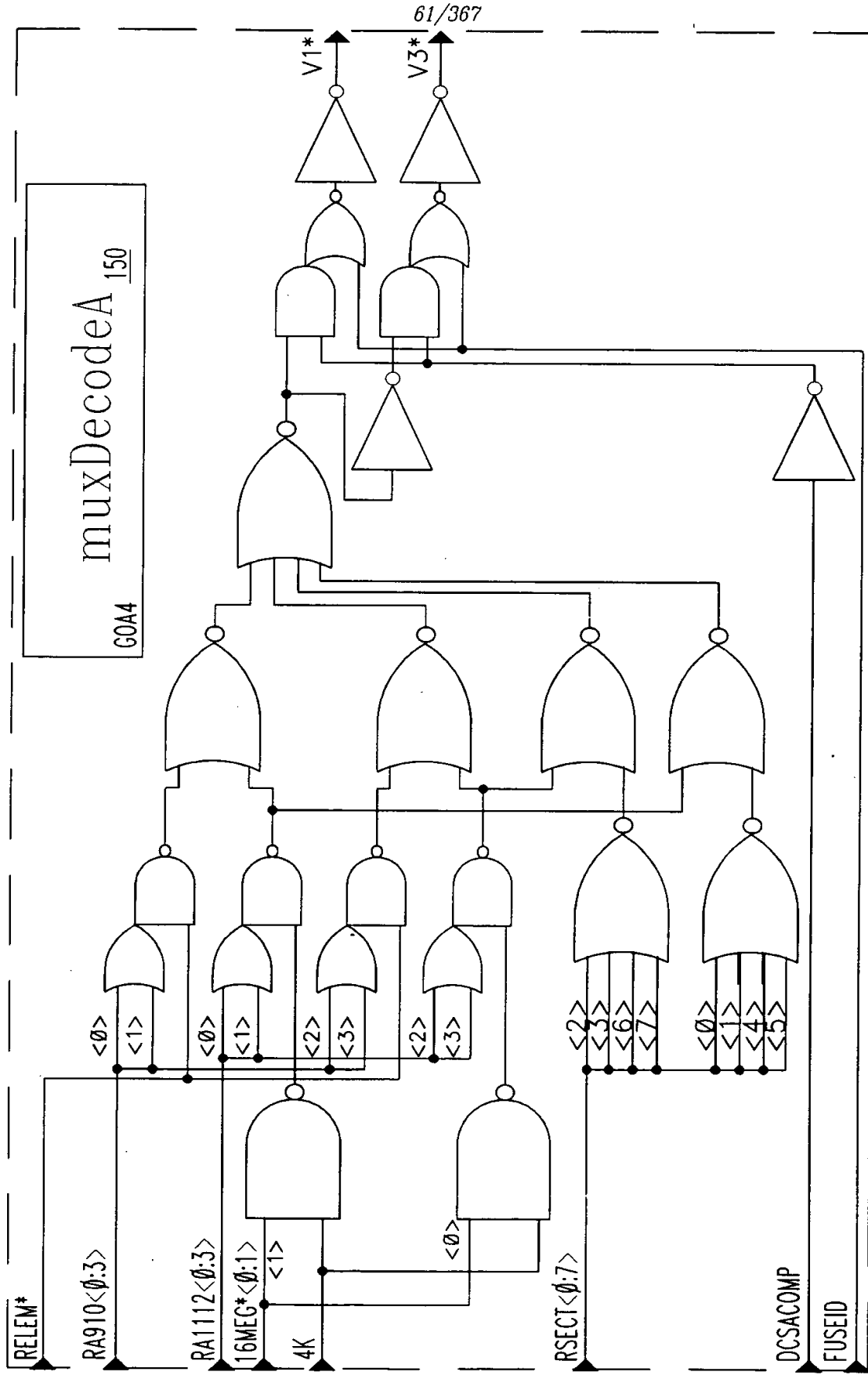


FIG. 14

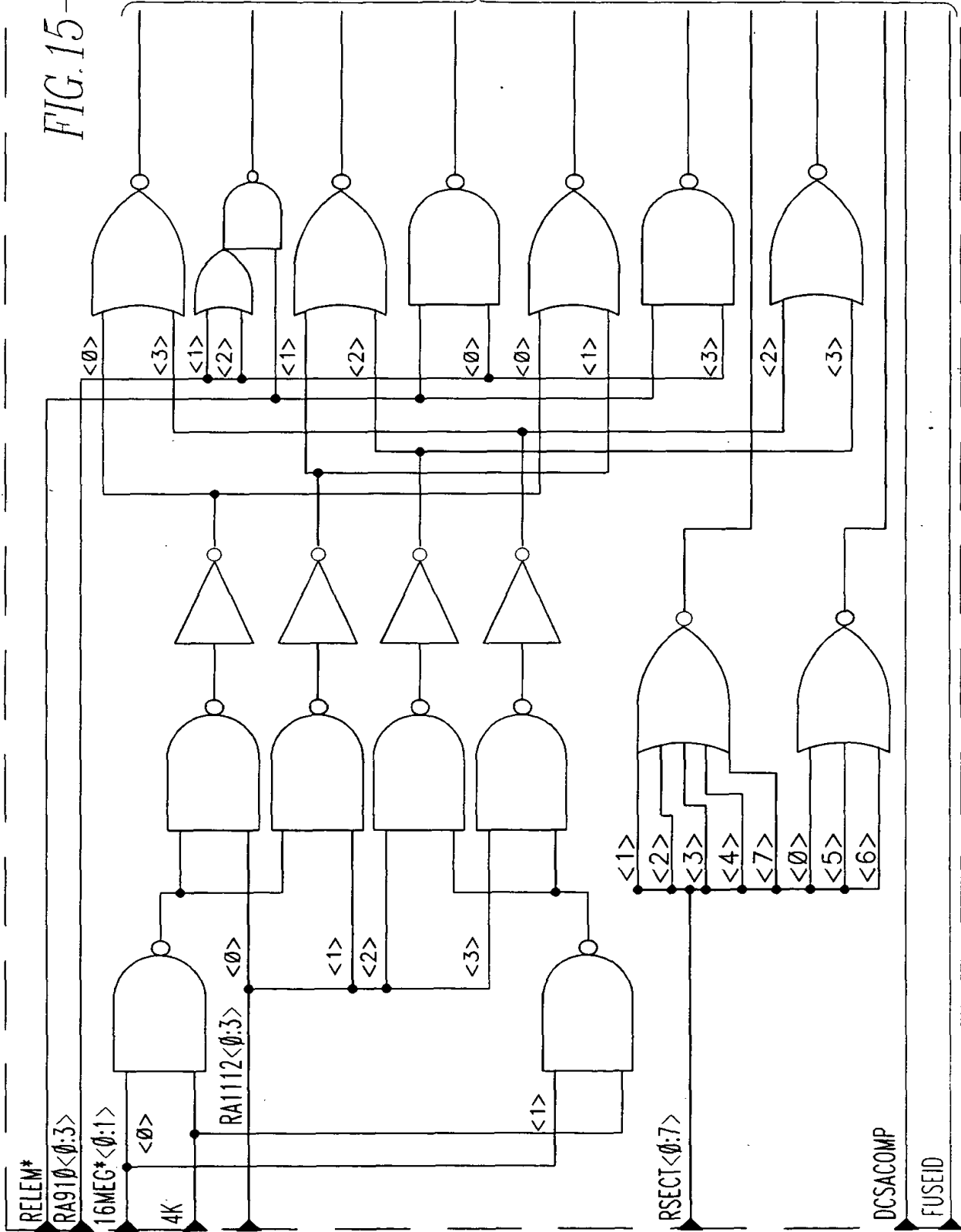


FIG. 15-2

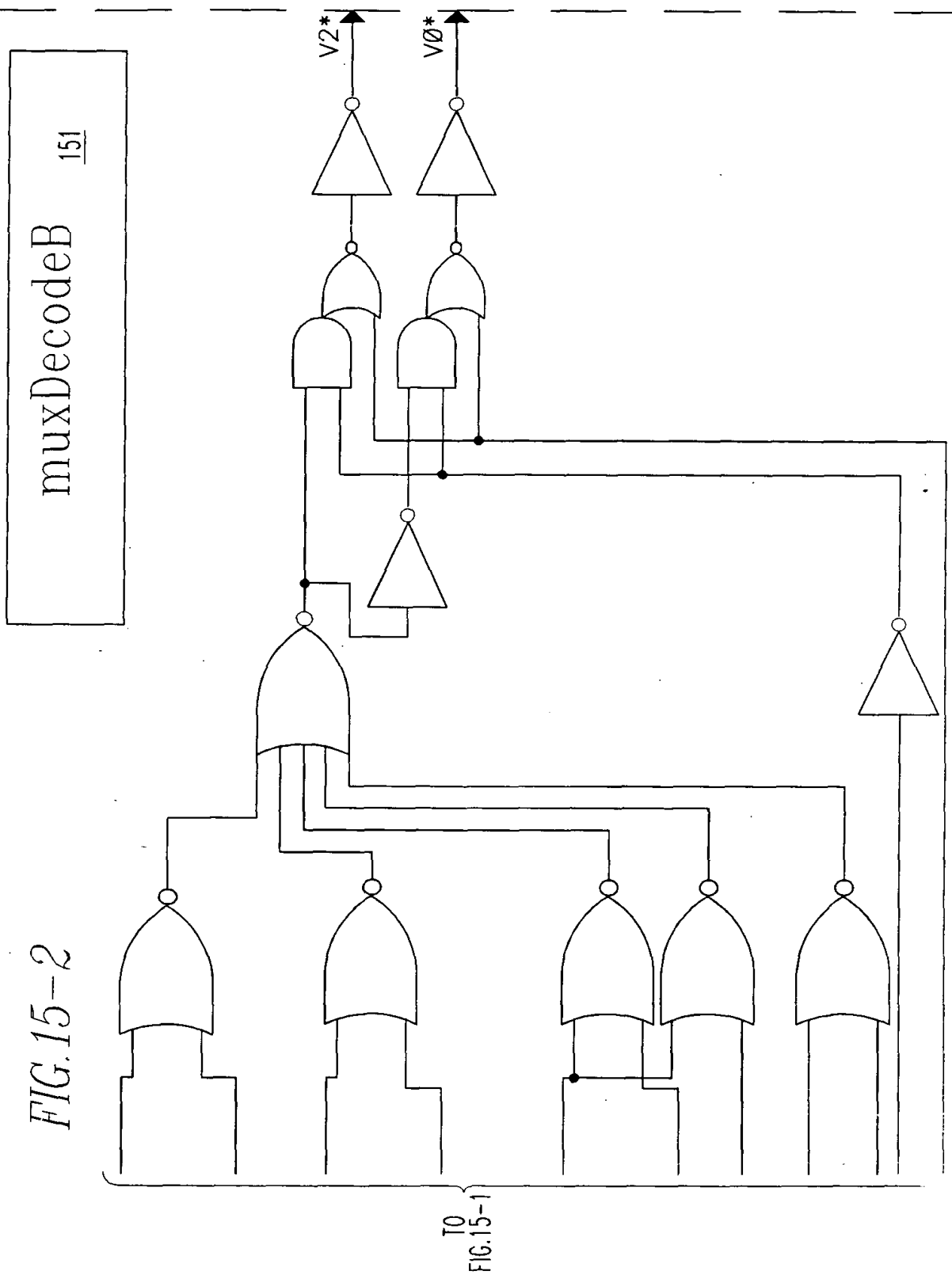
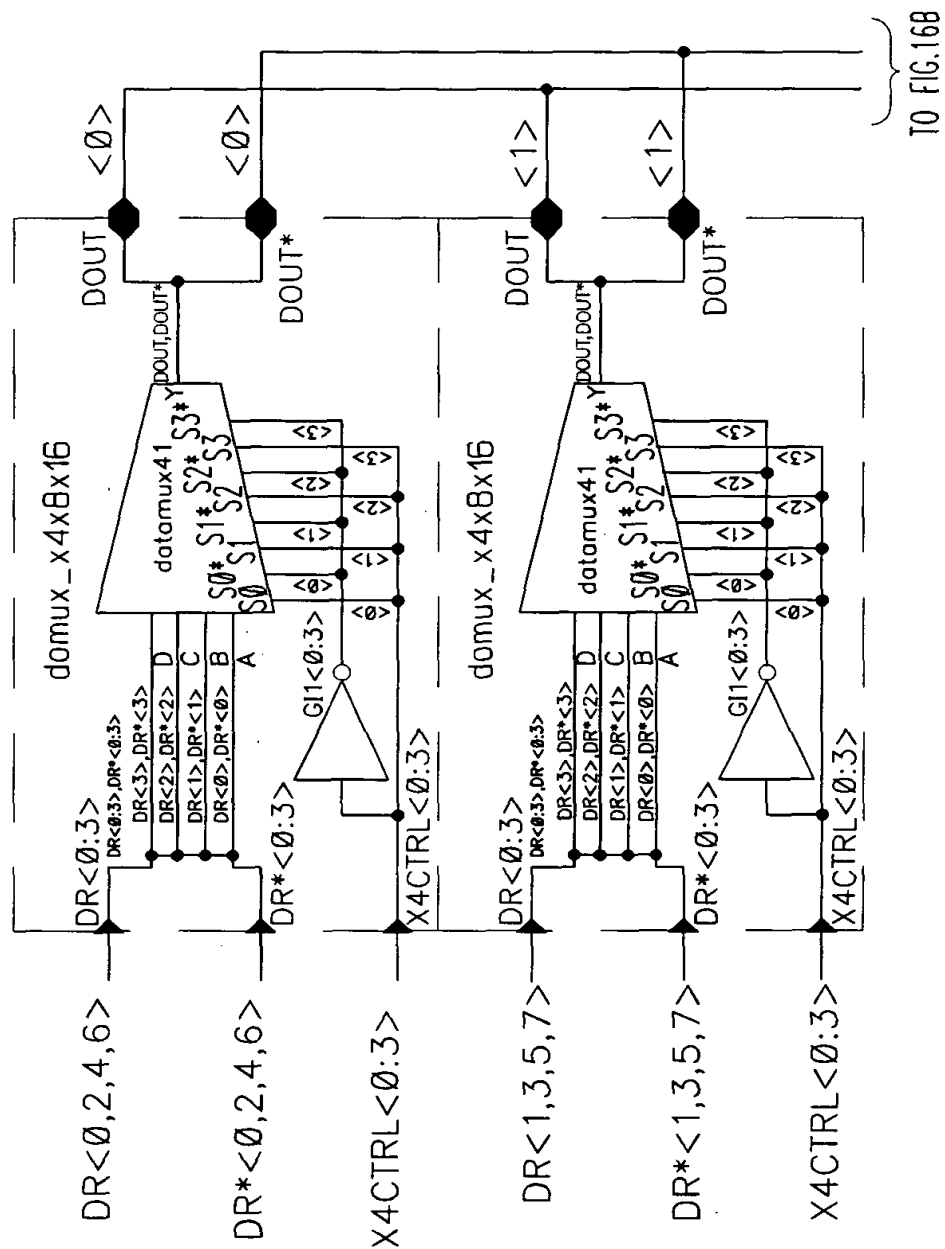


FIG. 16A

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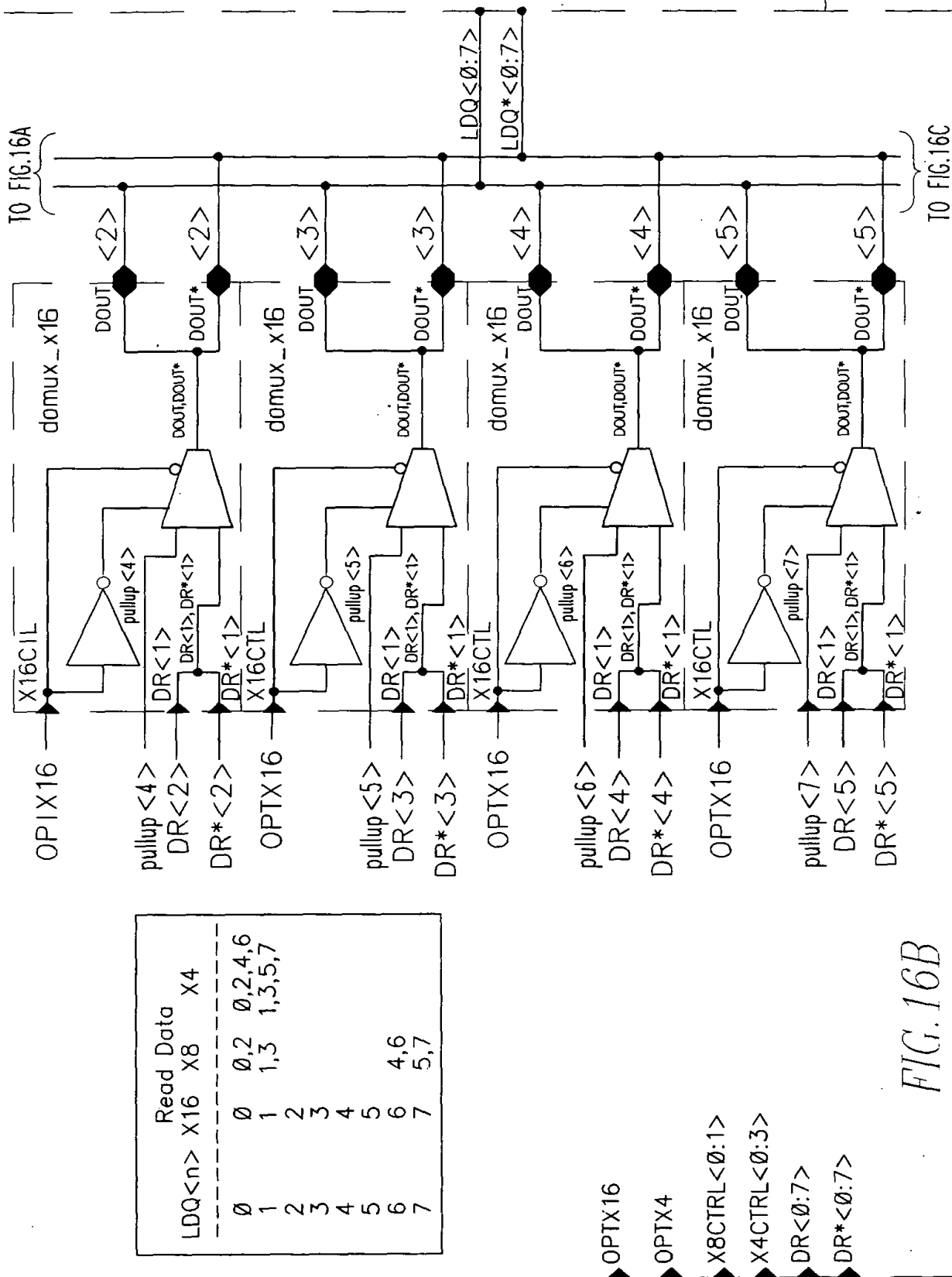


FIG. 16B

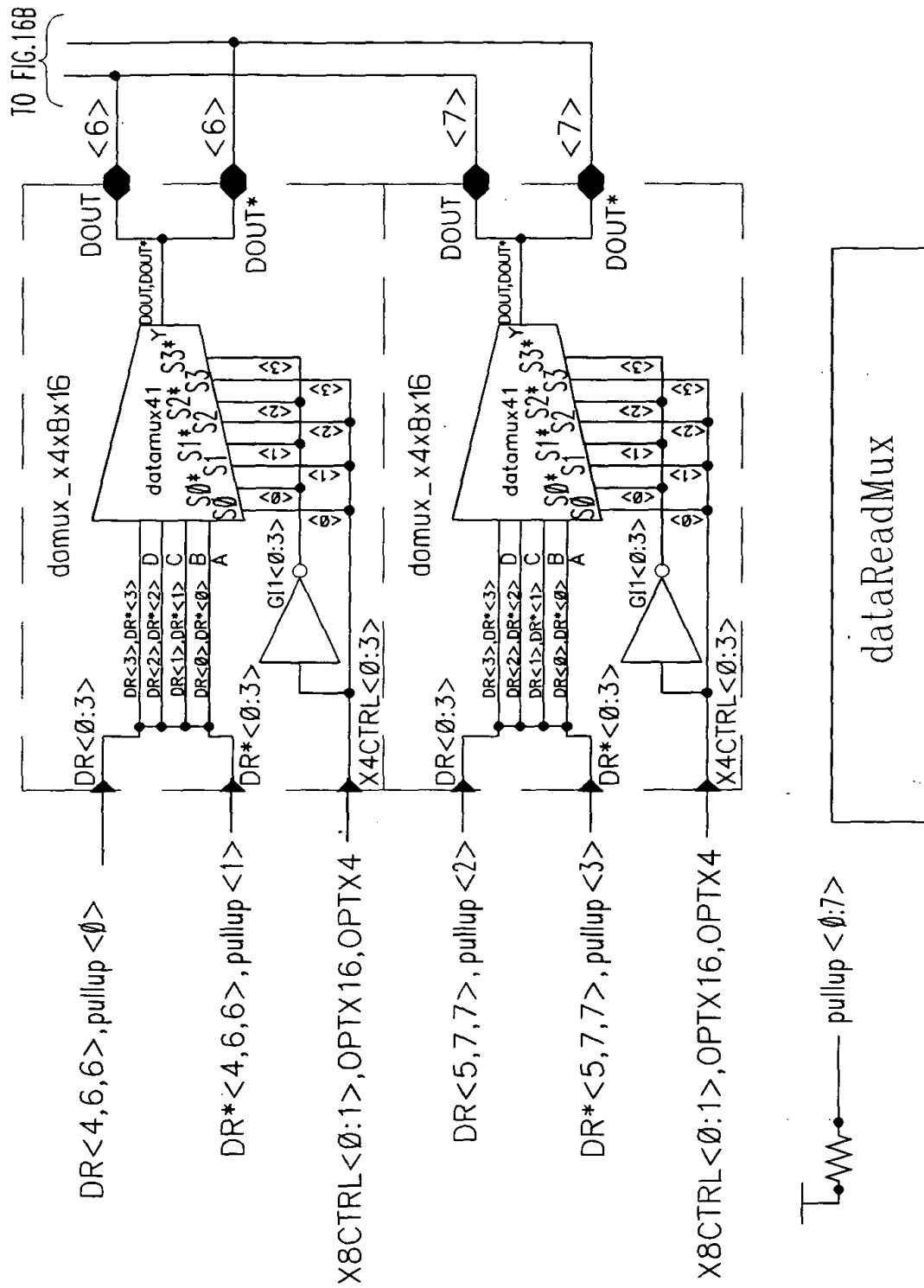
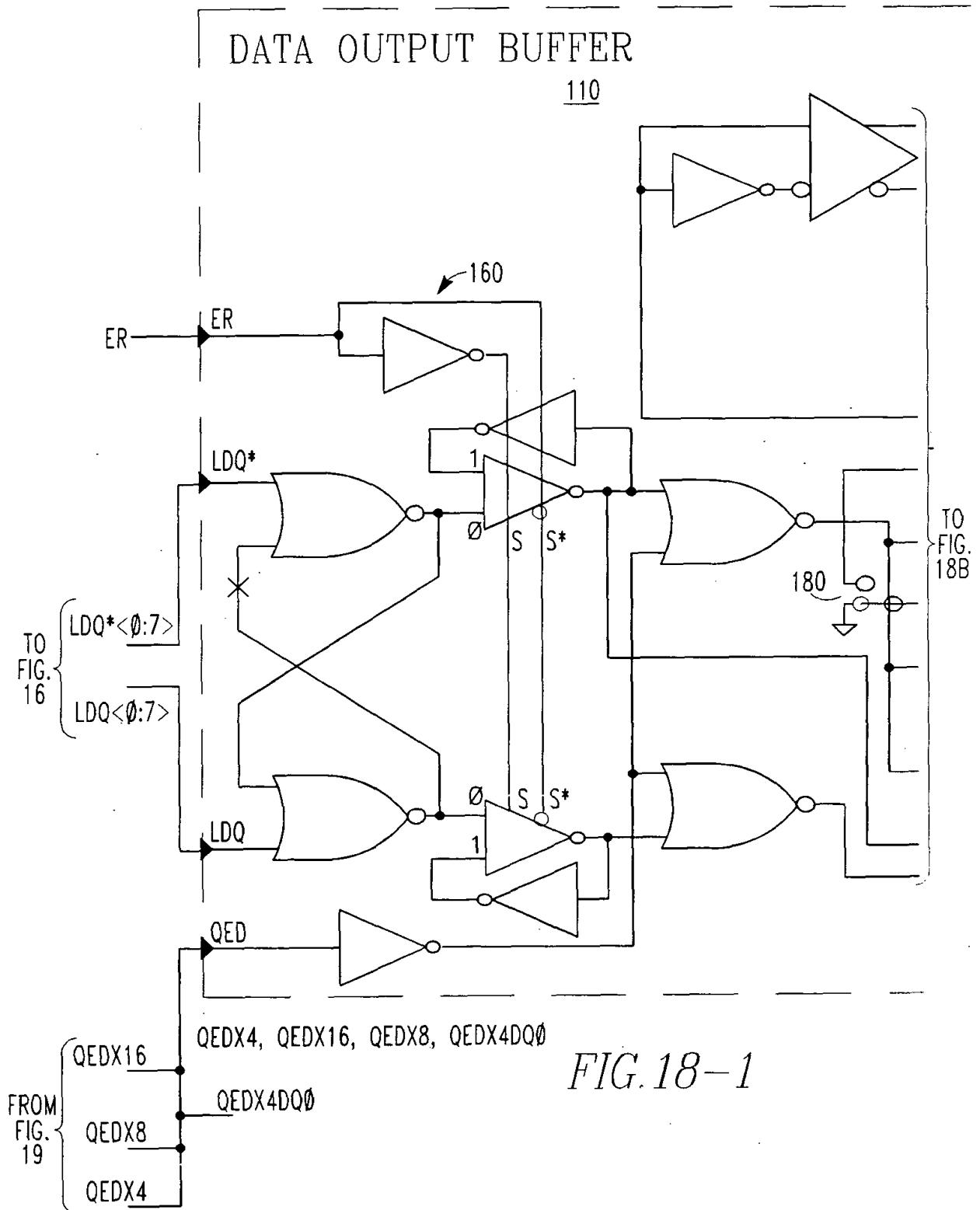


FIG. 16C



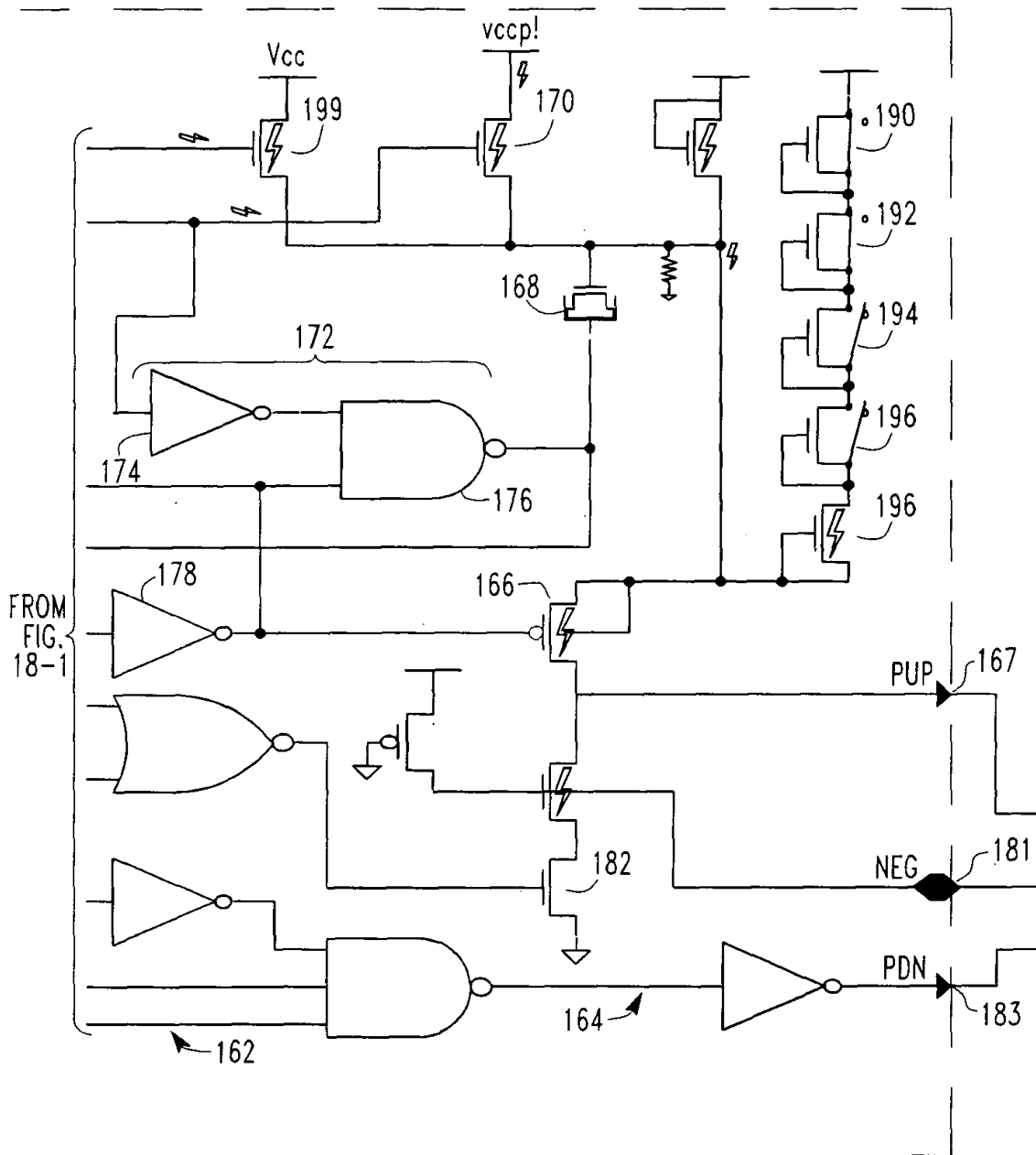


FIG. 18-2

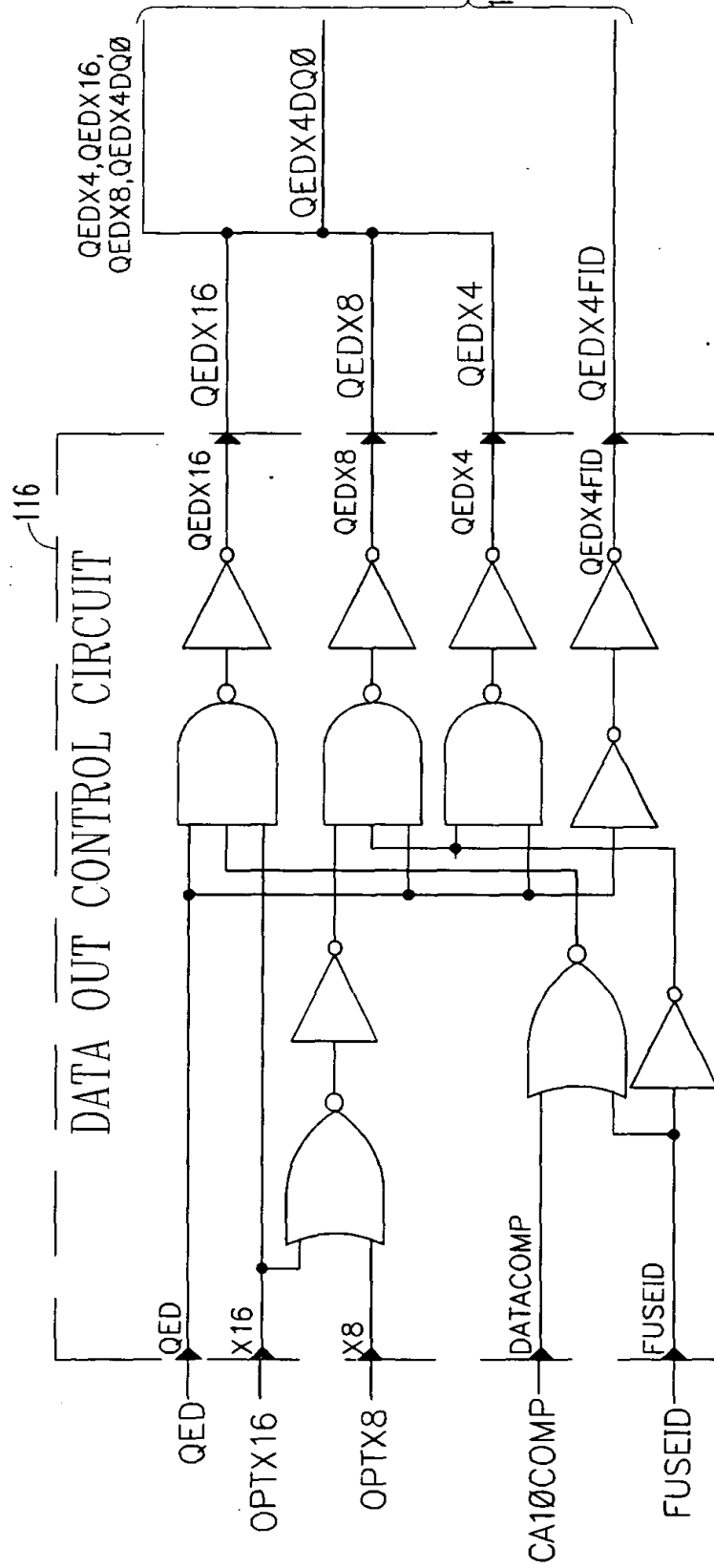


FIG. 19

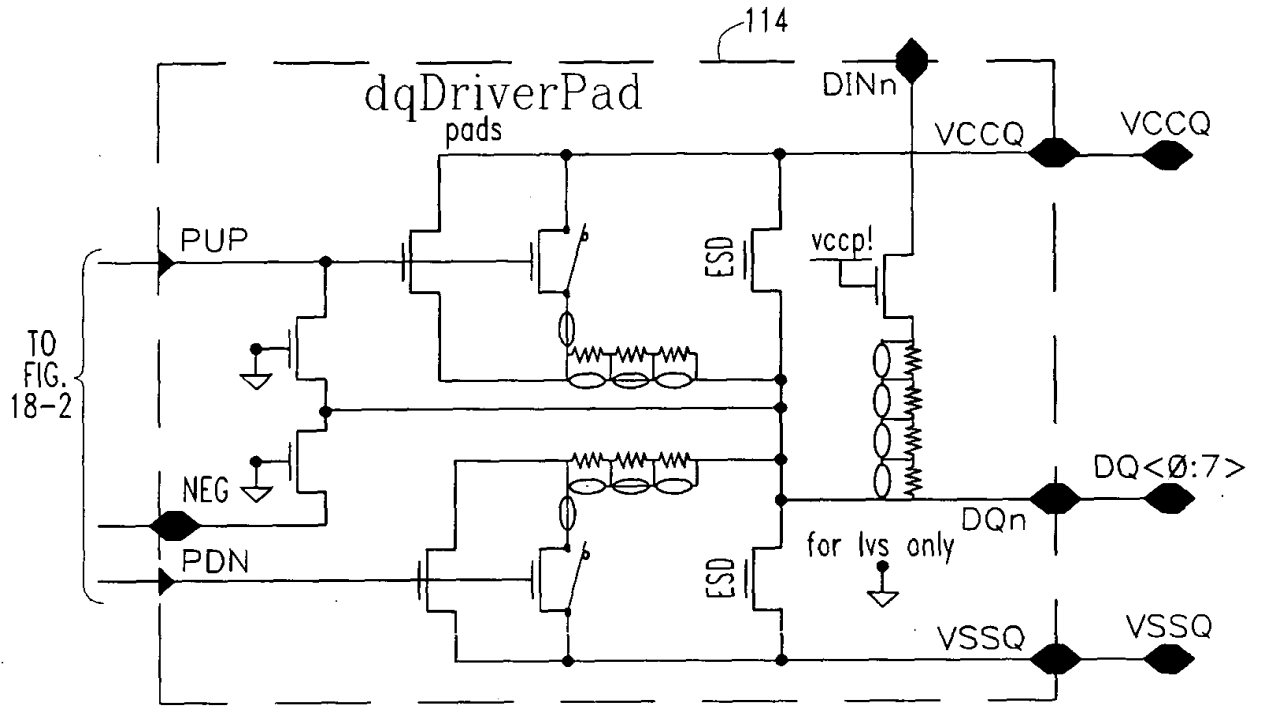


FIG. 20

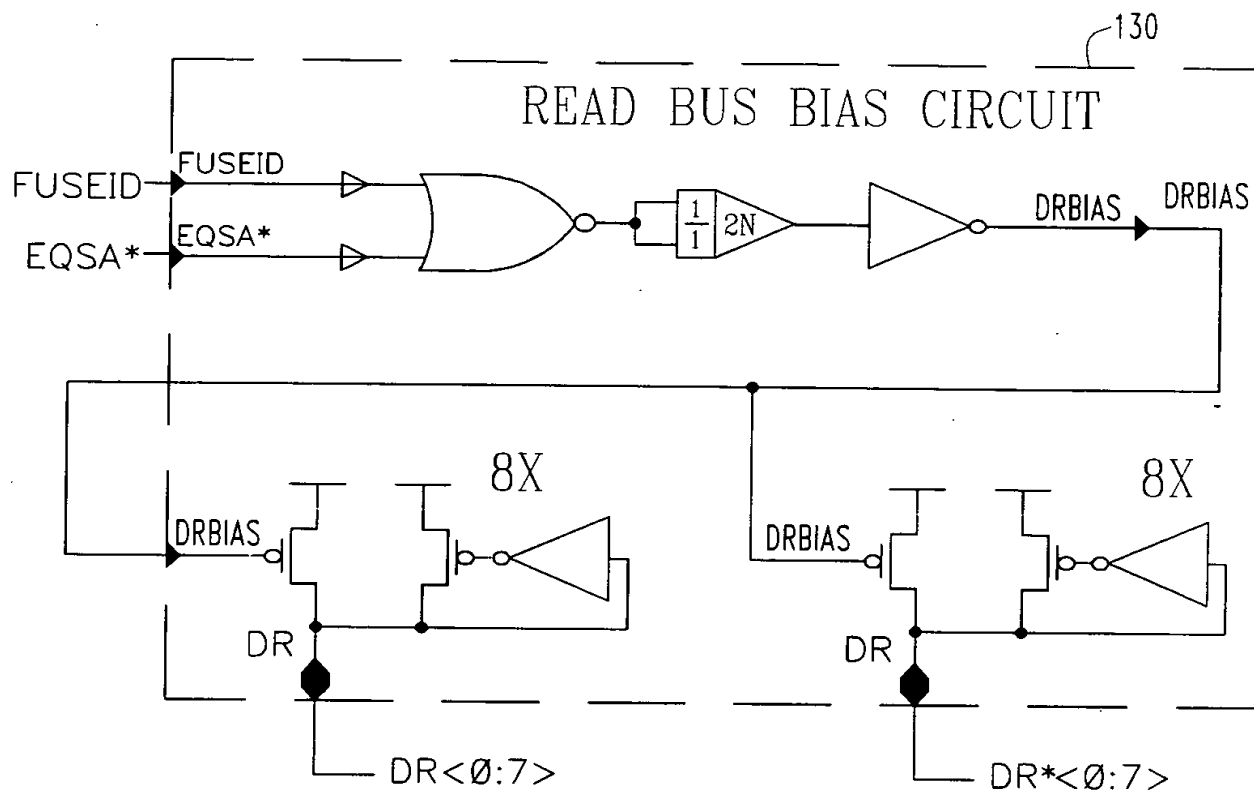
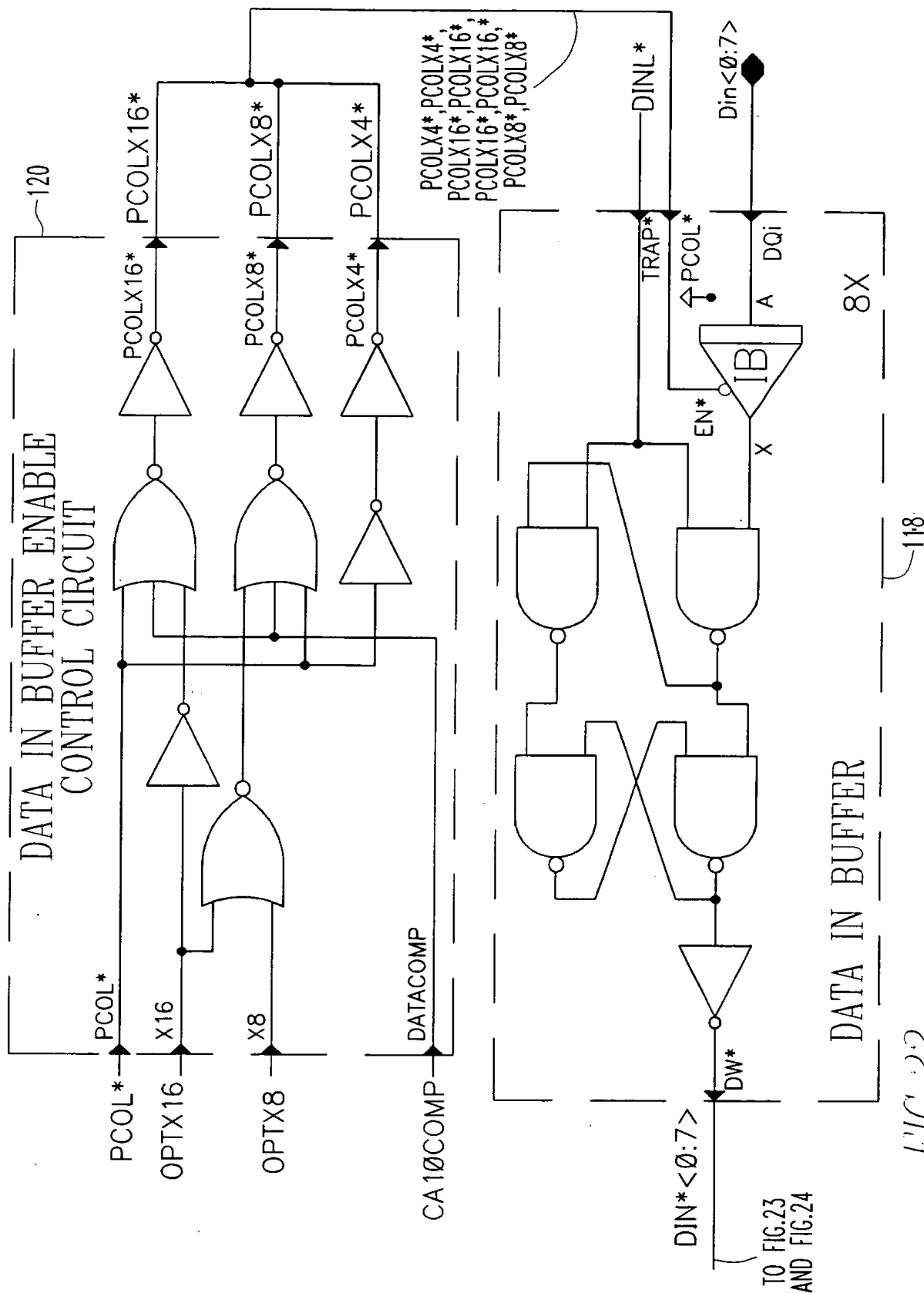


FIG. 21



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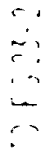


FIG. 23-1

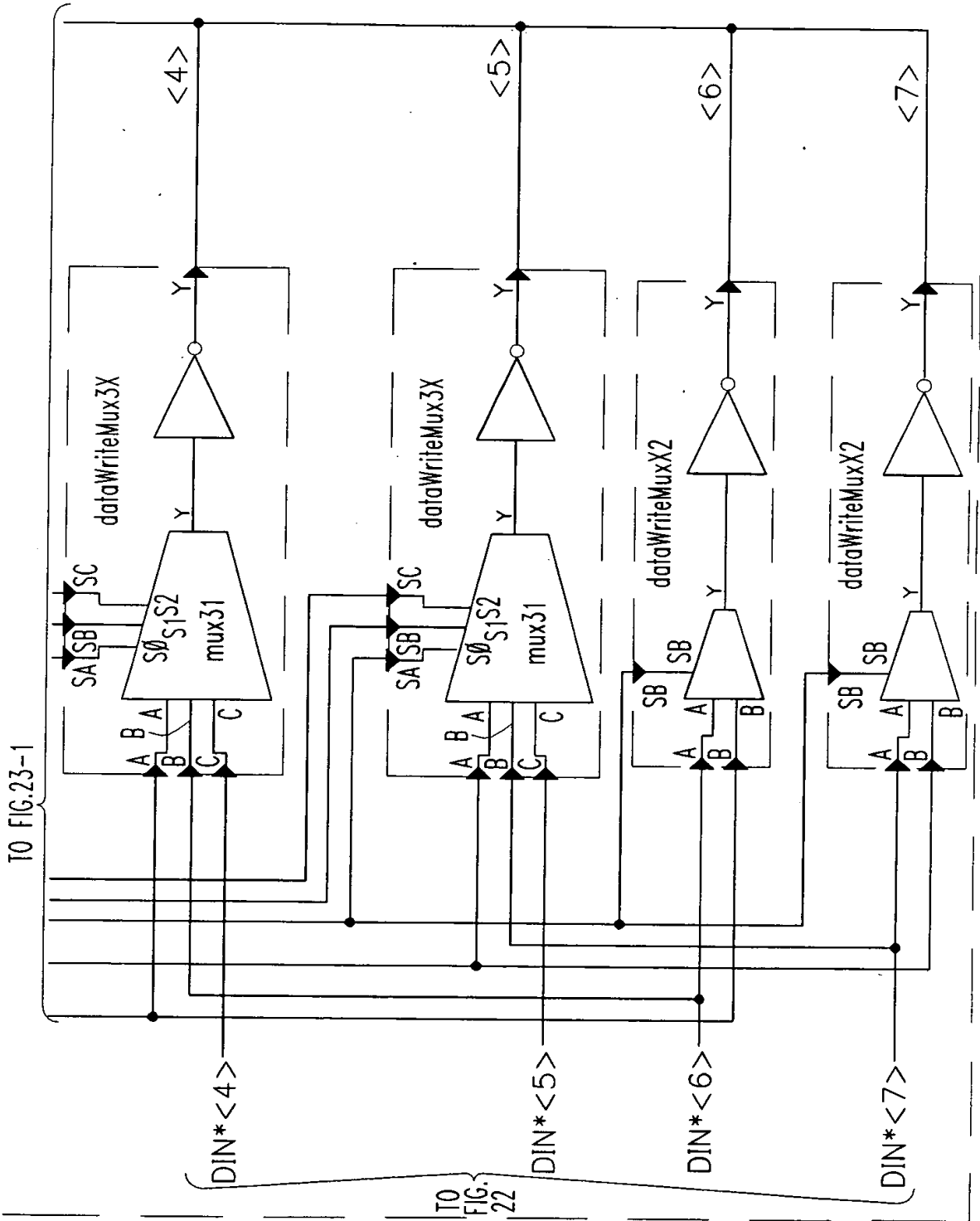


FIG. 23-2

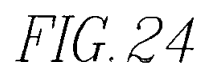


FIG. 24

FIG. 24

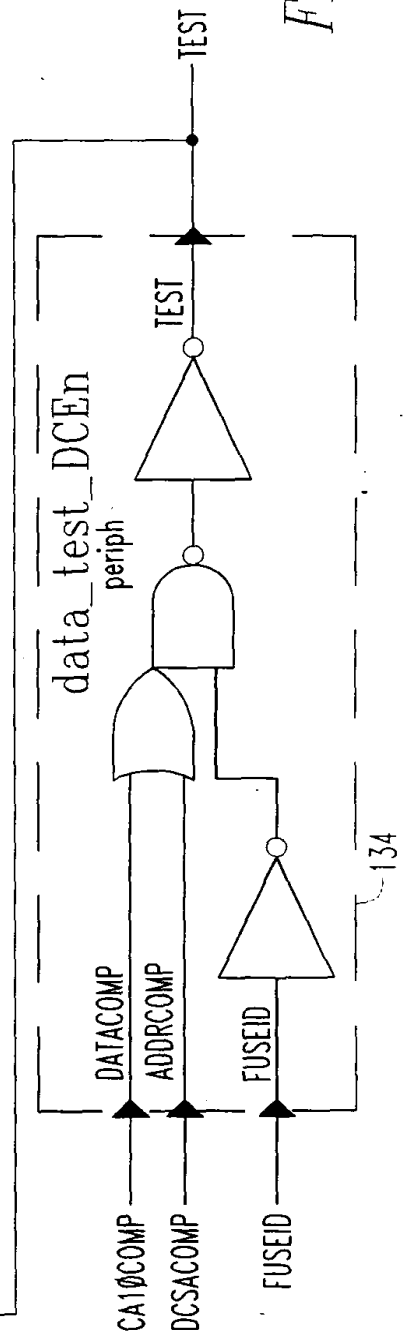
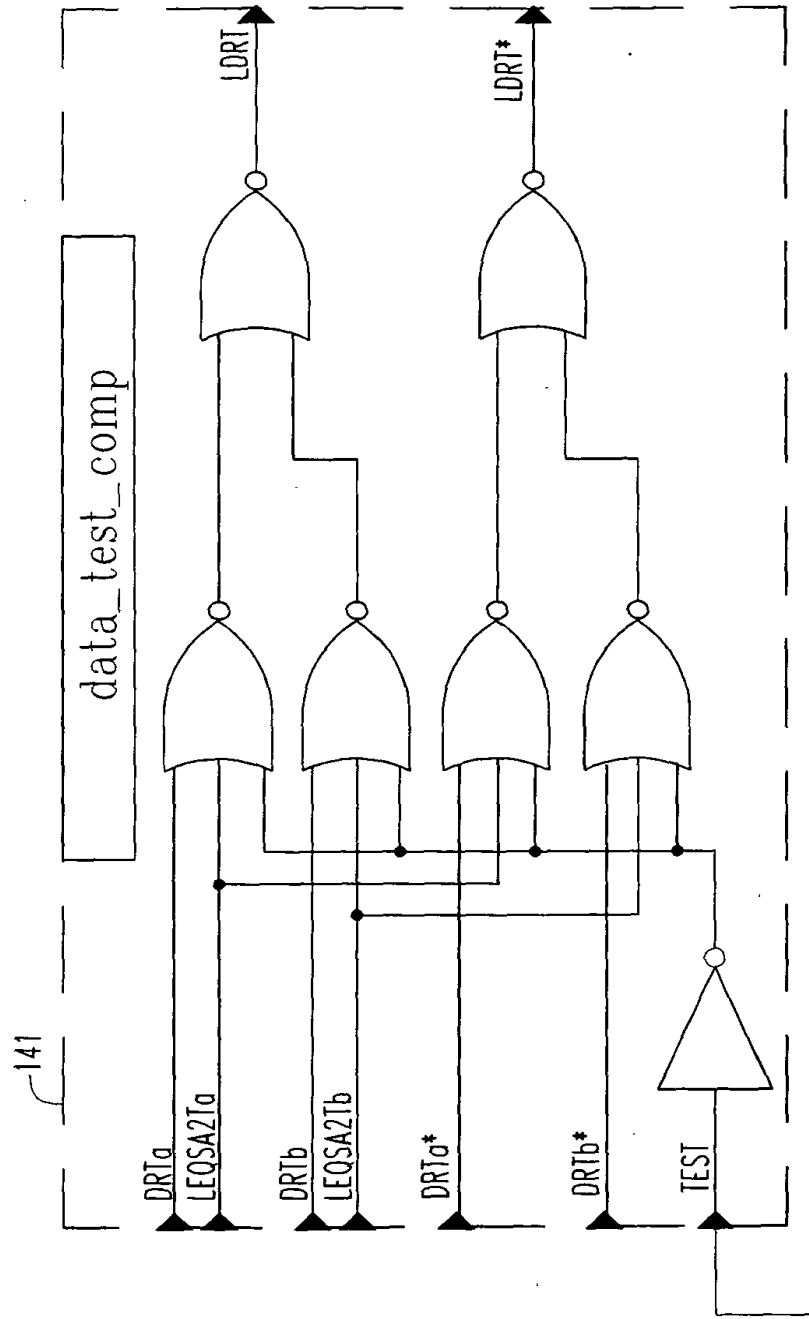
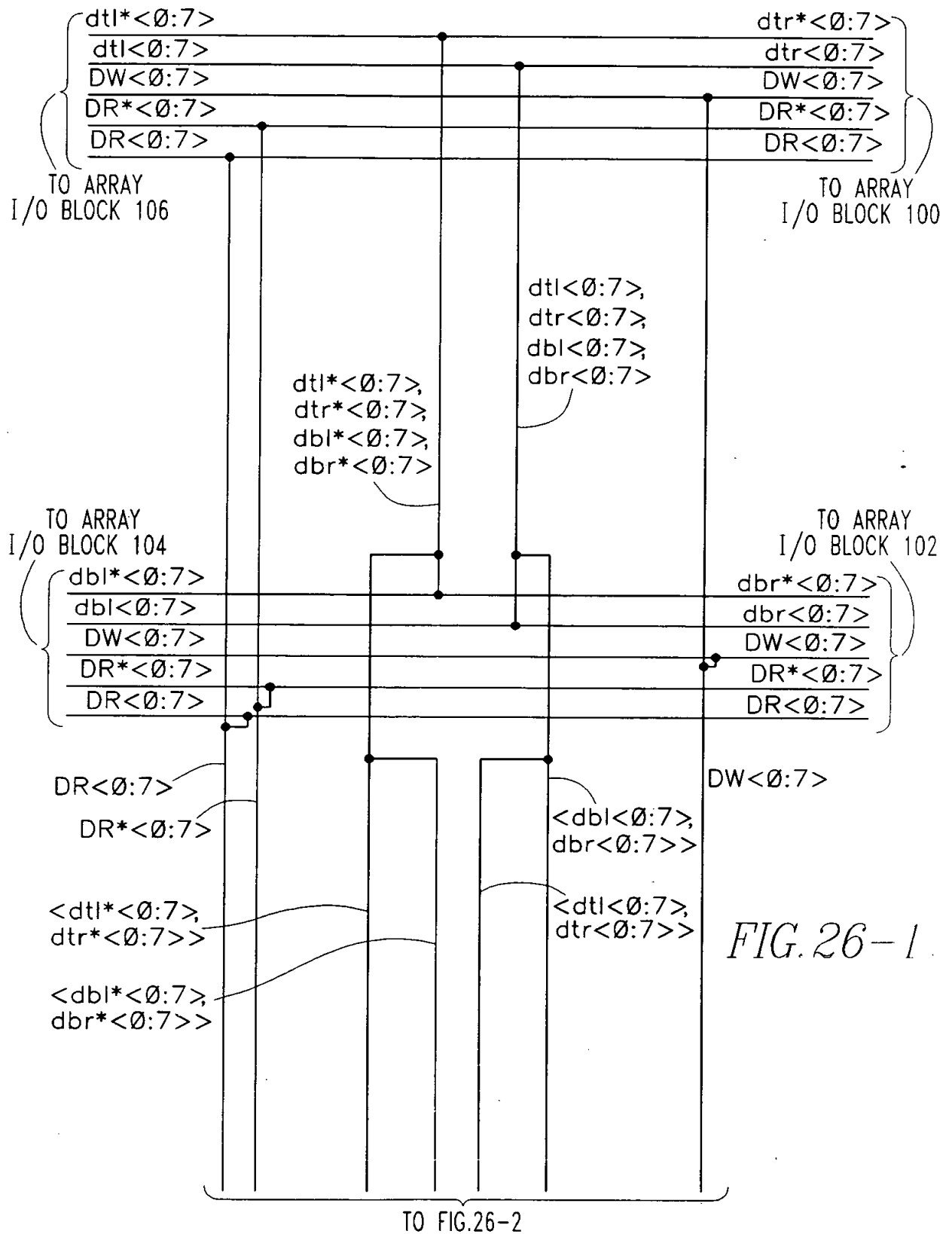


FIG. 25



FROM FIG.26-1

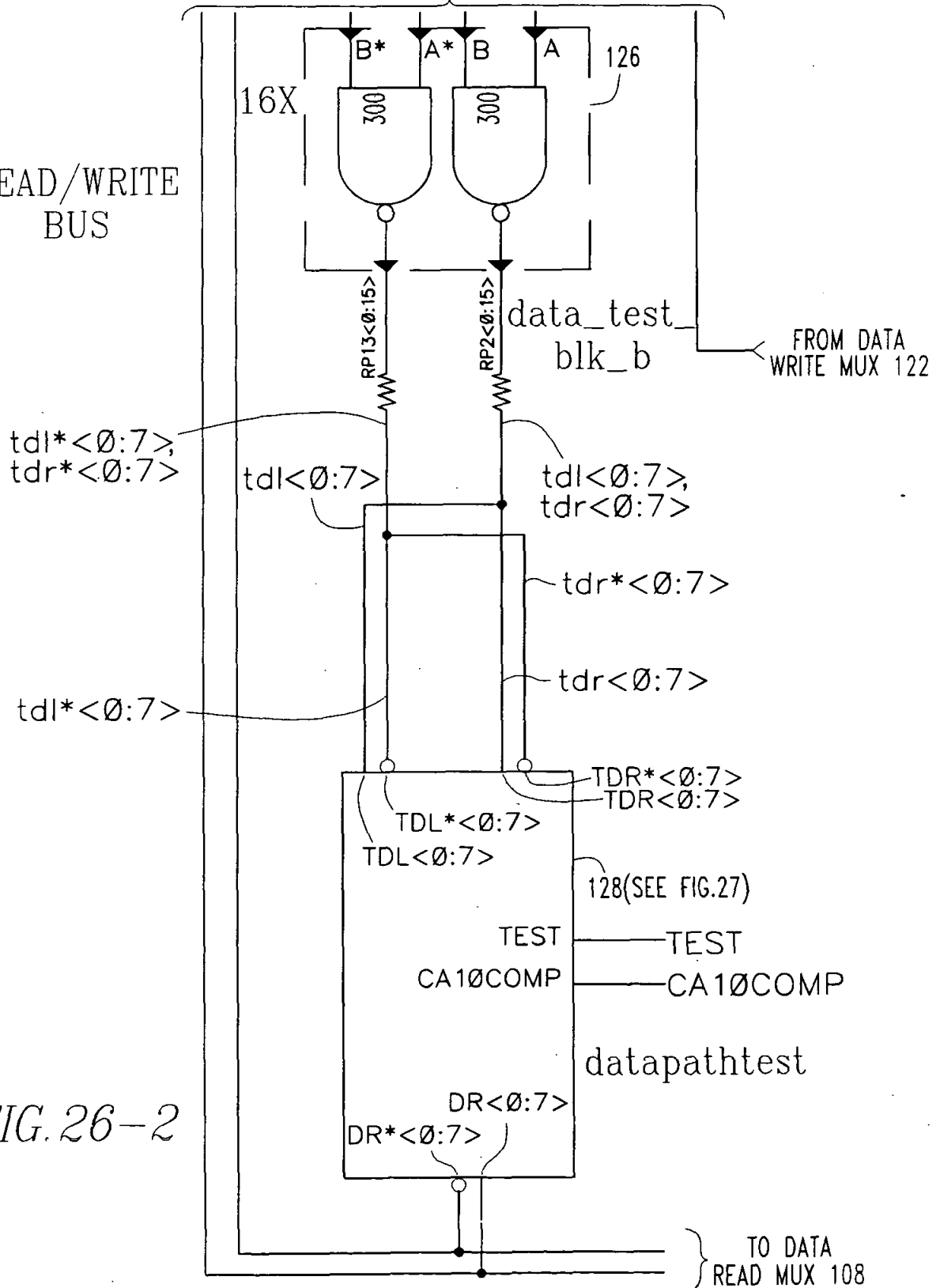
READ/WRITE
BUS

FIG. 26-2

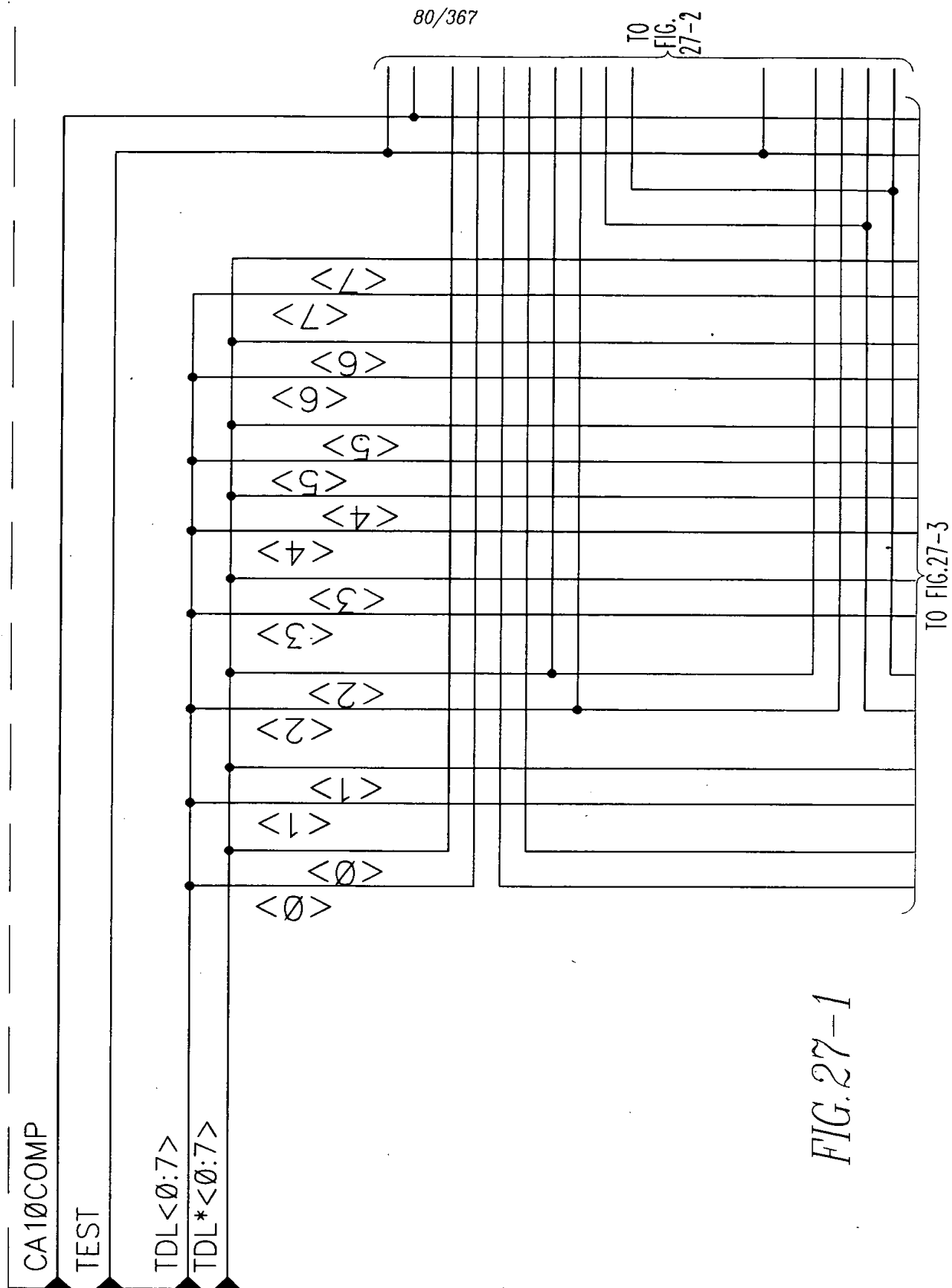


FIG. 27-1

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FIG. 27-2

TO FIG. 27-3

FIG. 27-2

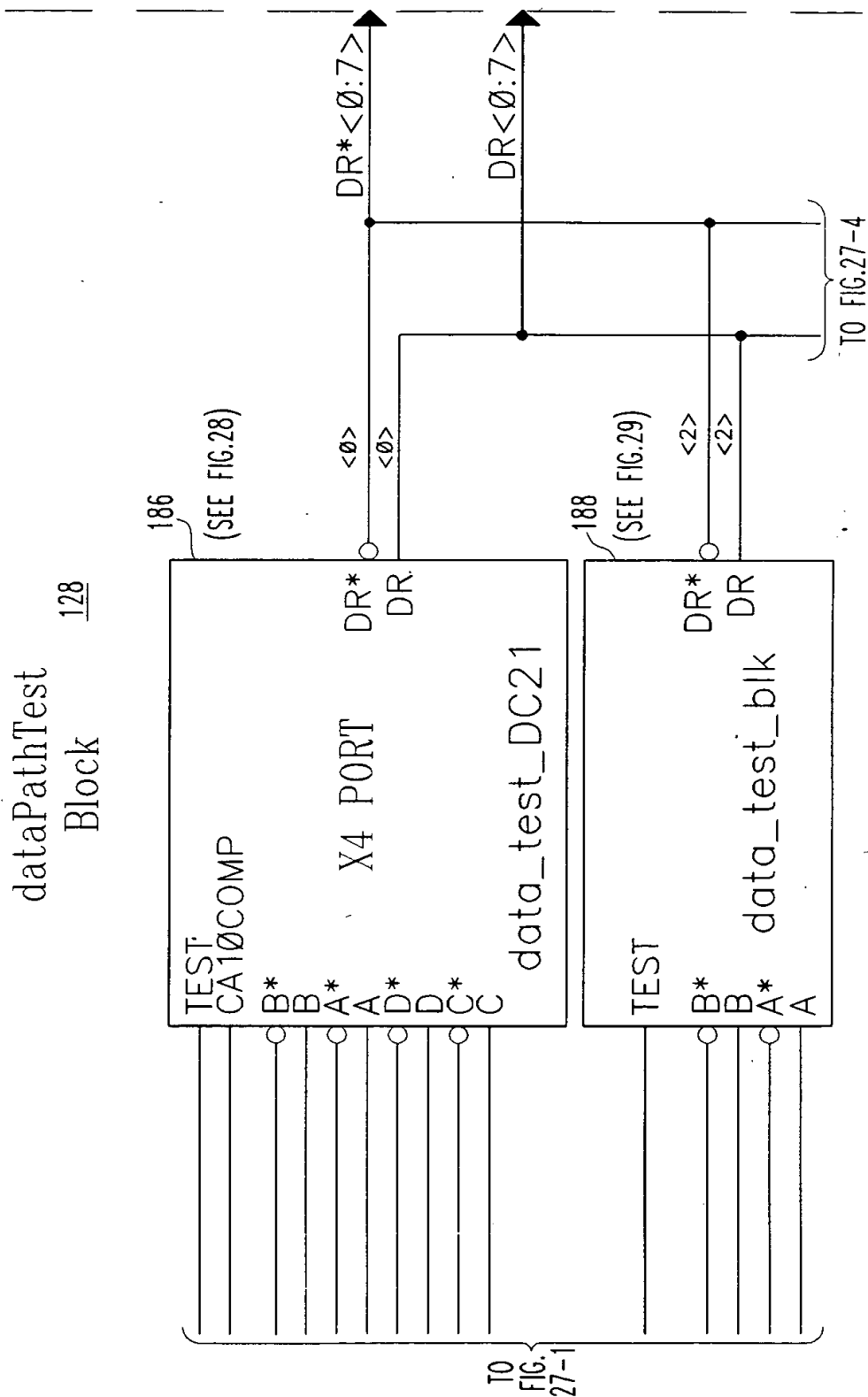
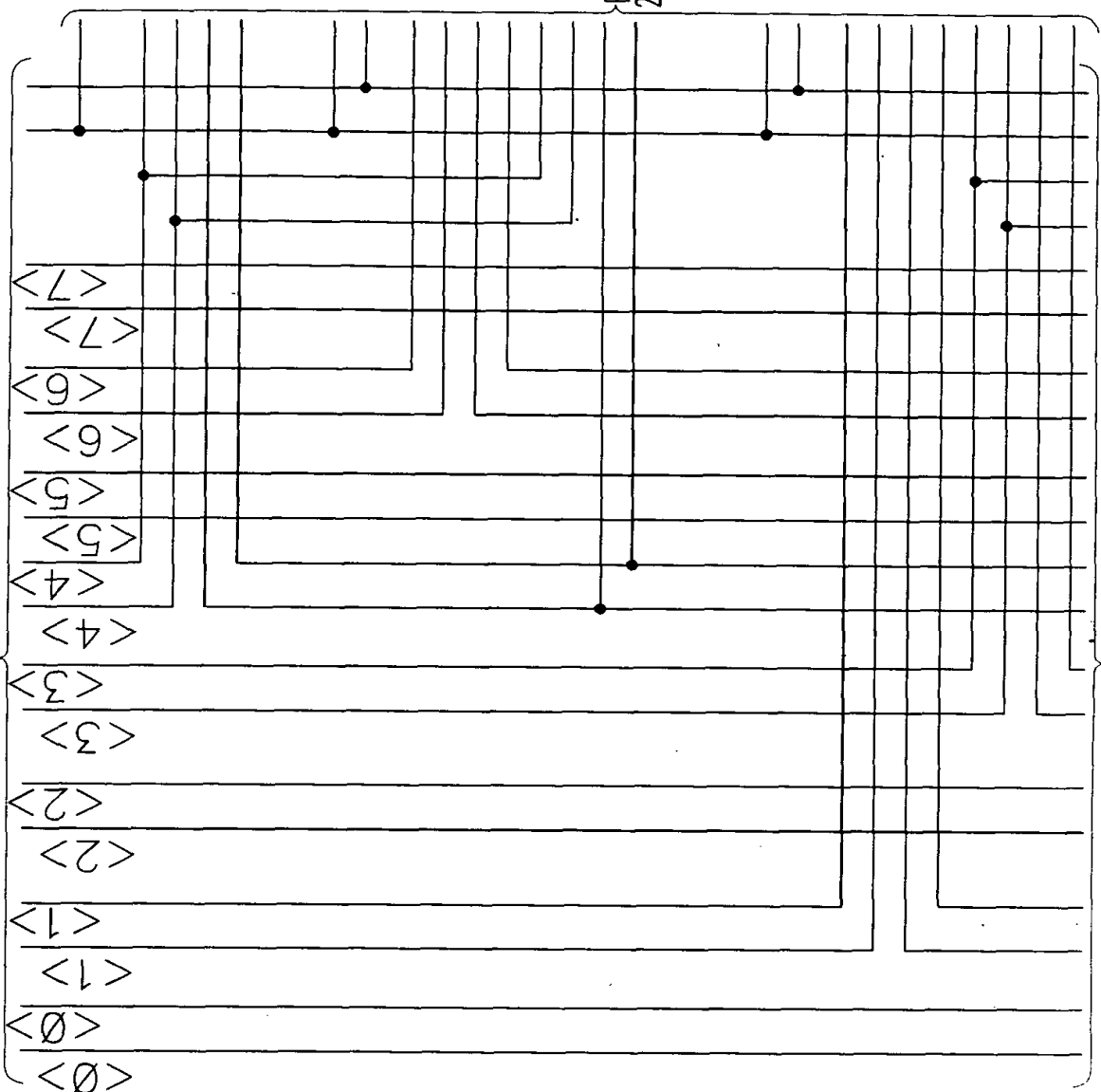


FIG. 27-3

TO FIG. 27-1



TO FIG. 27-5

FIG. 27-3

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TO
FIG.
27-4

FIG. 27-2

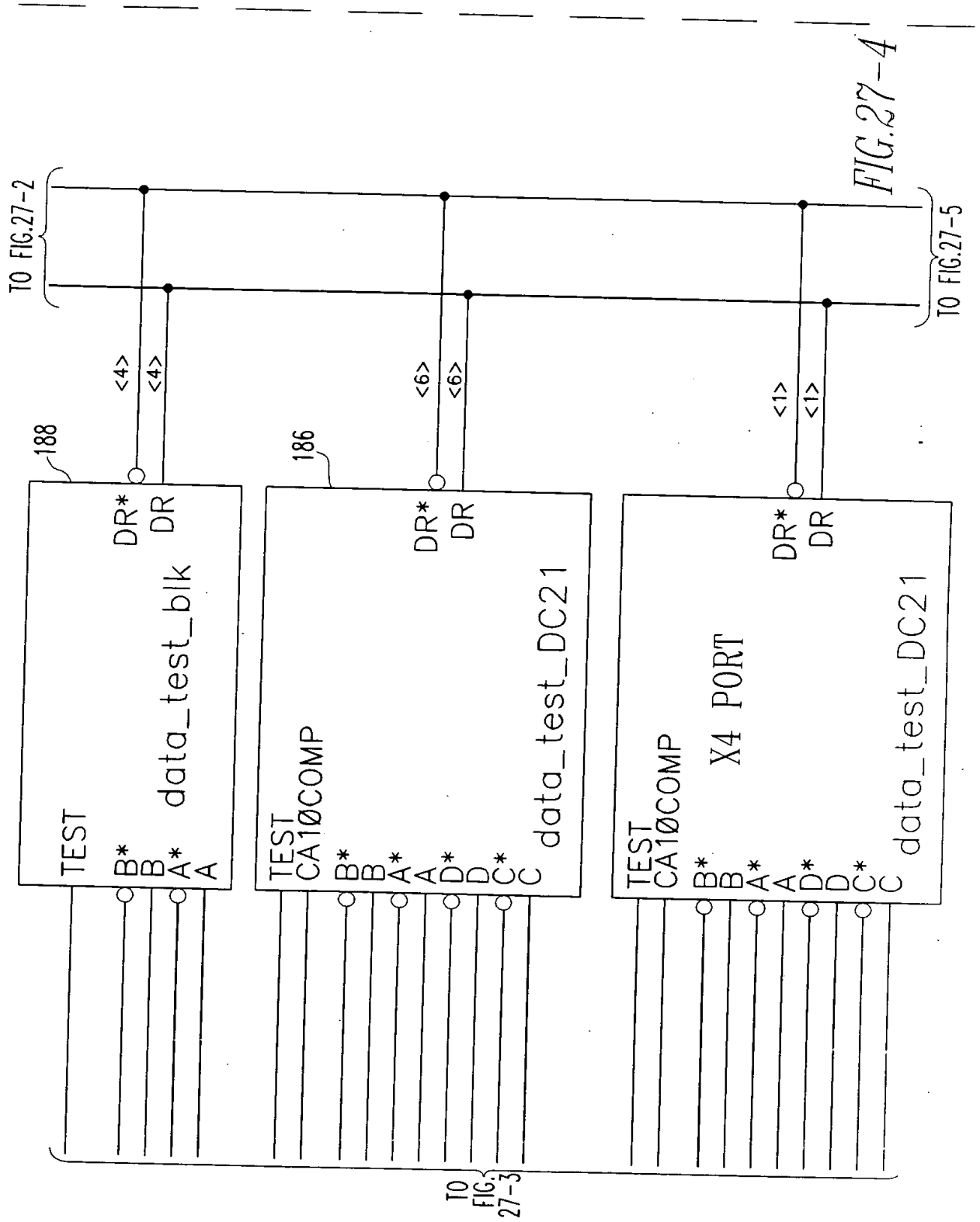
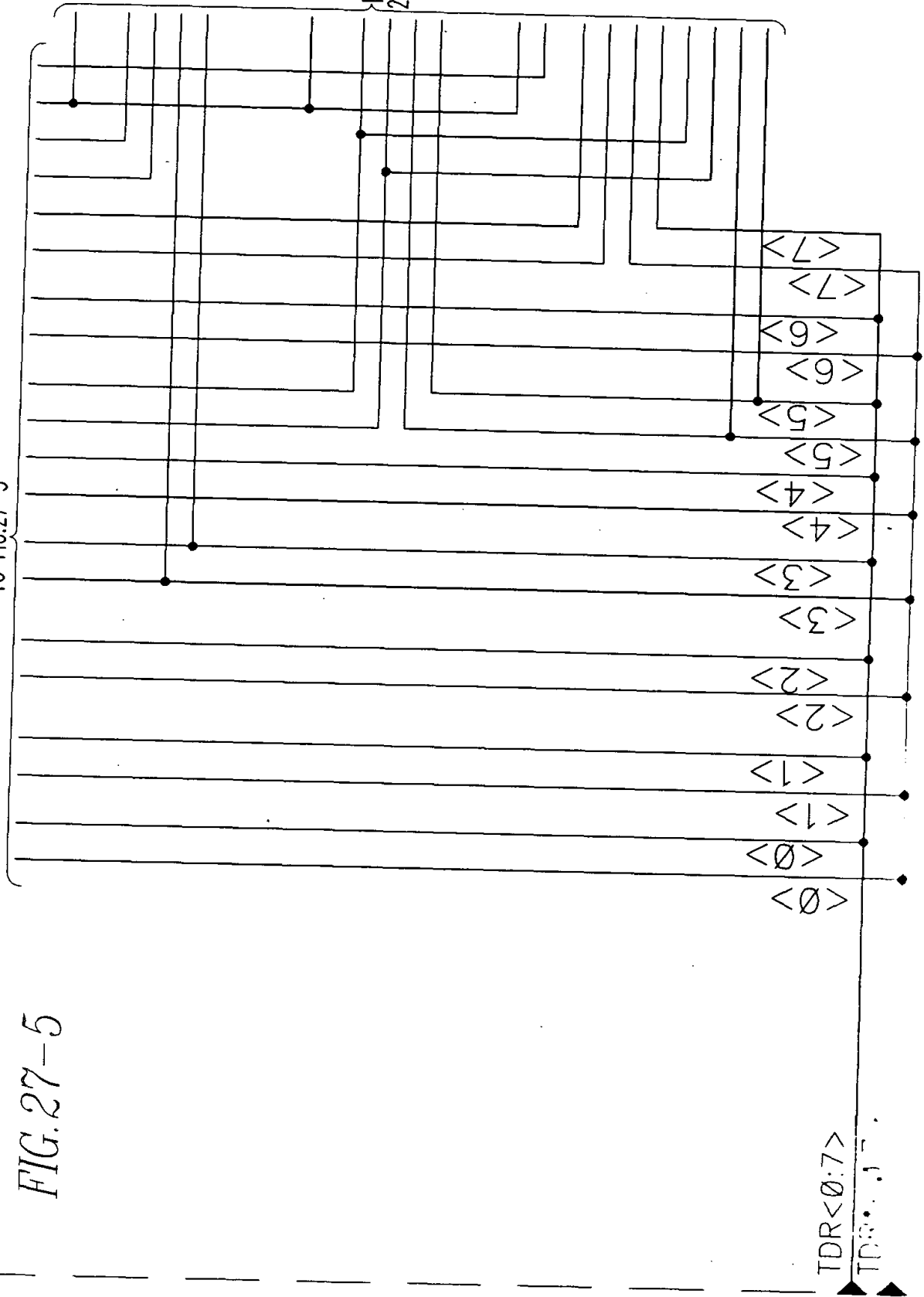
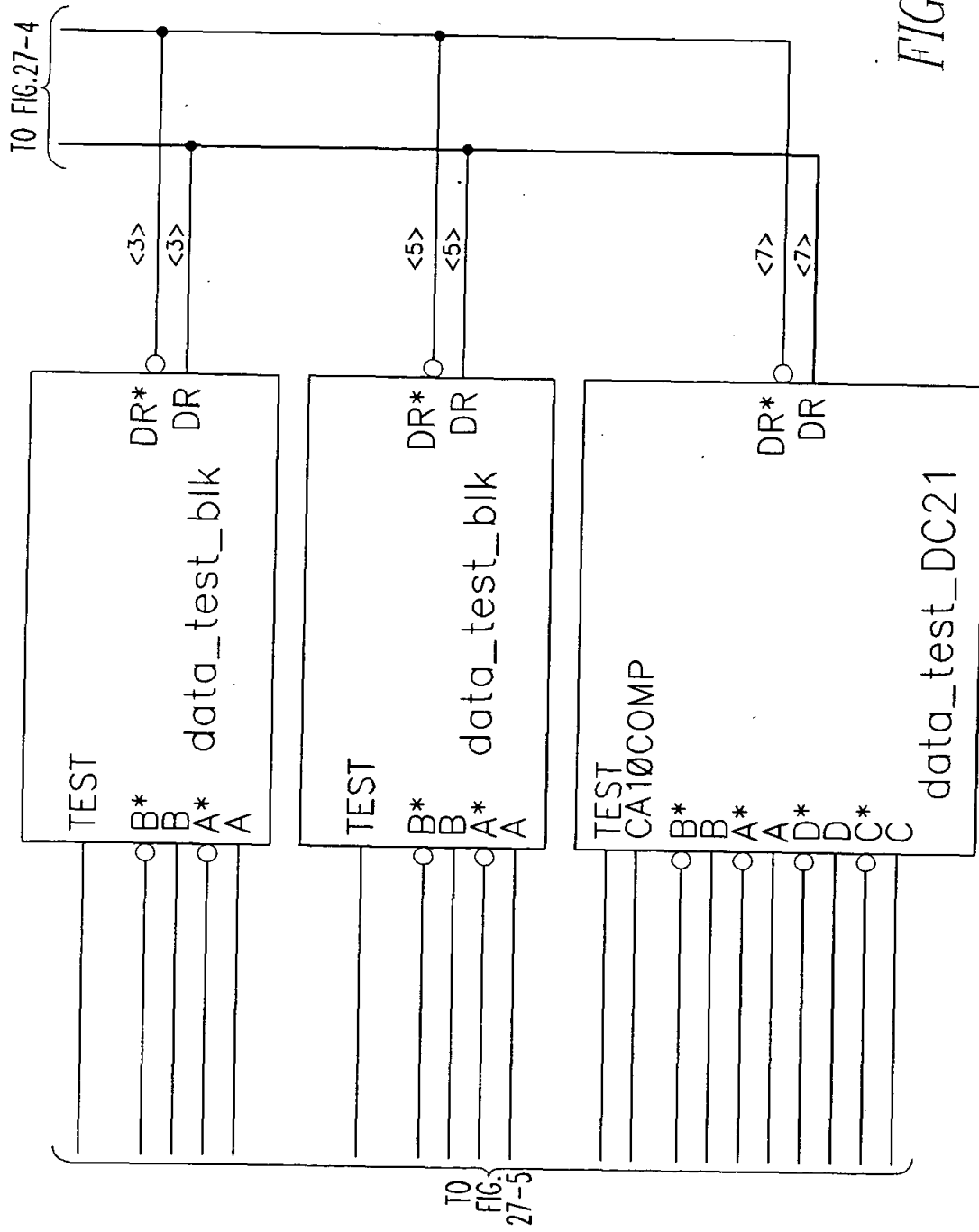


FIG. 27-5

TO FIG. 27-3





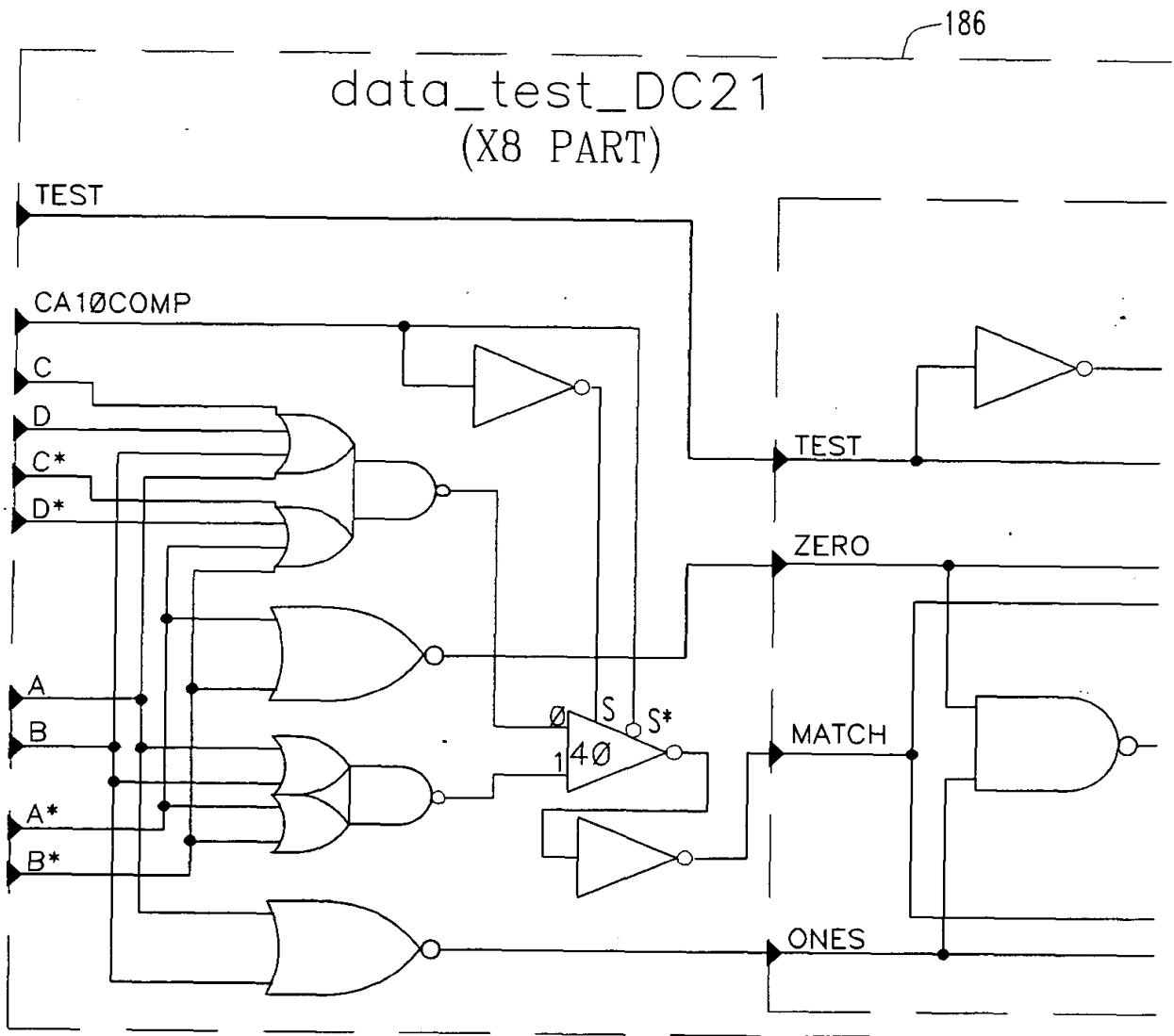


FIG. 28-1

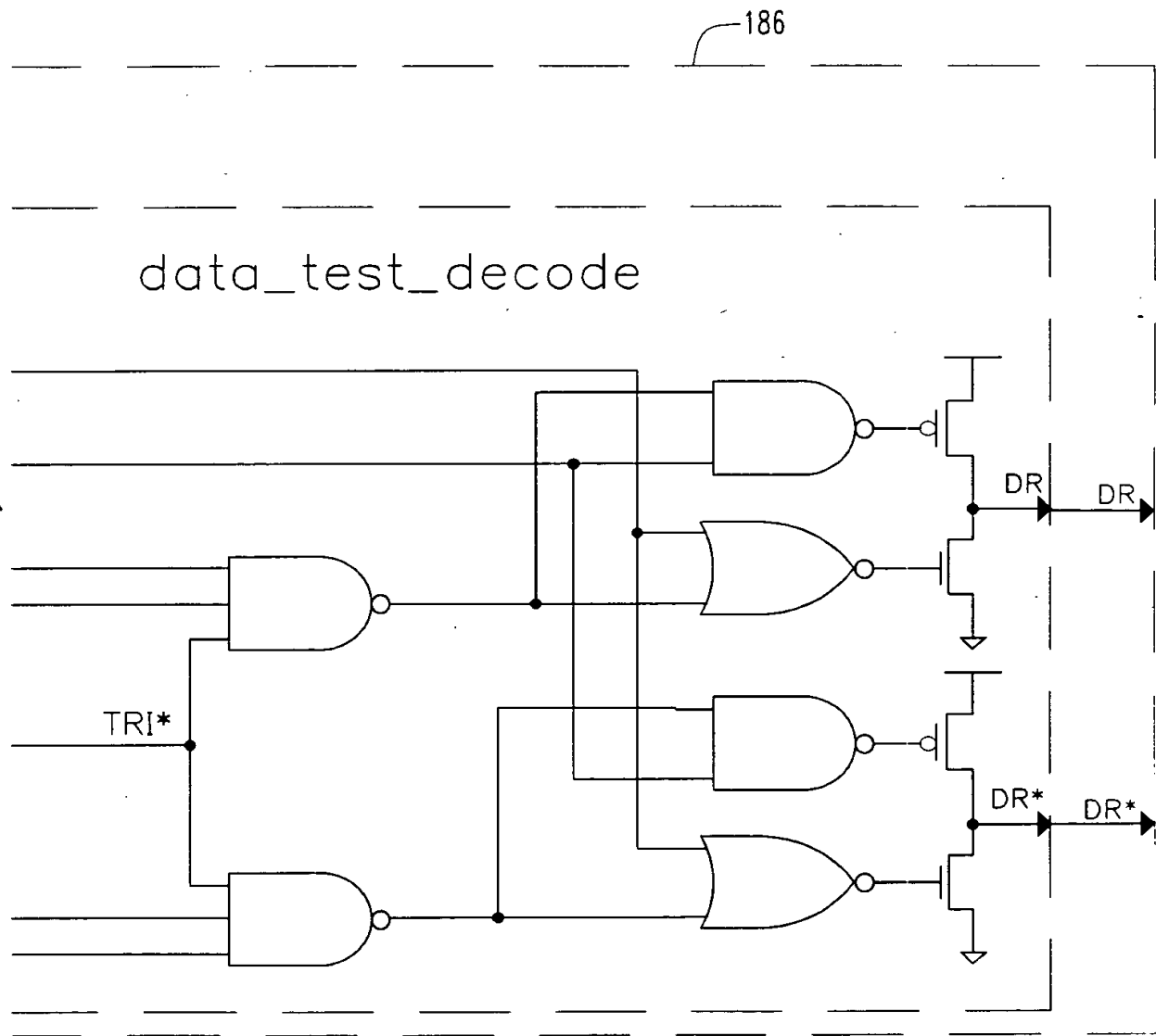


FIG. 28-2

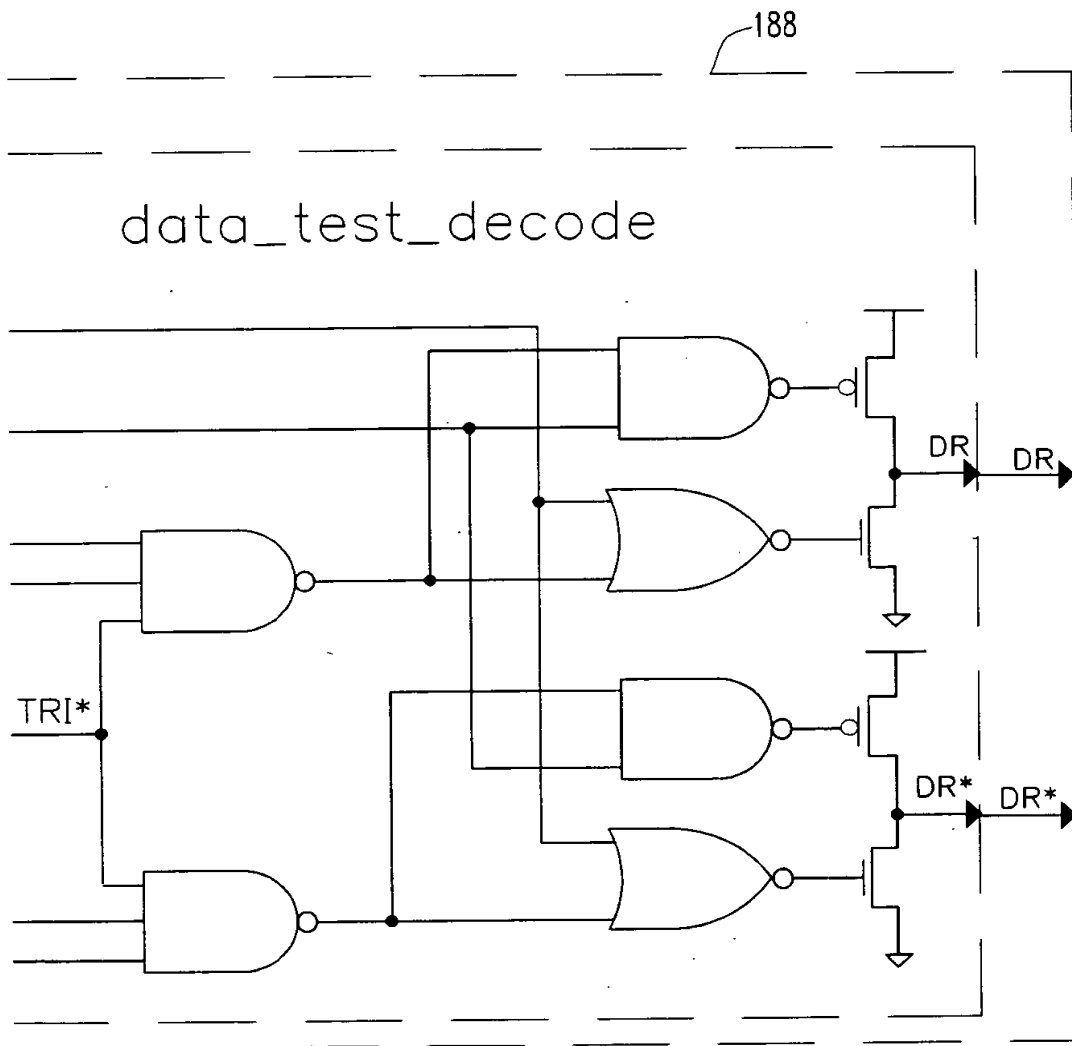
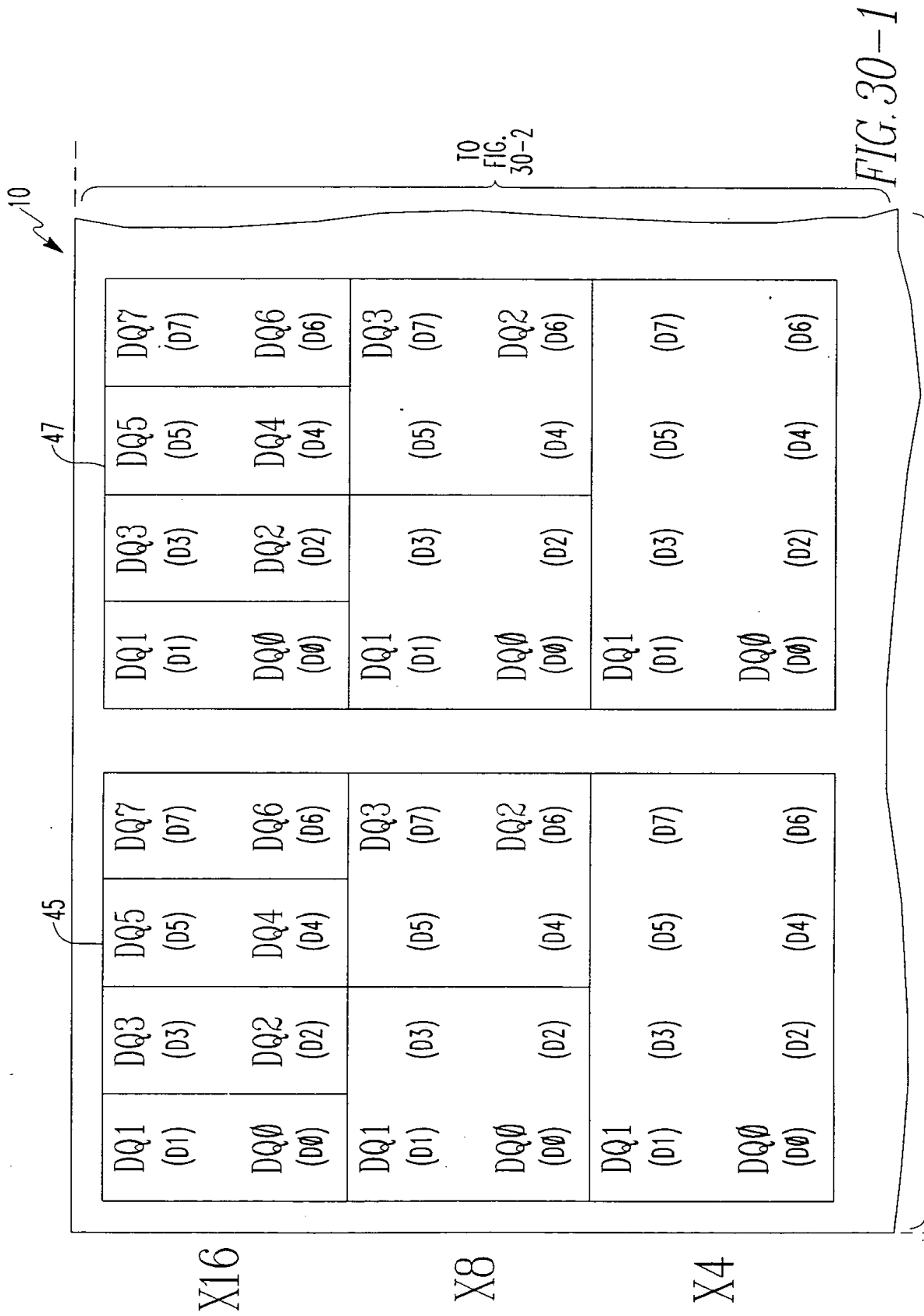


FIG. 29-2



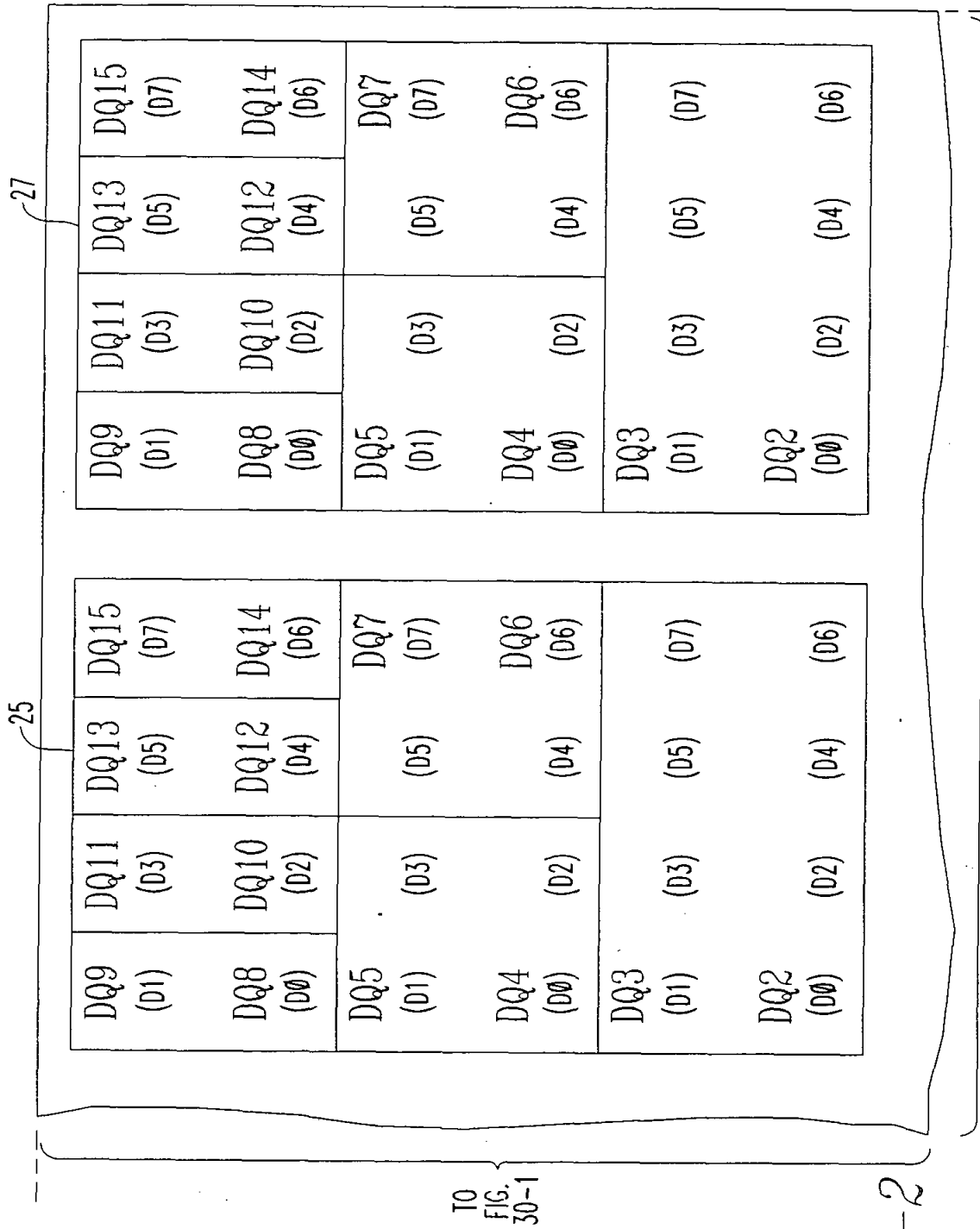


FIG. 30-2

TO FIG. 30-4

TO FIG. 30-1

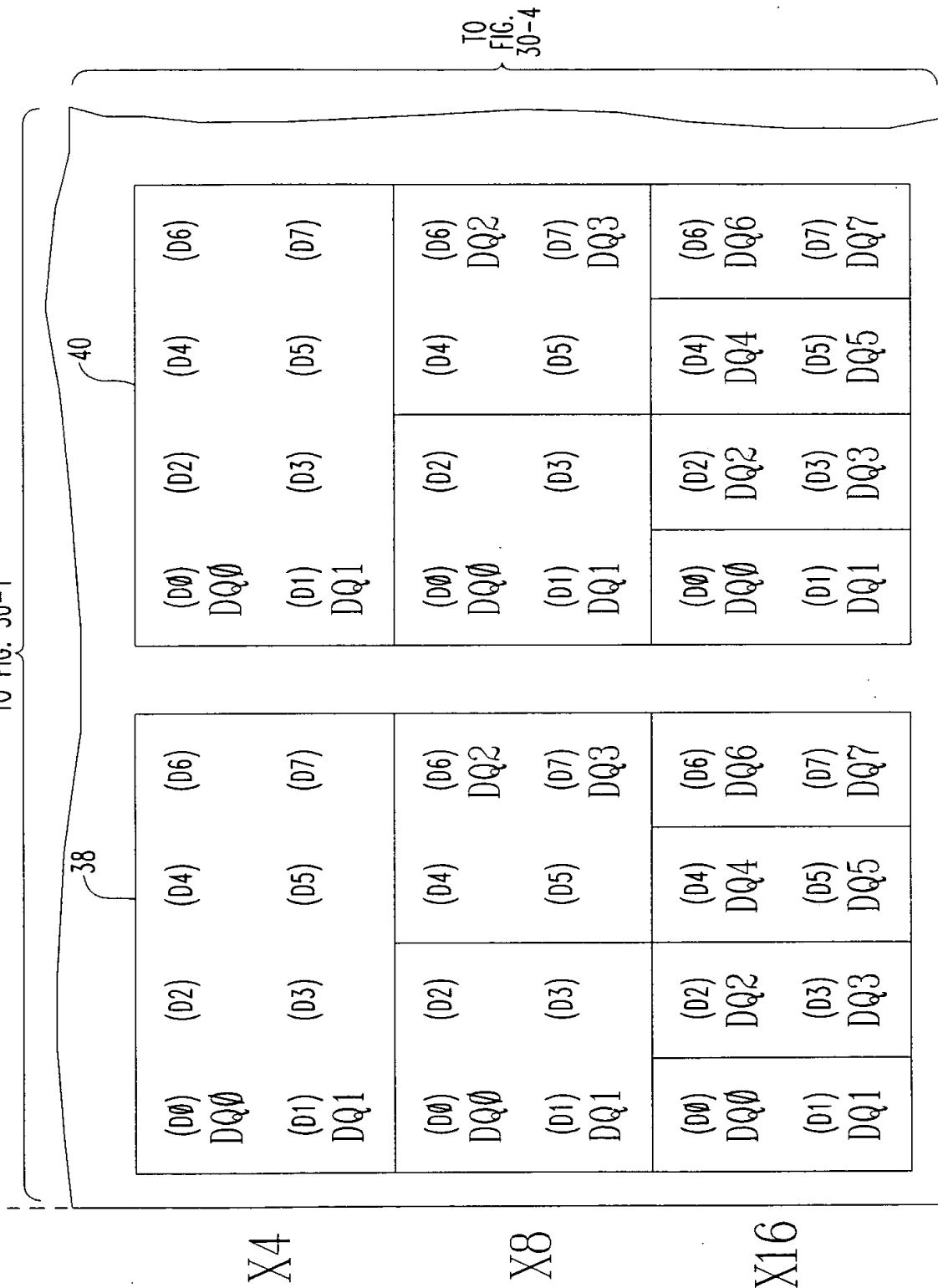


FIG. 30-3

TO FIG. 30-2

		31		33	
		(00) DQ2	(01) DQ3	(02) DQ4	(03) DQ5
		(02) DQ6	(03) DQ7	(04) DQ8	(05) DQ9
		(06) DQ10	(07) DQ11	(08) DQ12	(09) DQ13
		(10) DQ14	(11) DQ15	(12) DQ16	(13) DQ17

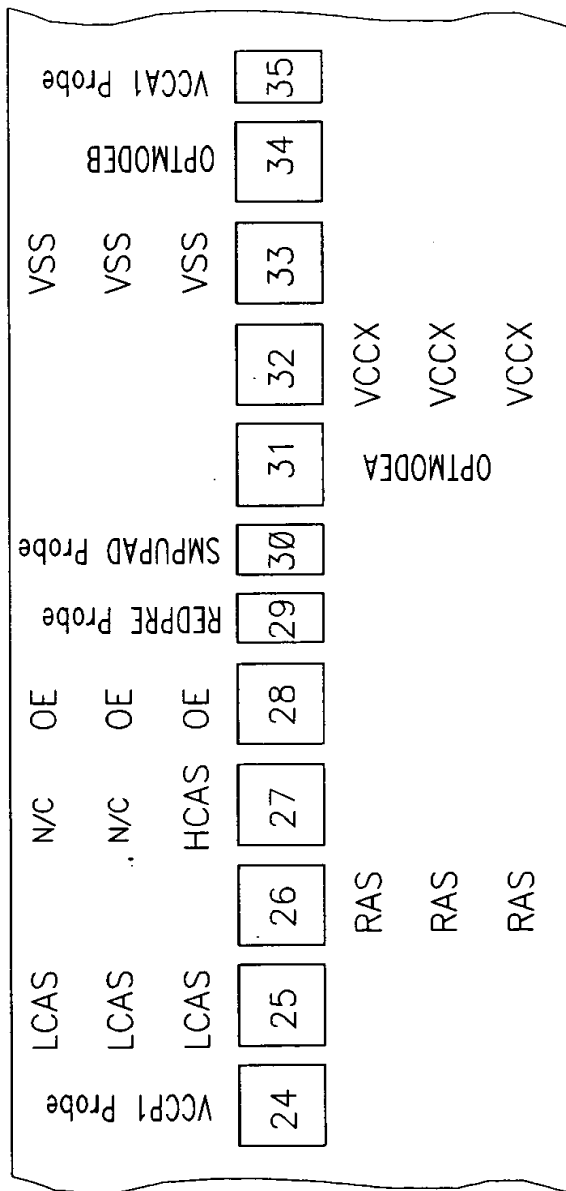
TO
FIG.
30-3

FIG. 30-1

X4	VSSQ	N/C	VSSQ	N/C	N/C						
X8	VSSQ	DQ3	VSSQ	DQ2	N/C						
X16	VSSQ	DQ7	VSSQ	DQ6	DQ5						
	1	2	3	4	5	6	7	8	9	10	11
X16	VCCQ	DQ0	VCCQ	DQ1	DQ2	VCCQ					
X8	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C					
X4	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C					

TO FIG. 31A2

FIG. 31A1



TO FIG. 31B2

FIG. 31B1

TO FIG. 31B1
→

A13	A12	A11	A10	A9
A13	A12	A11	A10	A9
A13	A12	A11	A10	A9
36	37	38	39	40
41	42	43	44	45
46				
A0	A1	A2	A3	A4
A0	A1	A2	A3	A4
A0	A1	A2	A3	A4
				A5
				A5
				A5

FIG. 31B2

TO FIG. 31C2

FIG. 31C1

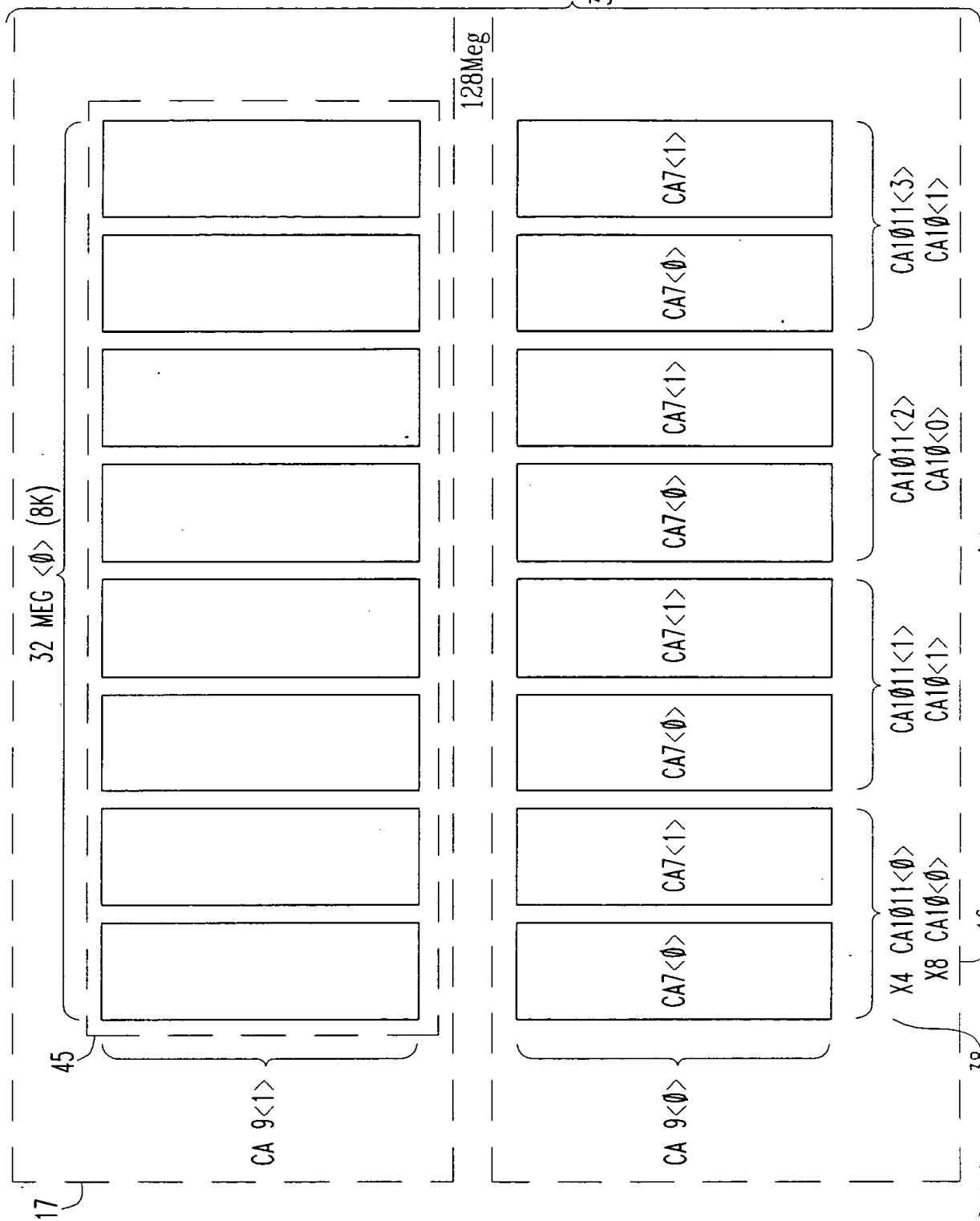
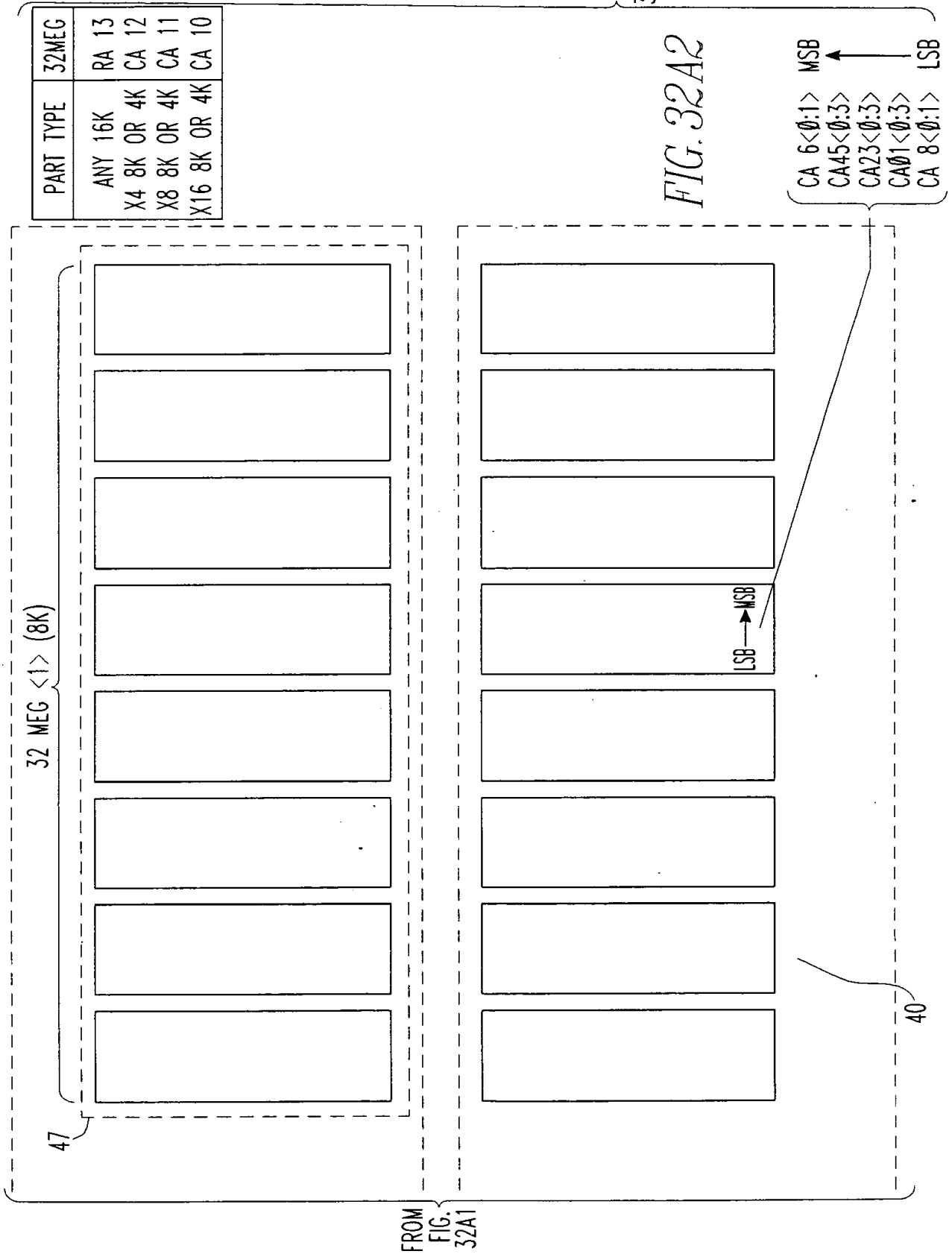
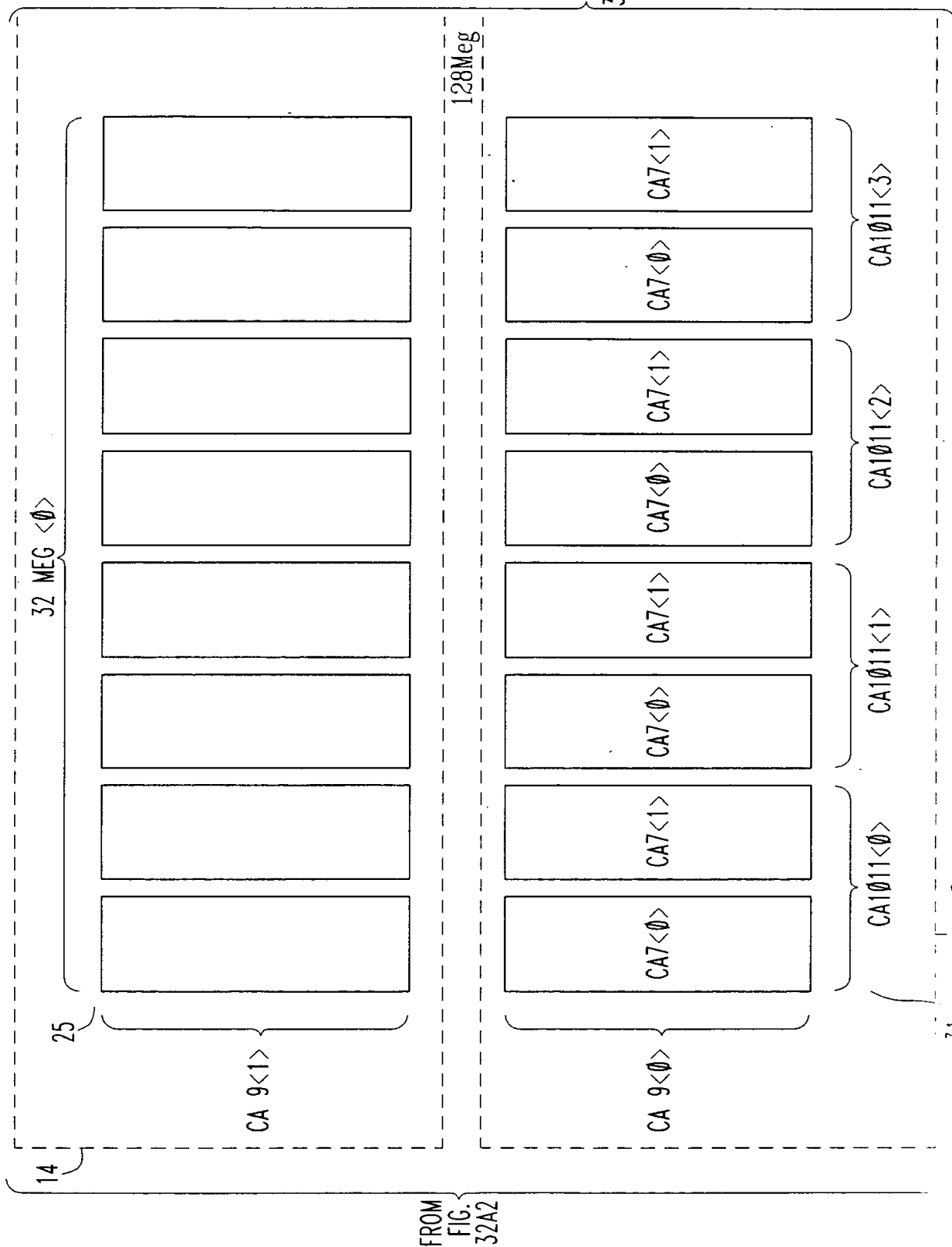


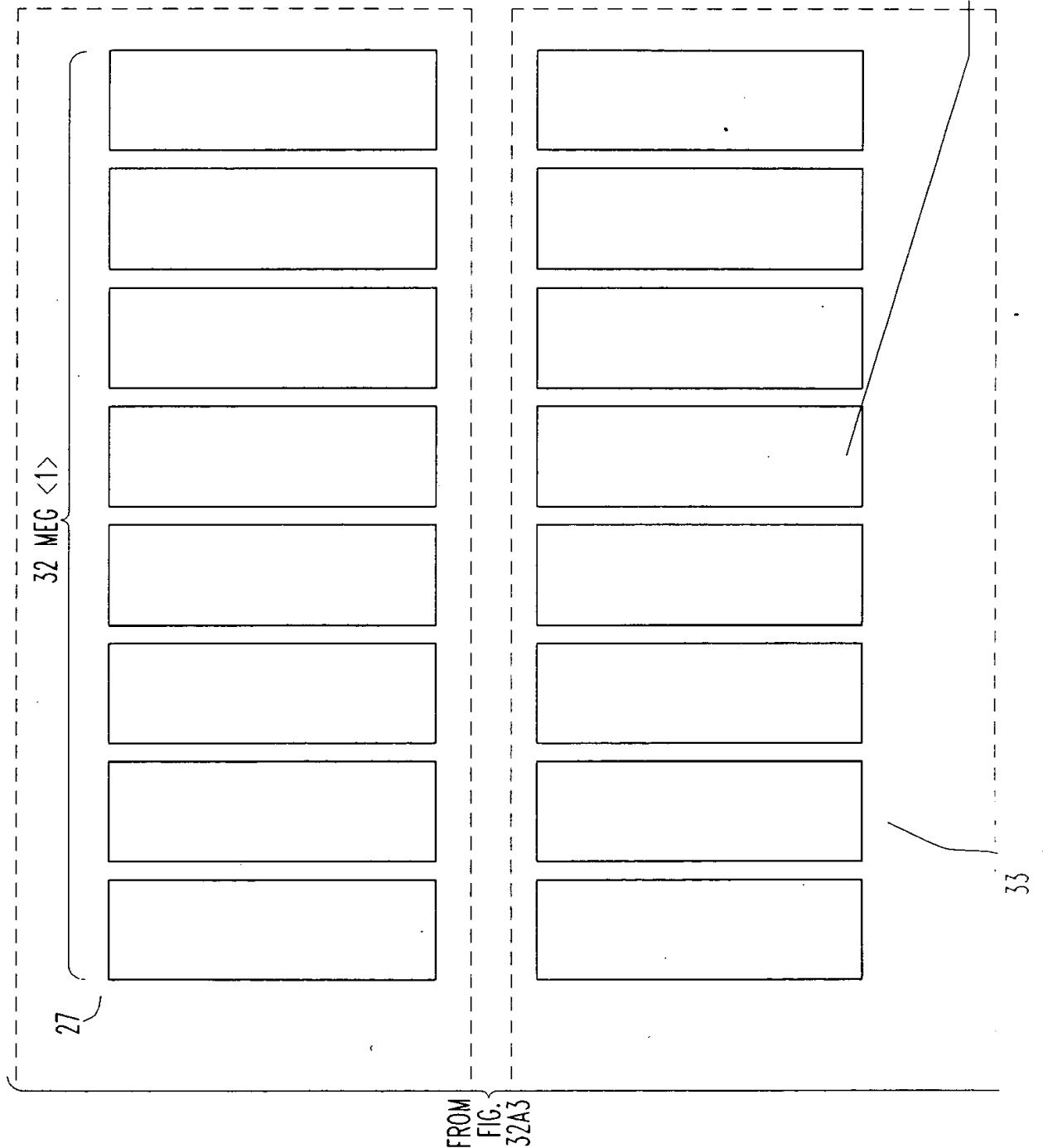
FIG. 32A1





FROM
FIG.
32A2

FIG. 32A3



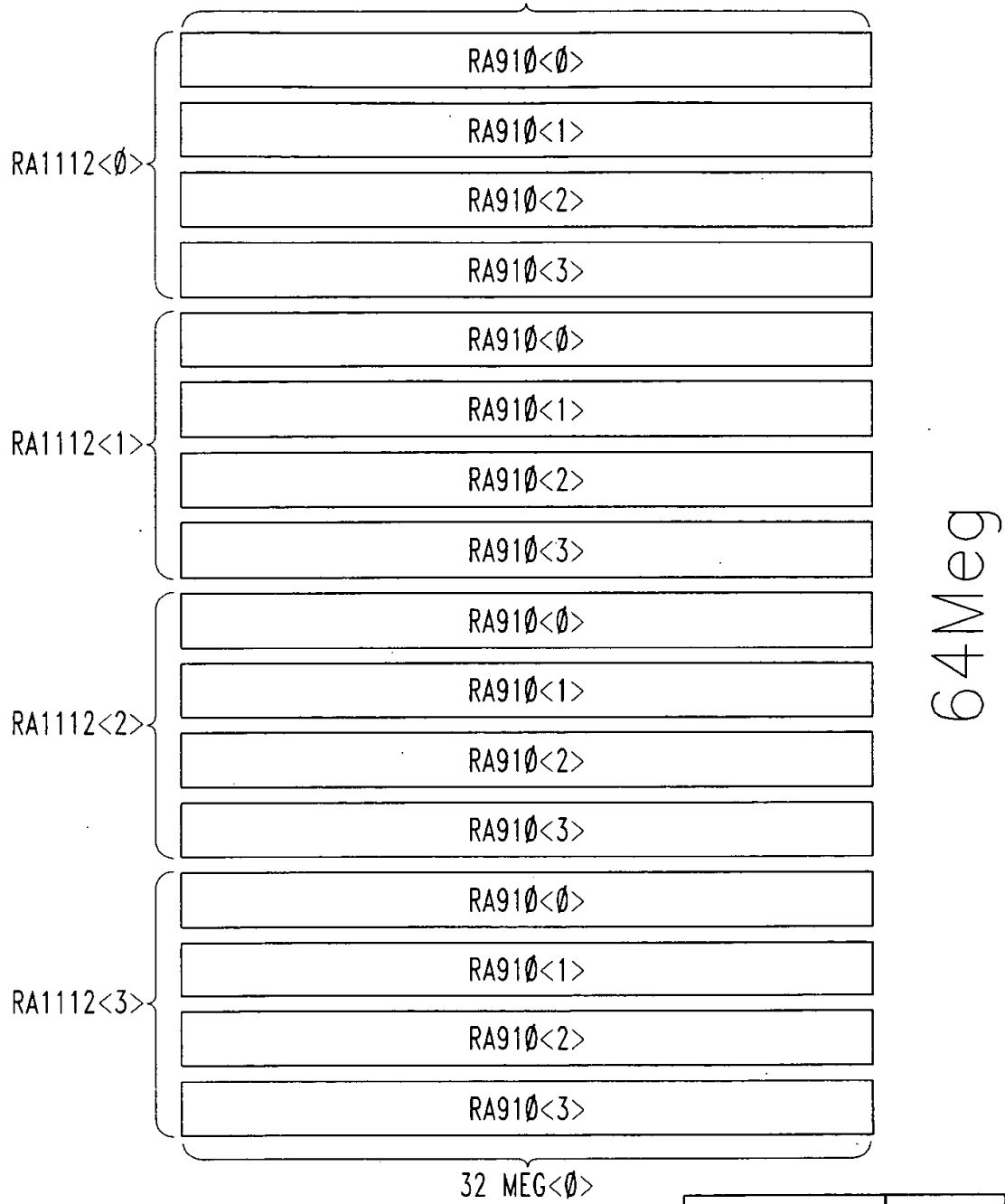


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

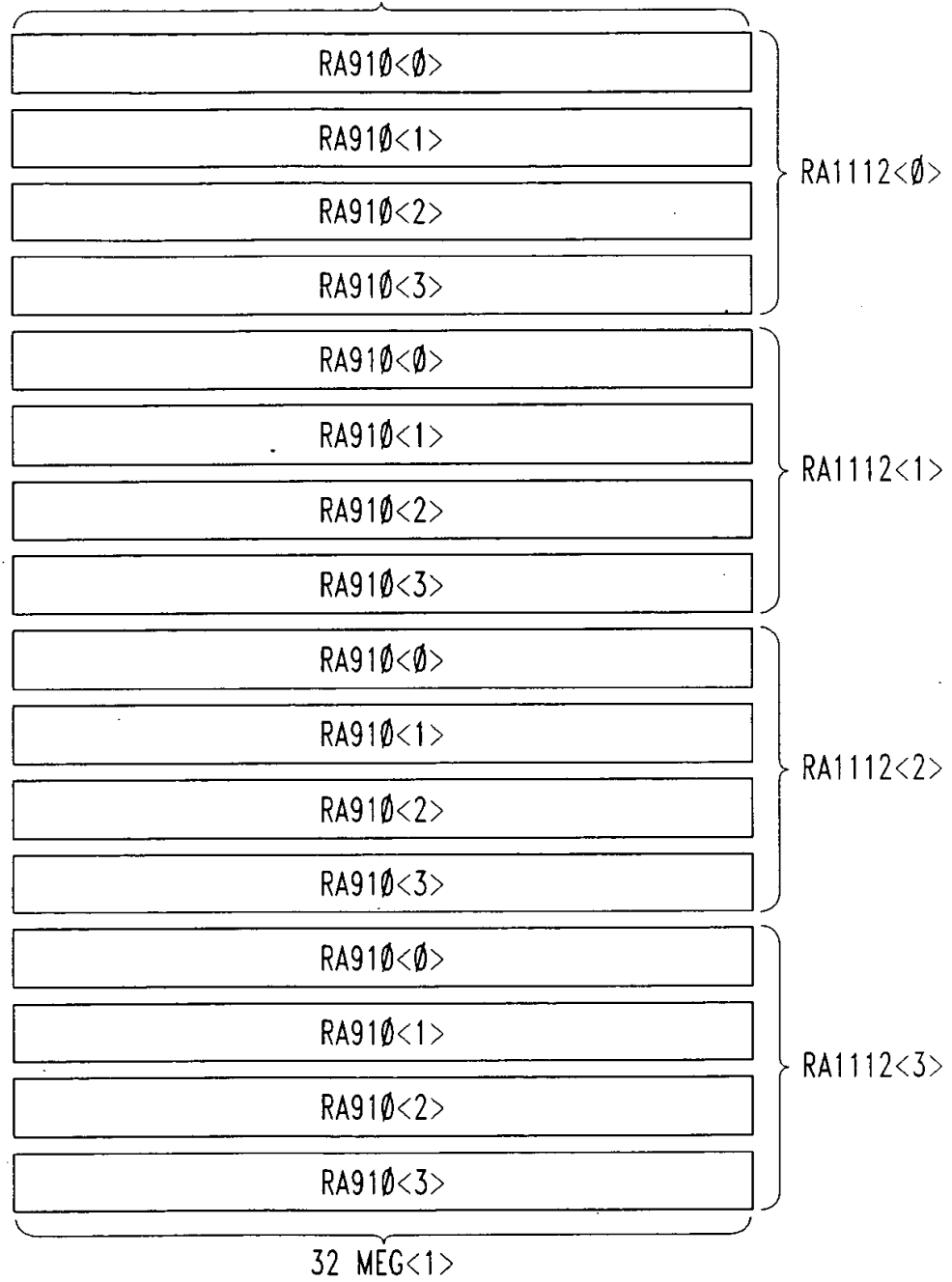
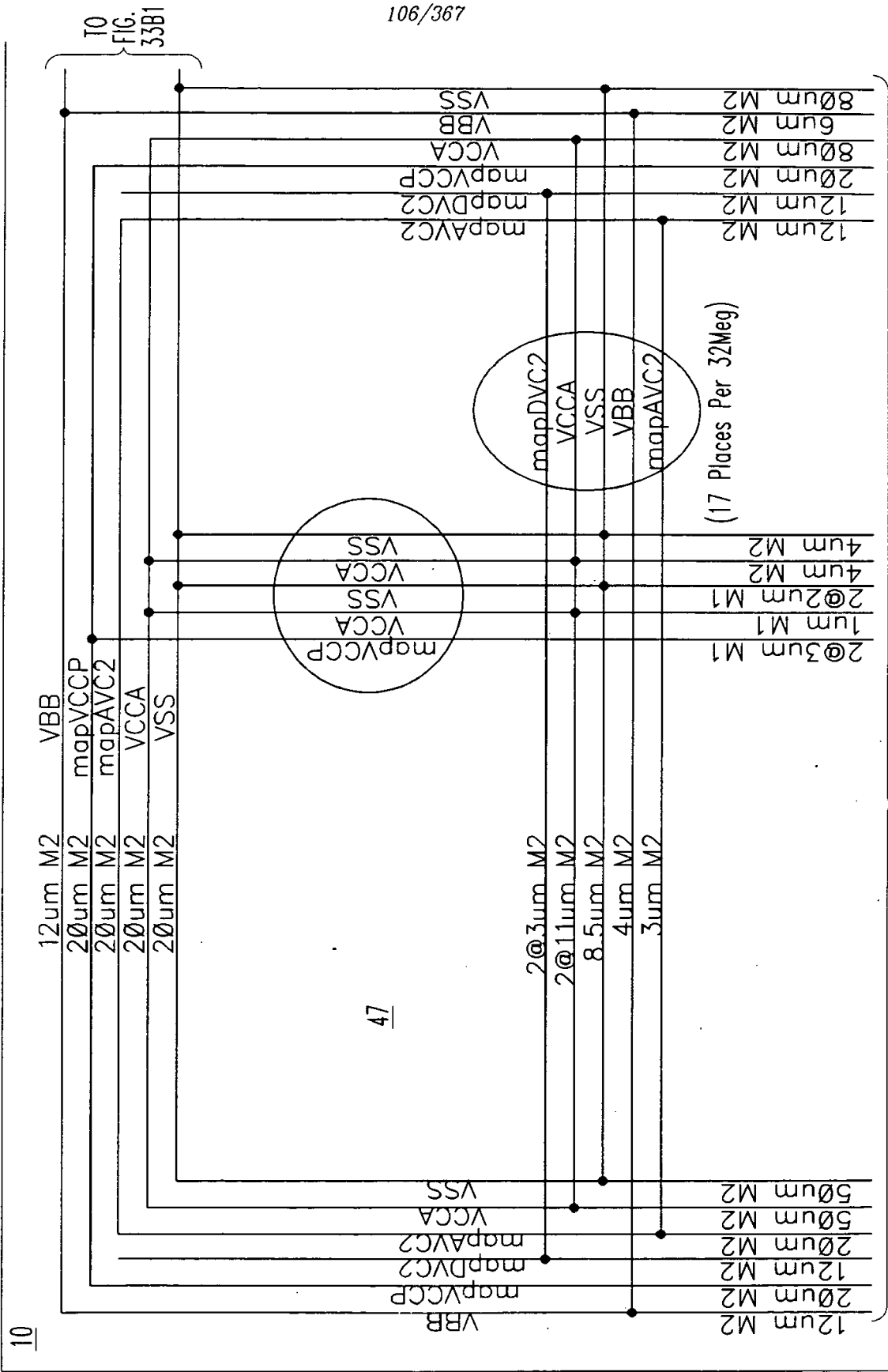


FIG. 32B2

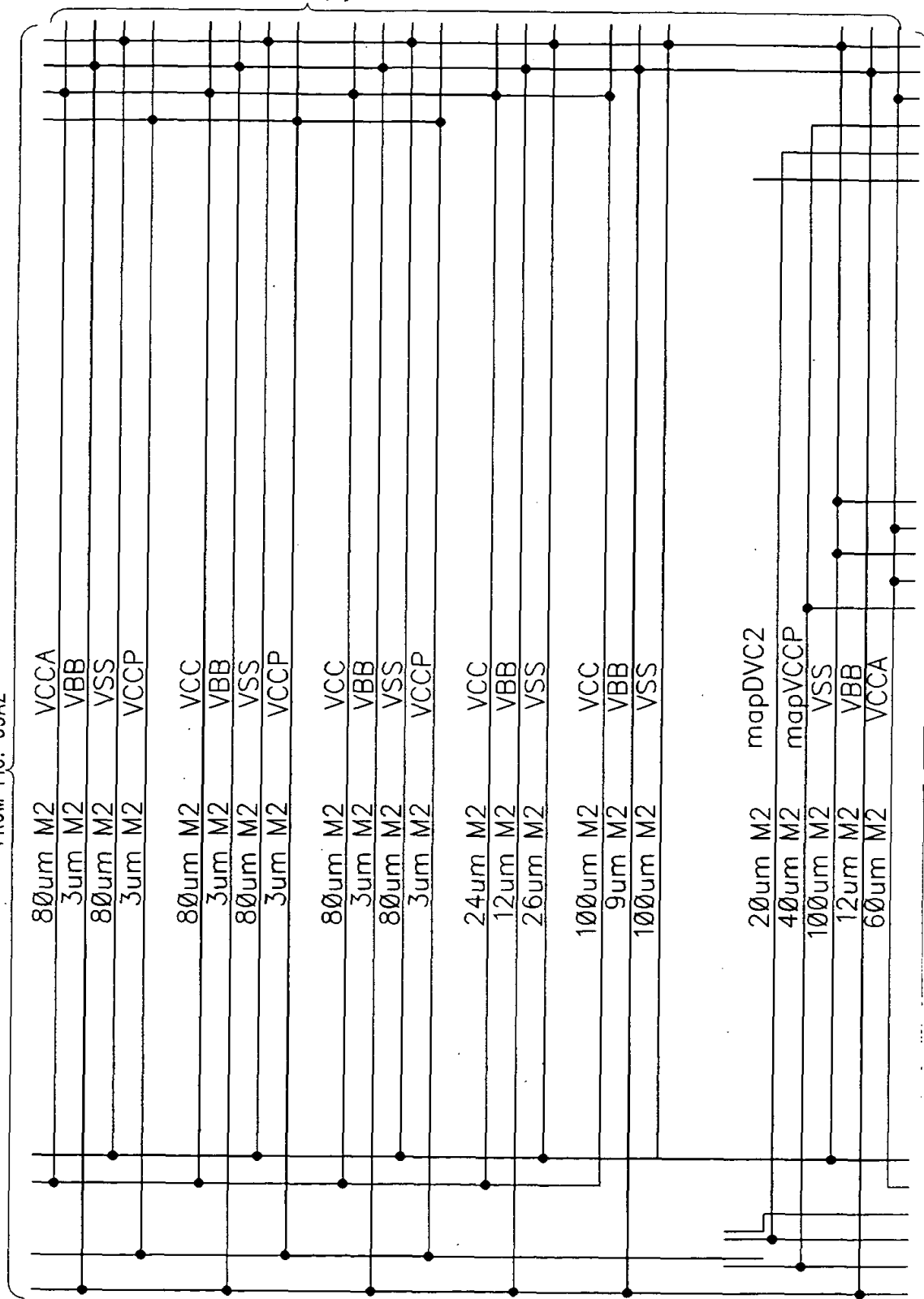


TO FIG. 33A2

FIG. 33A2

TO
FIG.
33B5

FROM FIG. 33A2



TO FIG. 33A4

FIG. 33A3

FROM FIG. 33A3

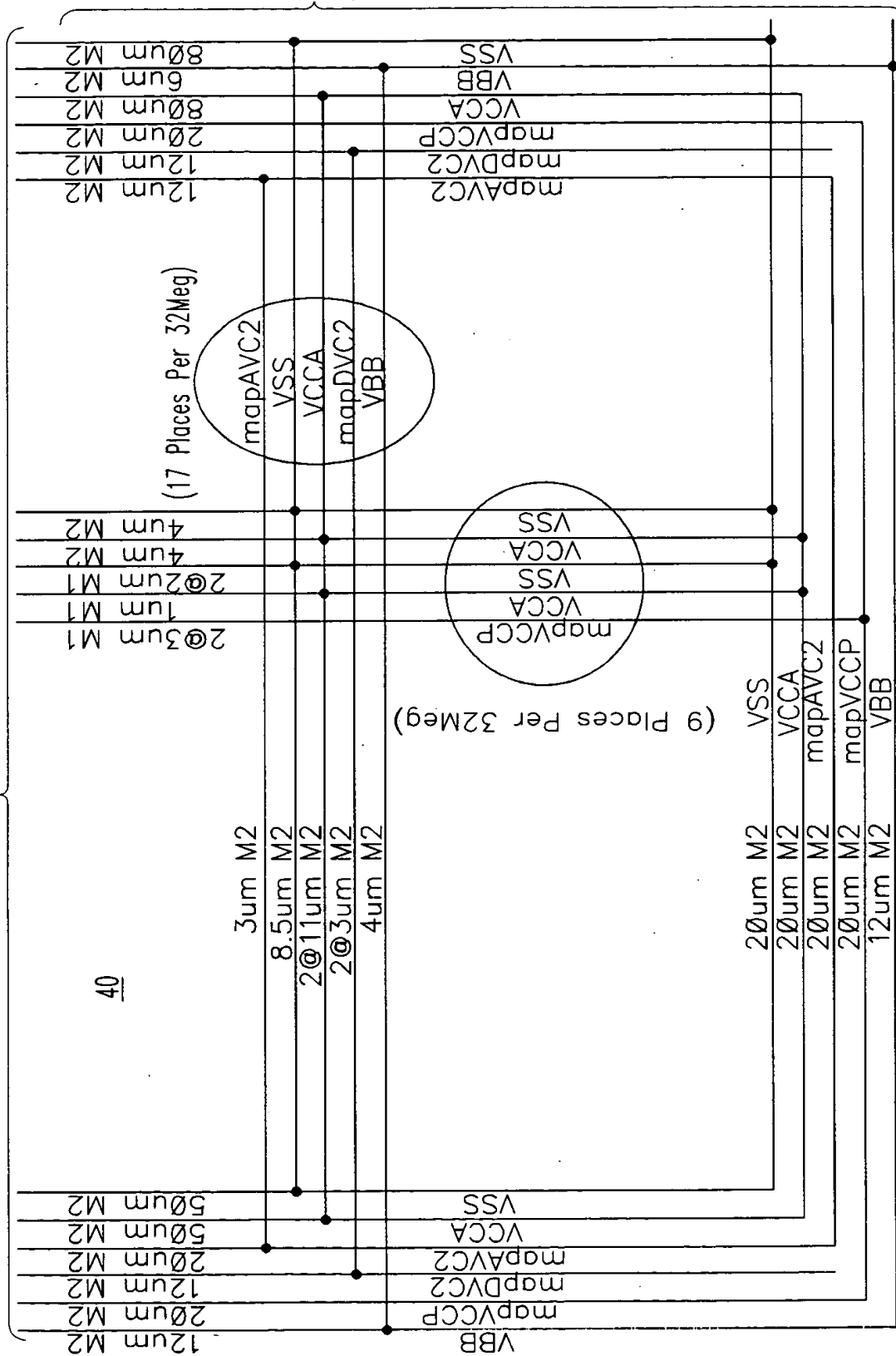
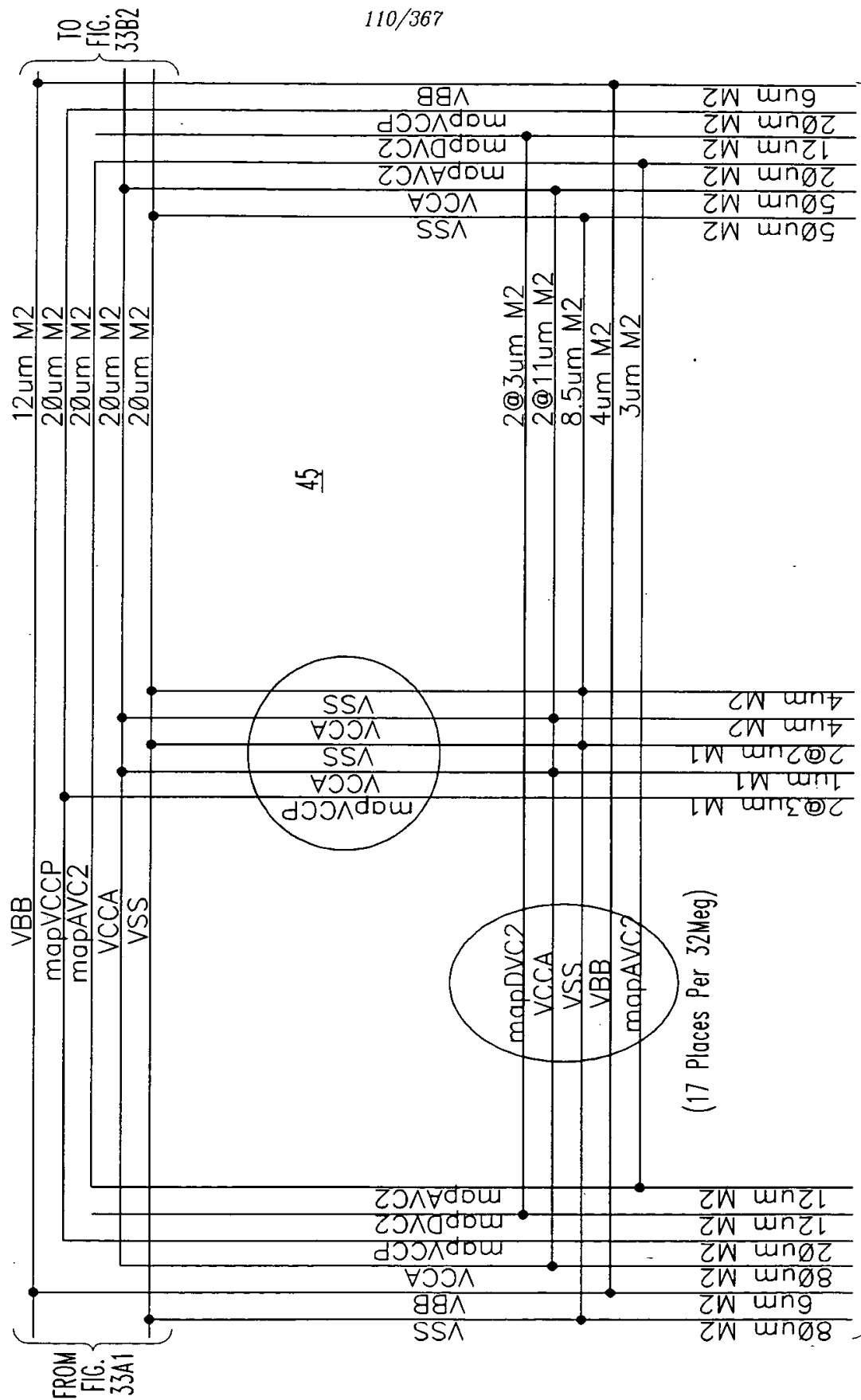


FIG. 33B7

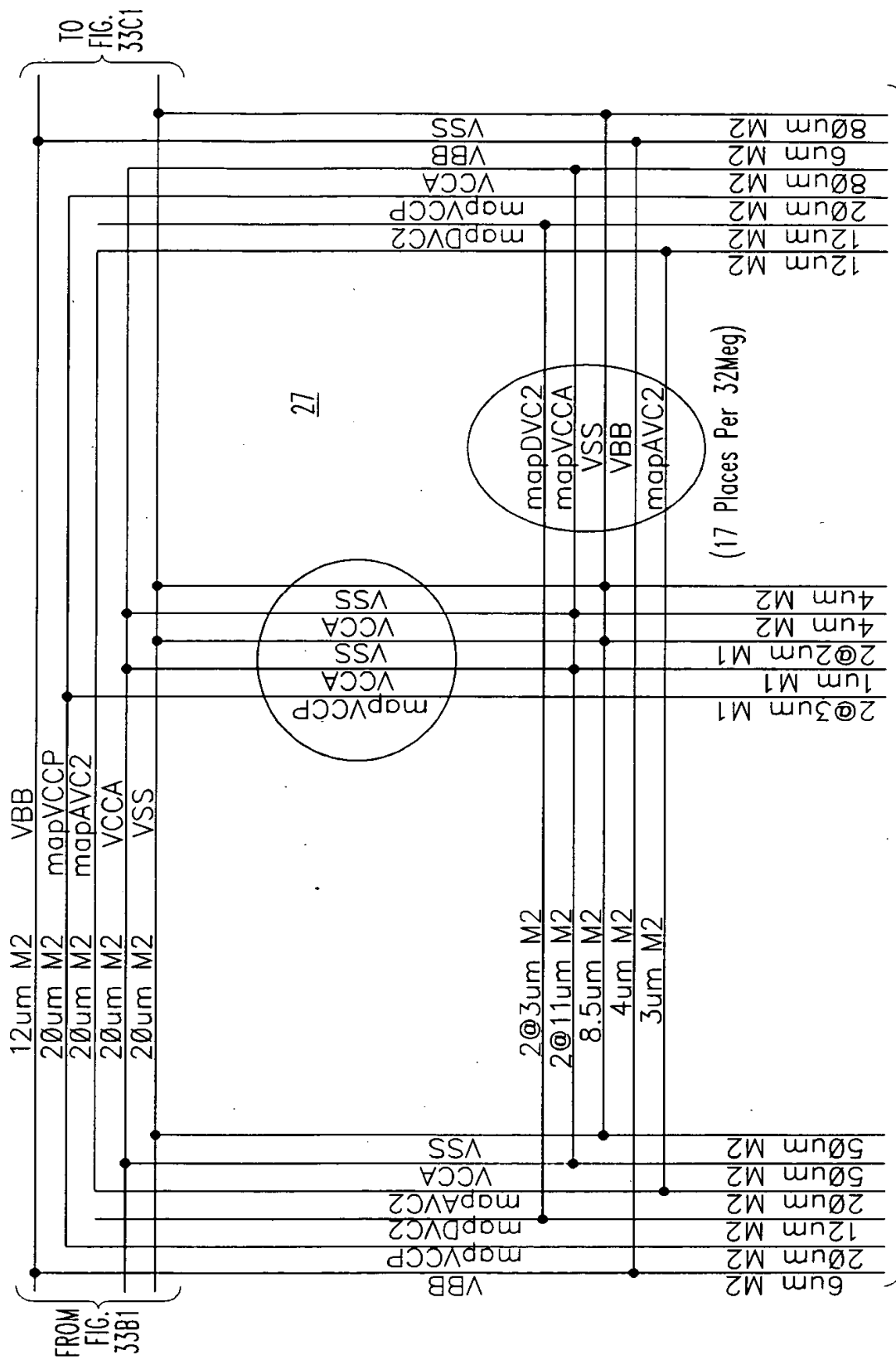
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FIG. 33A4

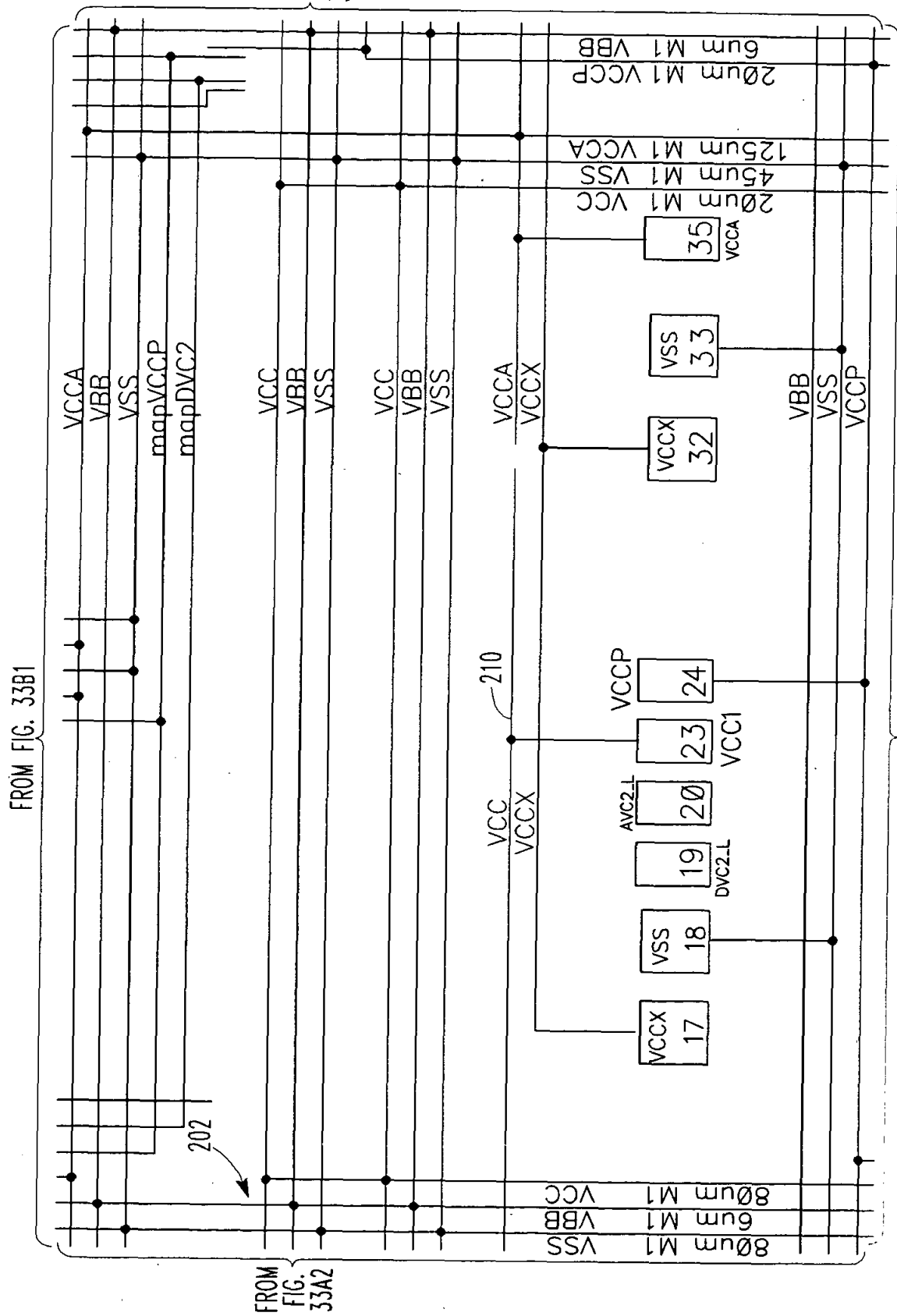


TO FIG. 33B3

FIG. 33B1



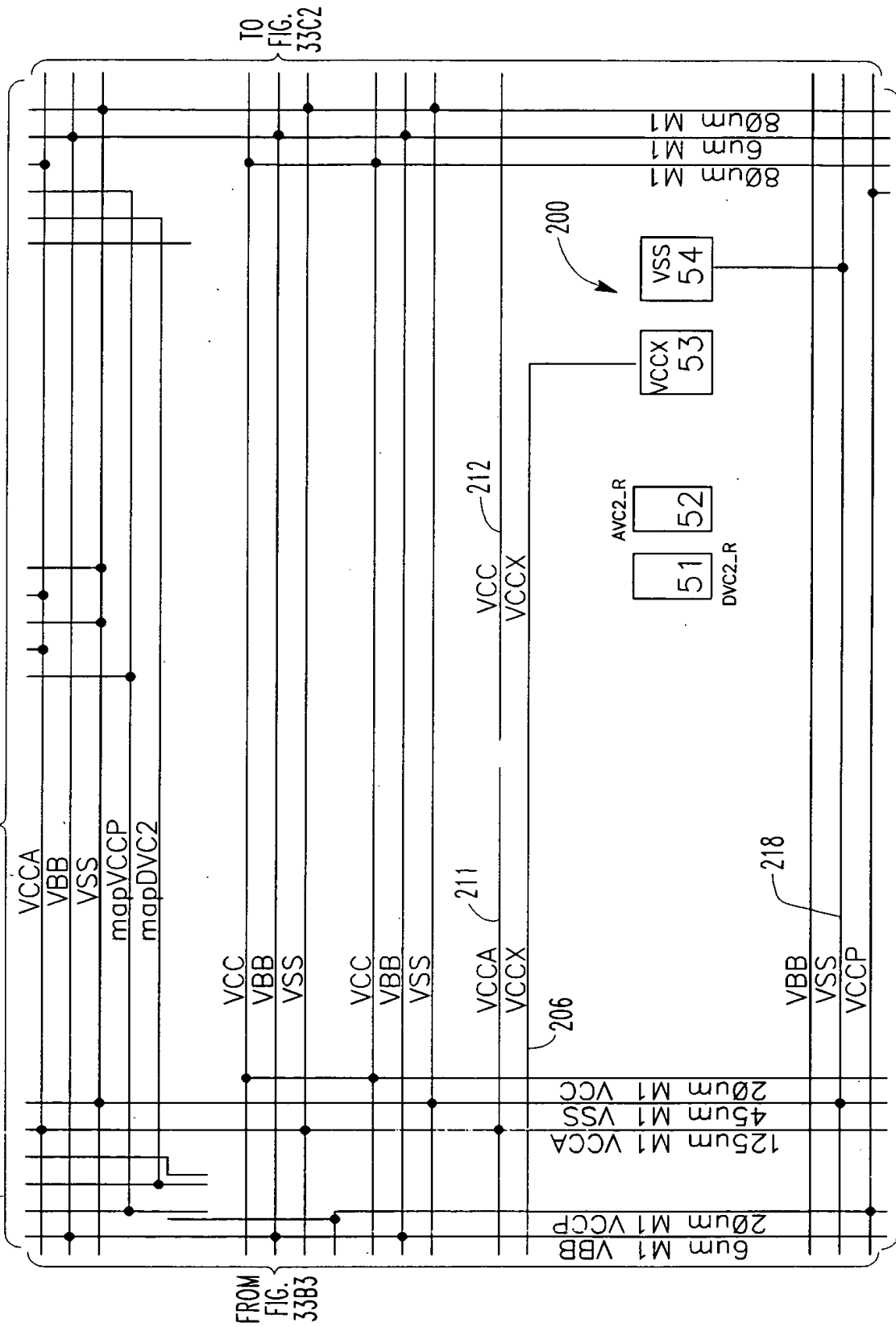
TO FIG. 33B4



TO FIG. 3383

FIG. 33B3

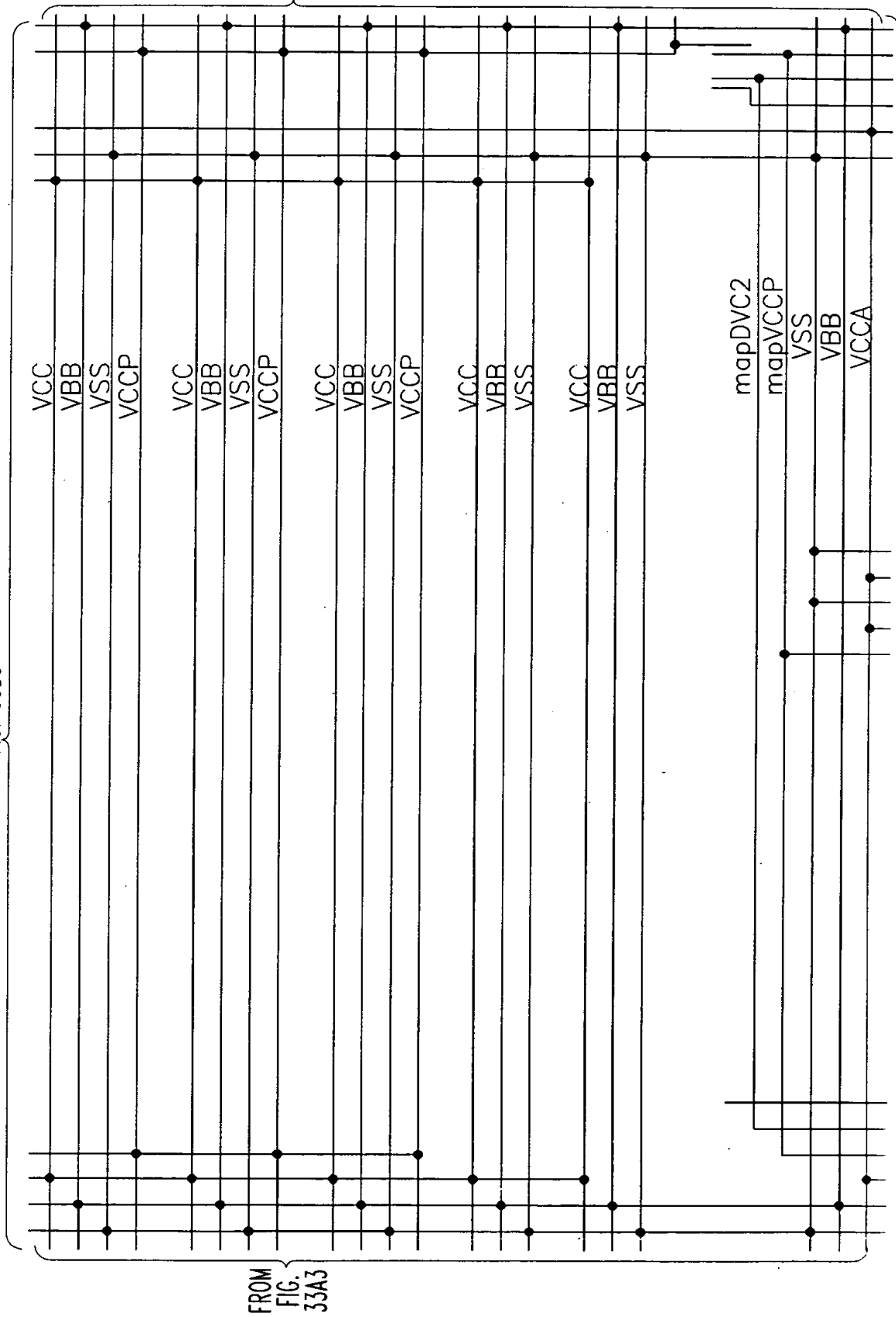
FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B4

FROM FIG. 33B3



FROM
FIG.
33A3

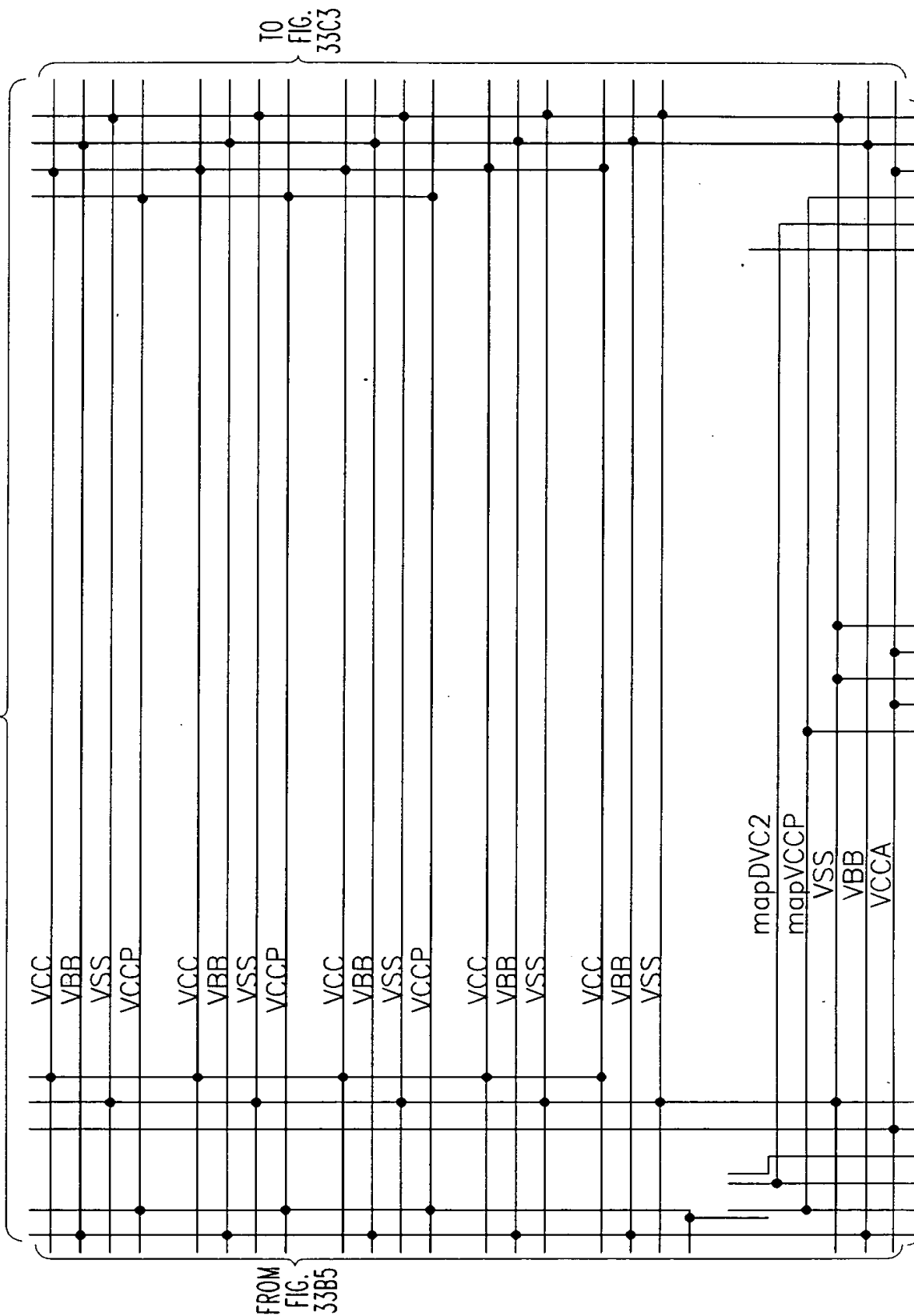
TO
FIG.
33B6

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TO FIG. 33B7

FIG. 33B5

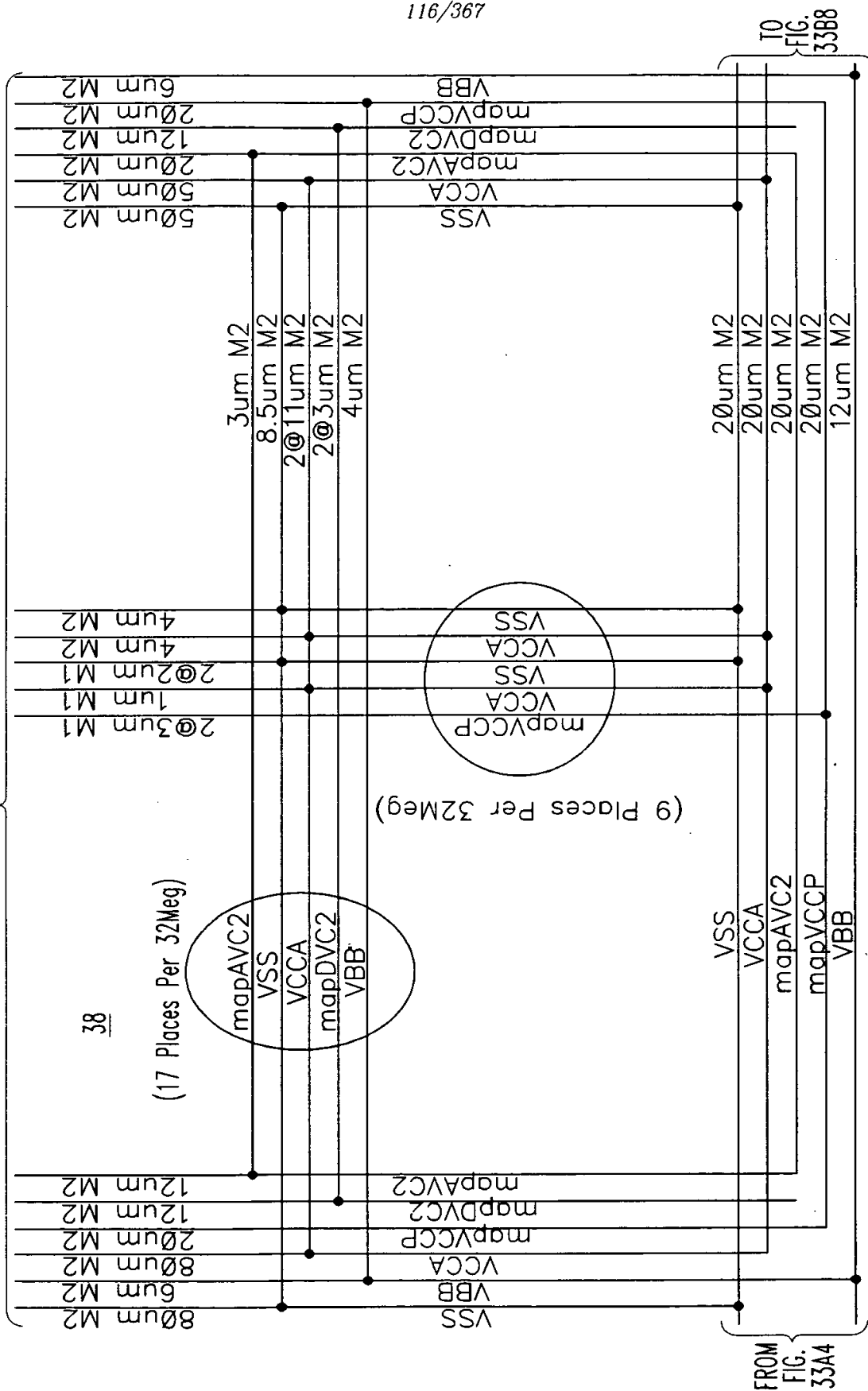
FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

FROM FIG. 33B5



FROM FIG. 33B6

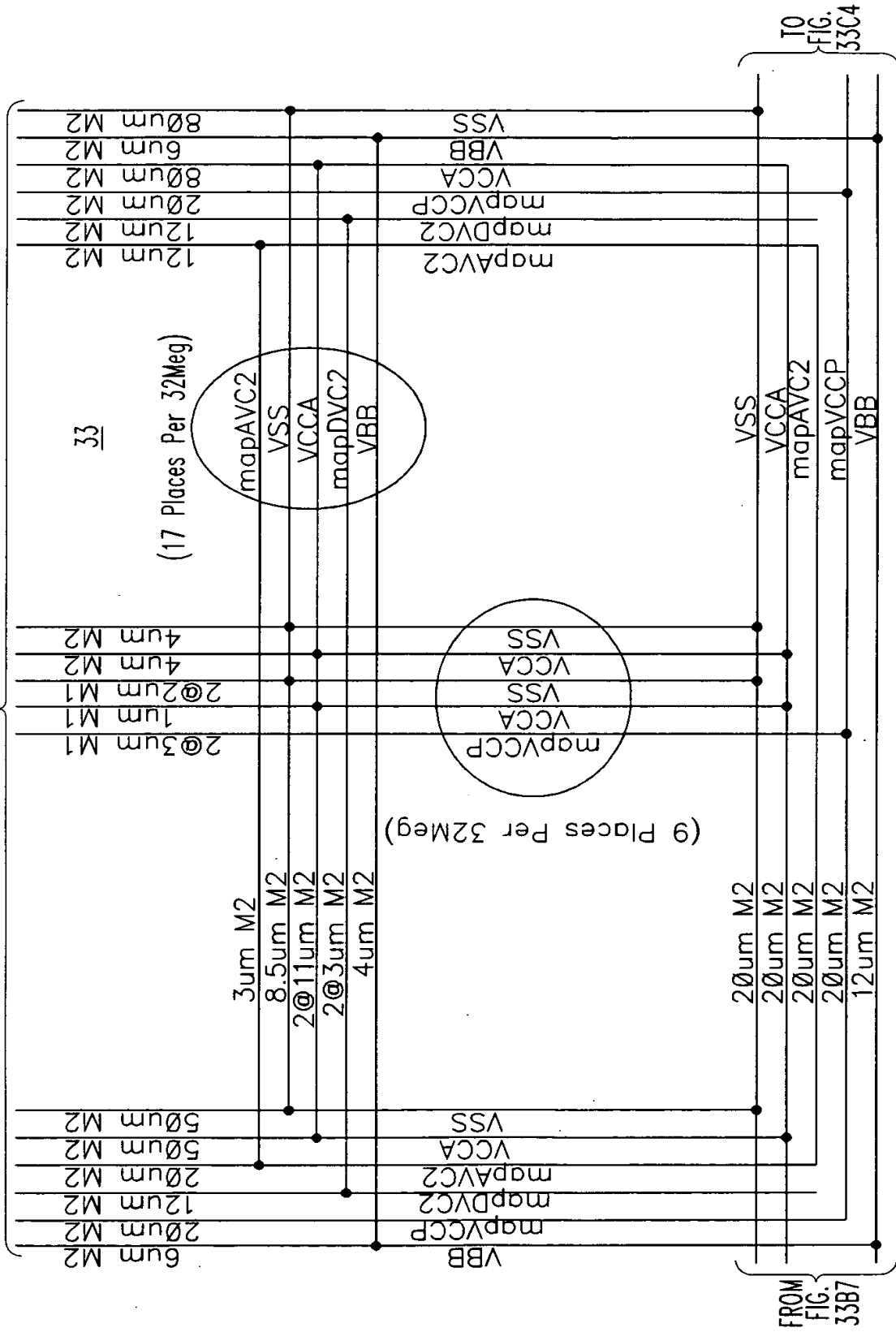
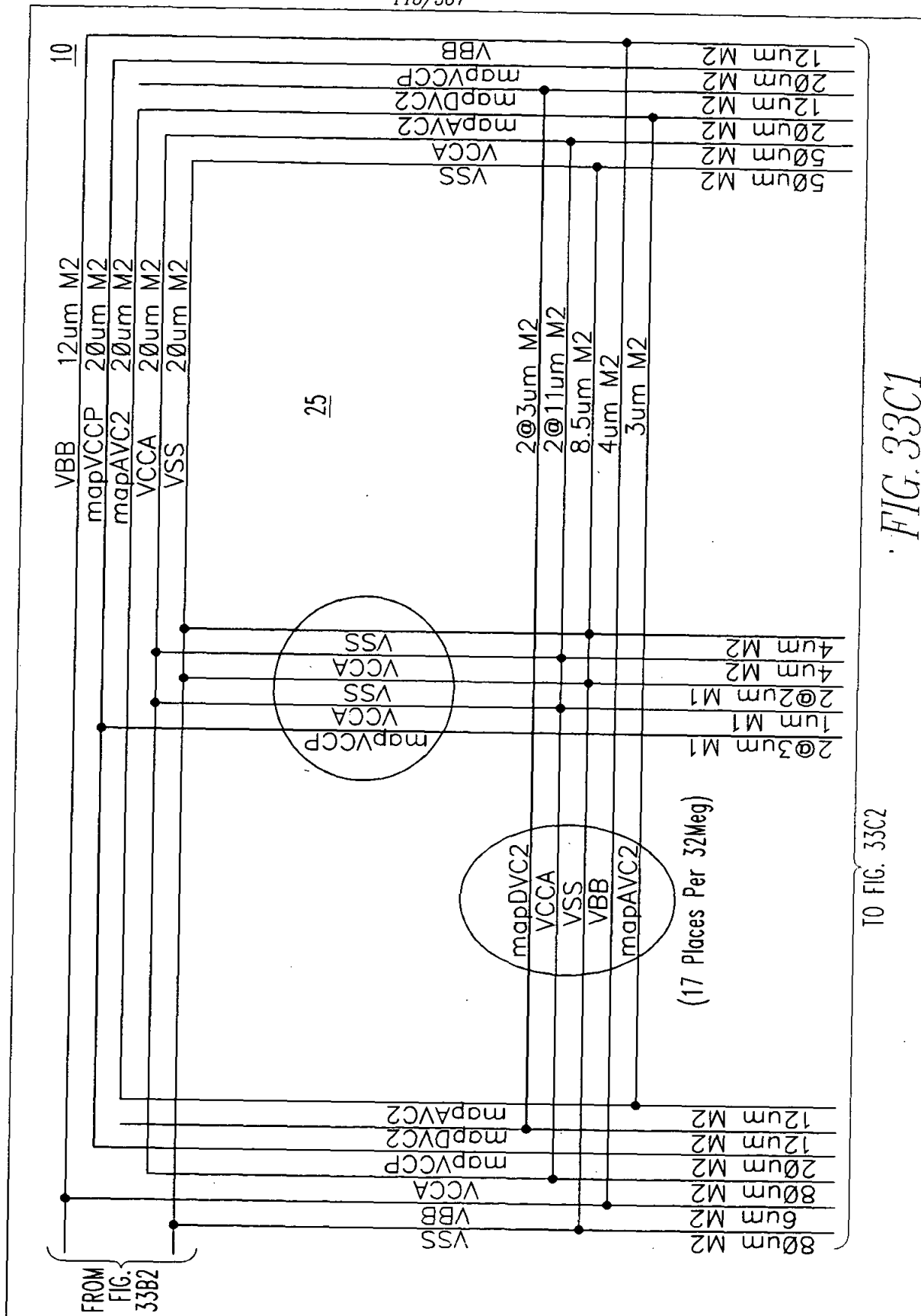


FIG. 33B8



FROM FIG. 33C1

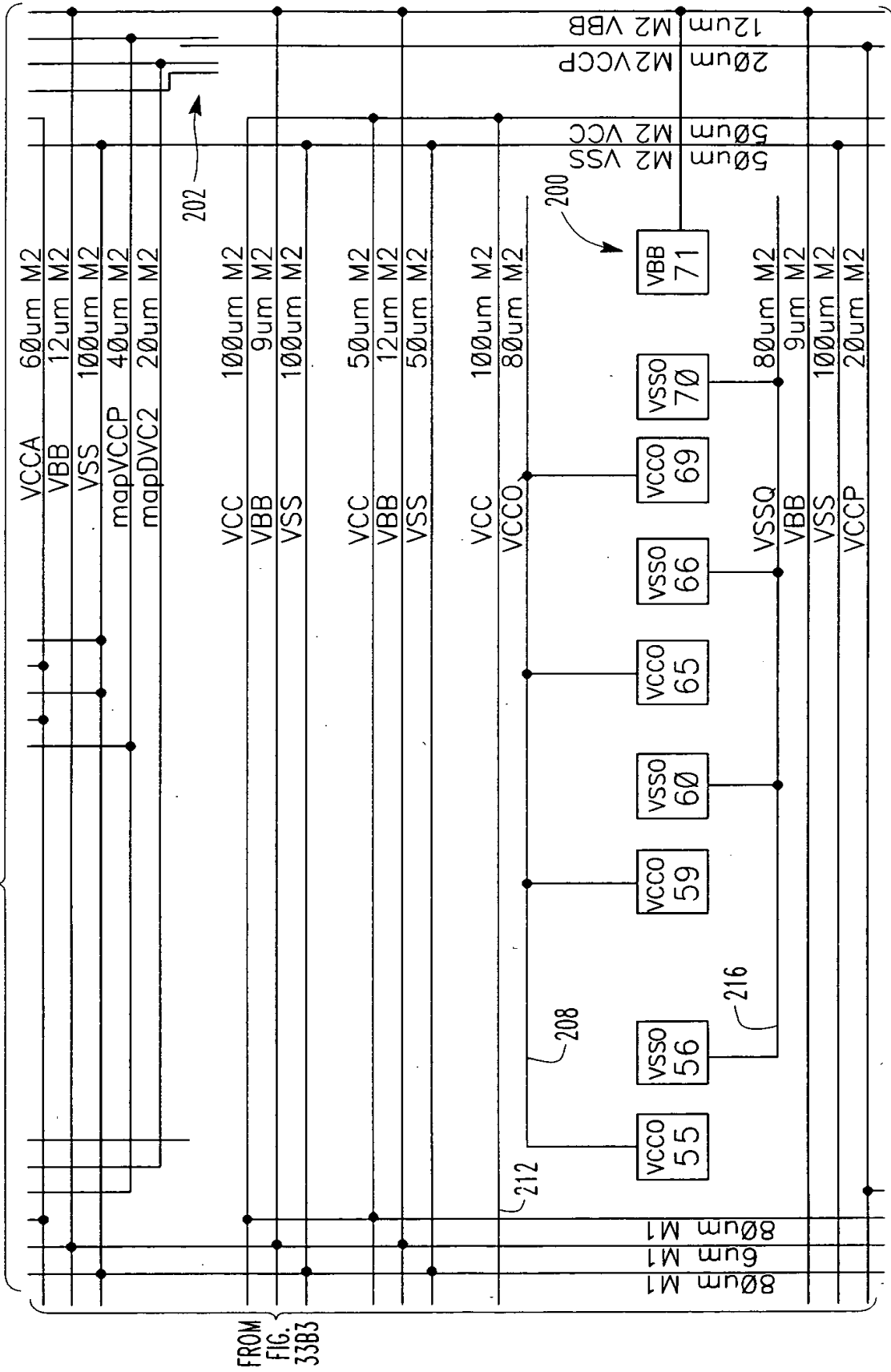
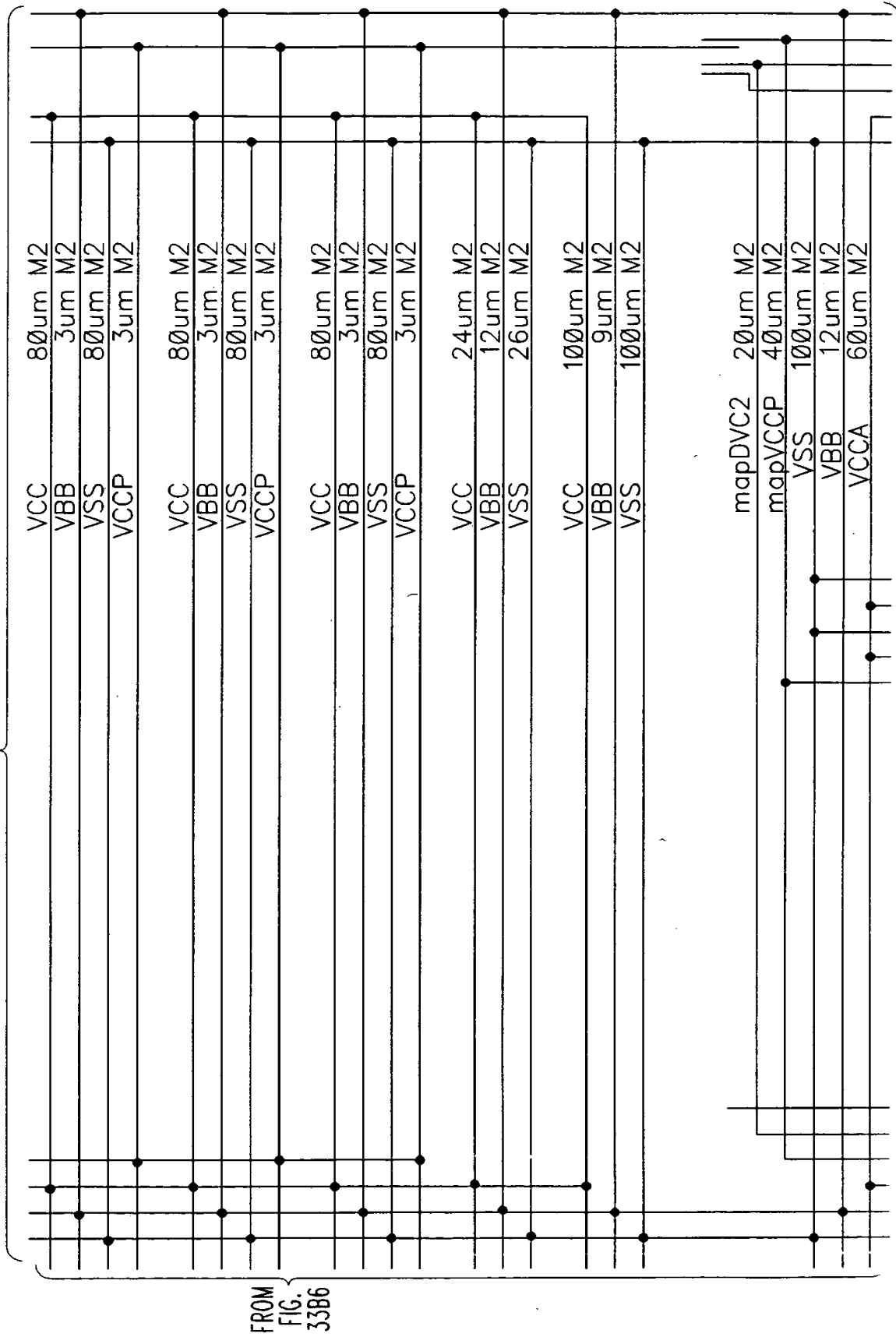


FIG. 33C2

TO FIG. 33C3

FIG. 33C3

FROM FIG. 33C2



TO FIG. 33C4

FIG. 33C3

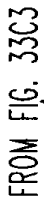


FIG. 33C4

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10

45

200

DVC2
GENERATOR 500

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP
PUMP CIRCUITS 402

DVC2
GENERATOR 501

TO
FIG. 33D3

TO FIG. 33D2

FIG. 33D1

TO FIG. 33D1

47

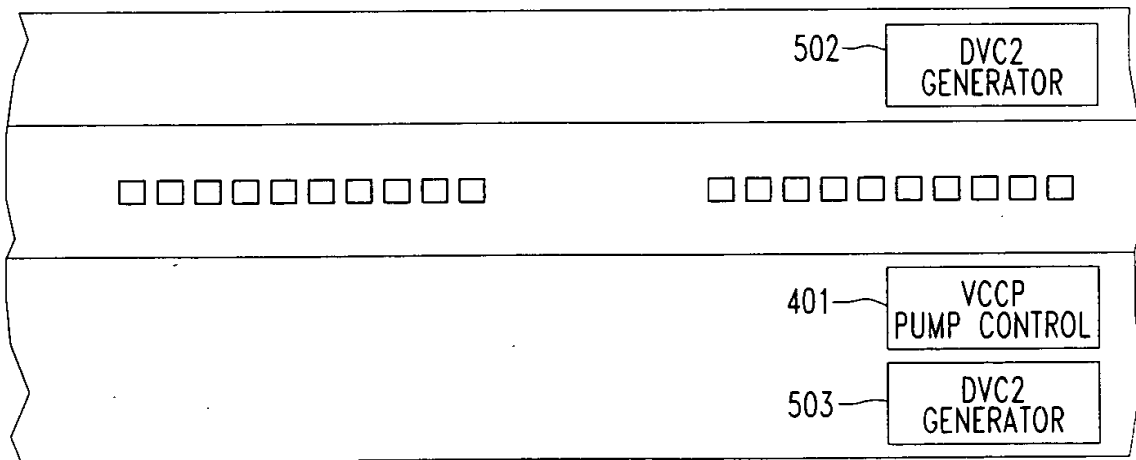
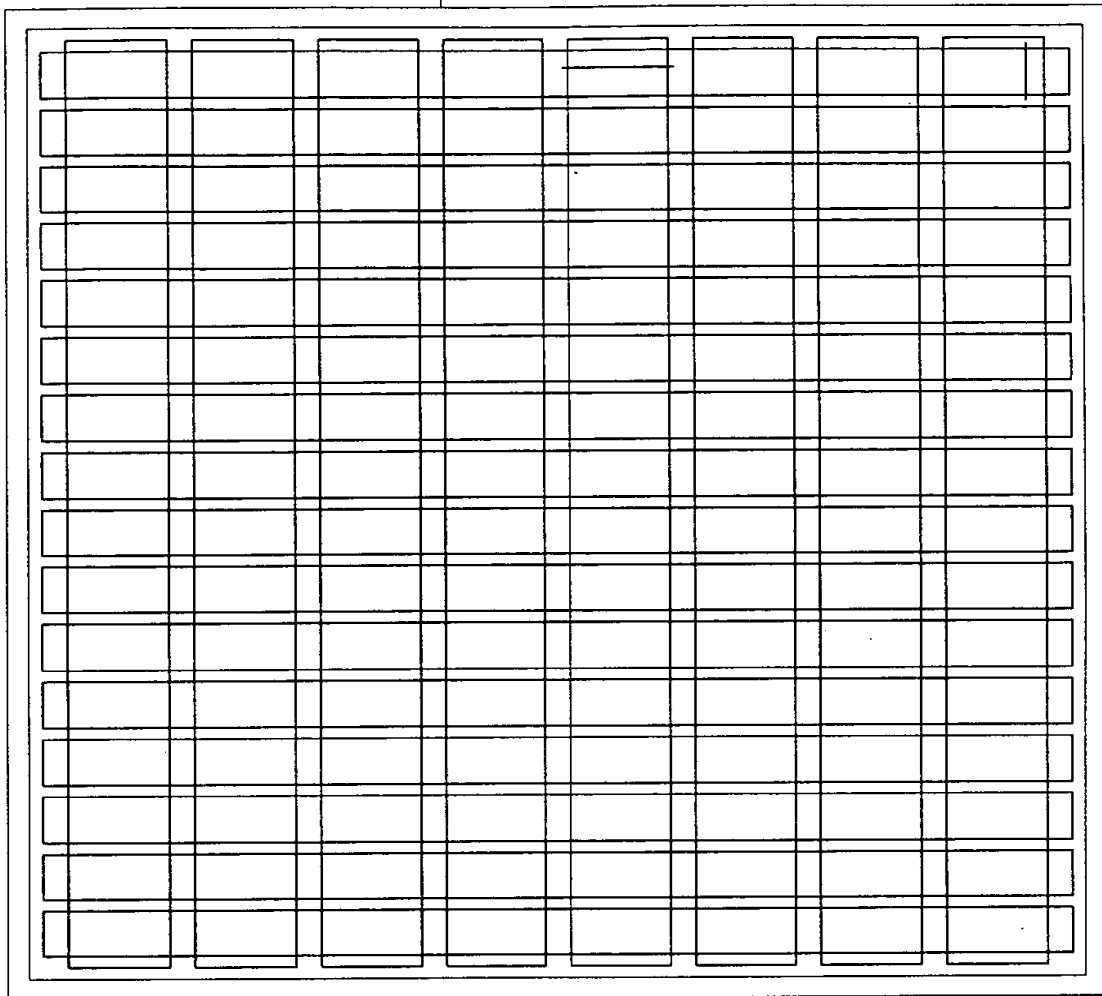
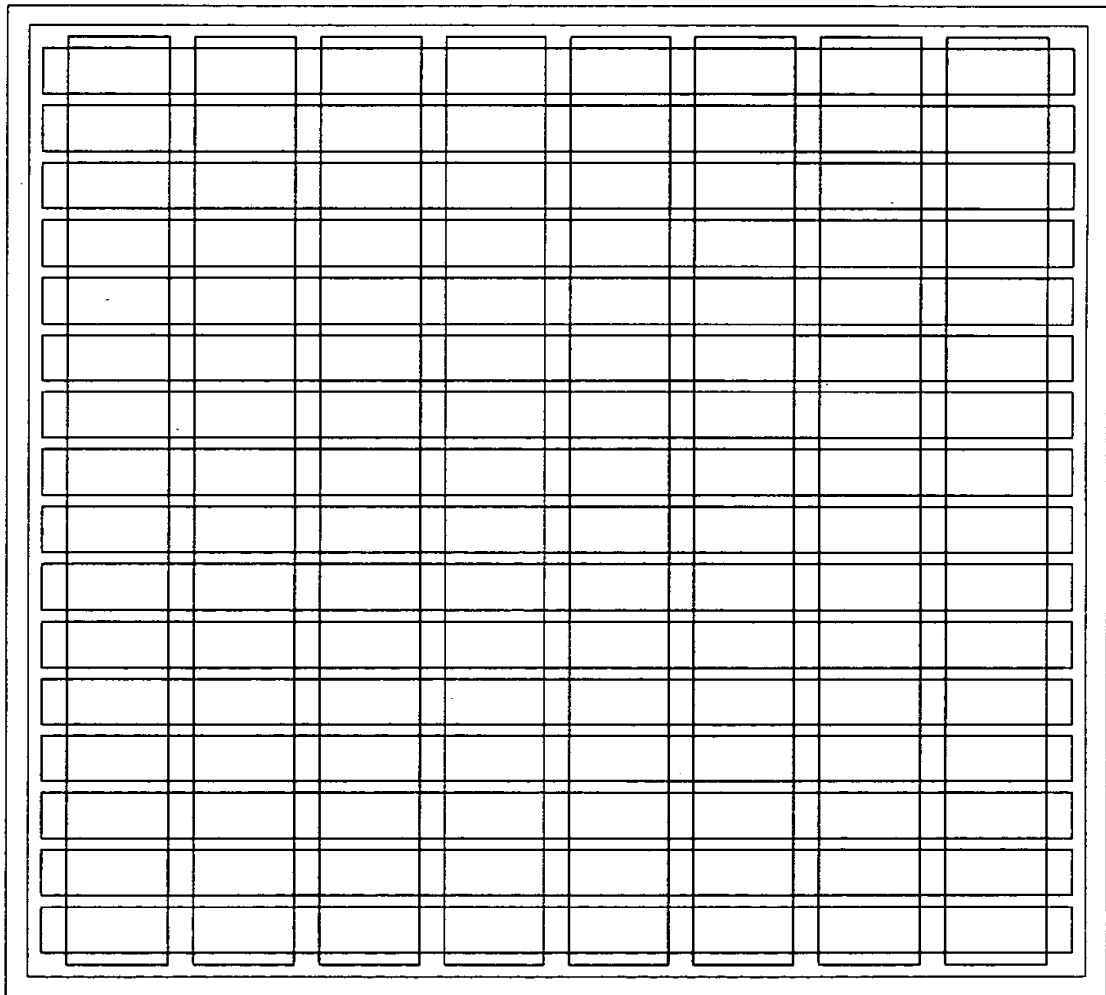


FIG. 33D2

TO
FIG.
33D4

TO
FIG.
33D1

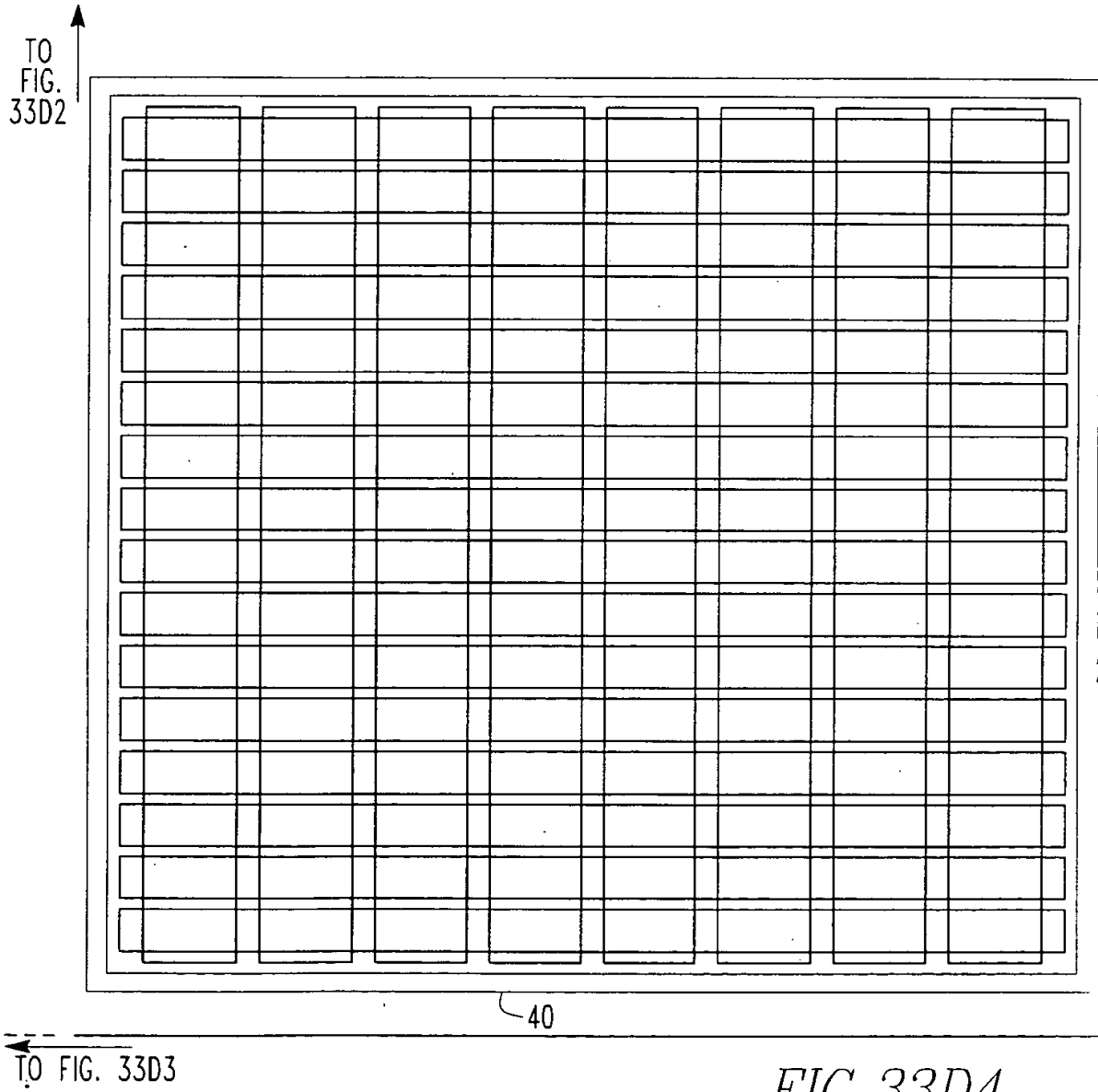
(SEE FIG. 33E1)



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TO FIG. 33D4

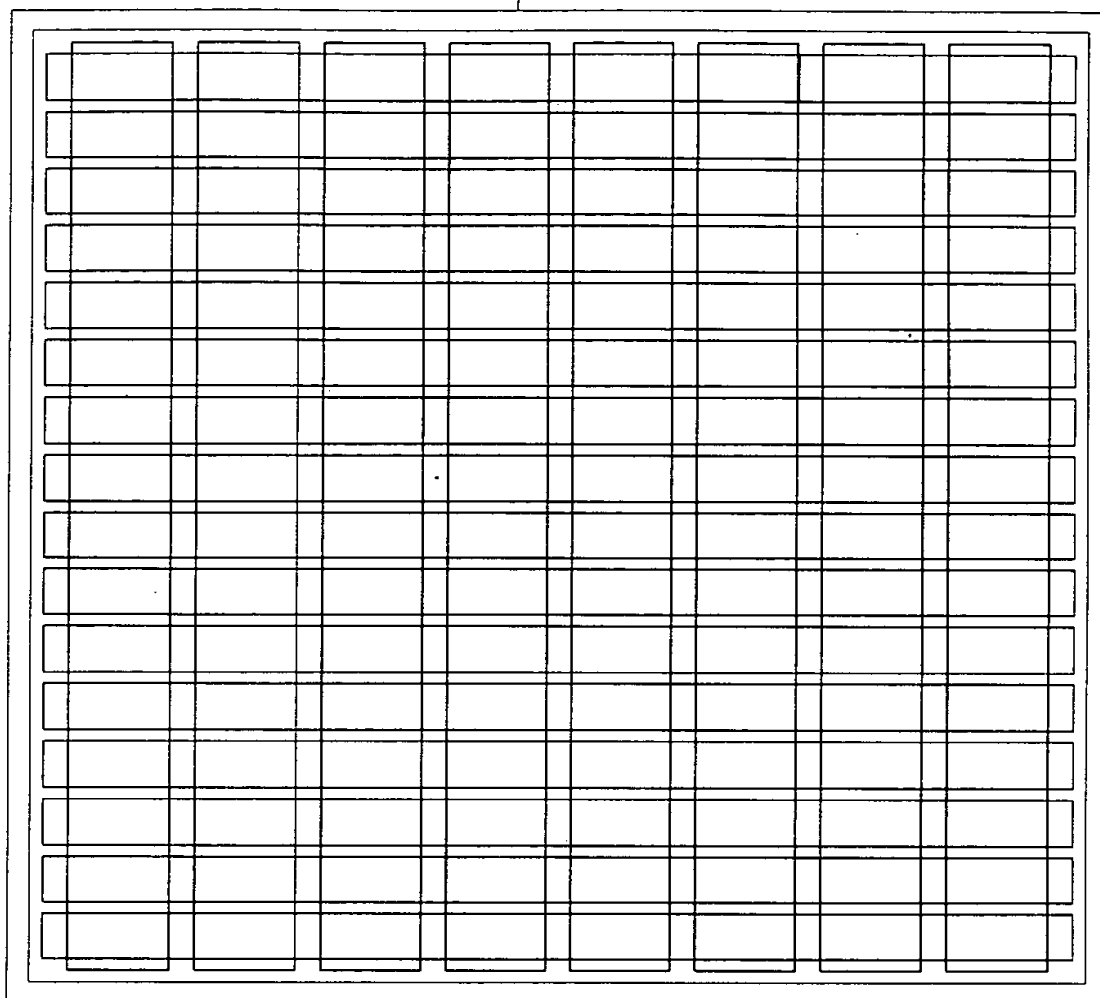
FIG. 33D3



(SEE FIG. 33D2)

25

TO FIG. 33E2



DVC2
GENERATOR 504

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP
REGULATOR 220

DVC2
GENERATOR 505

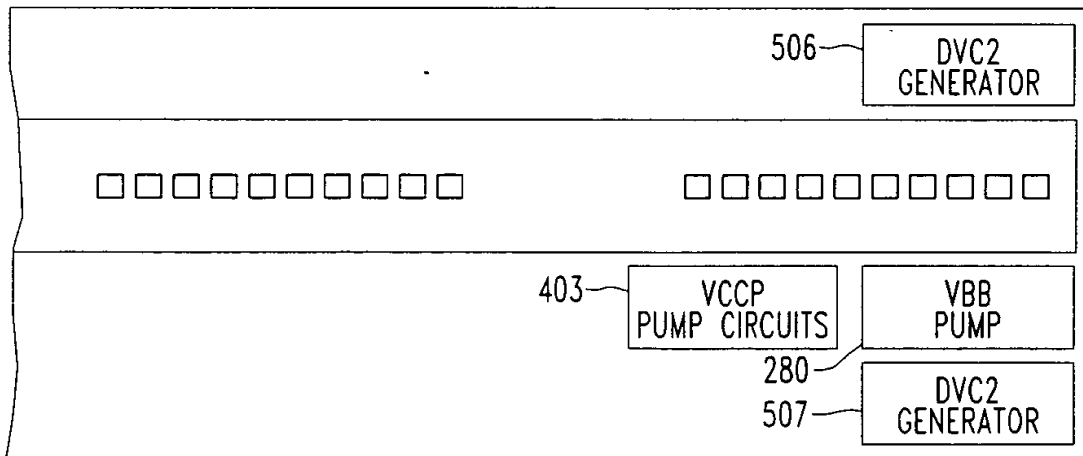
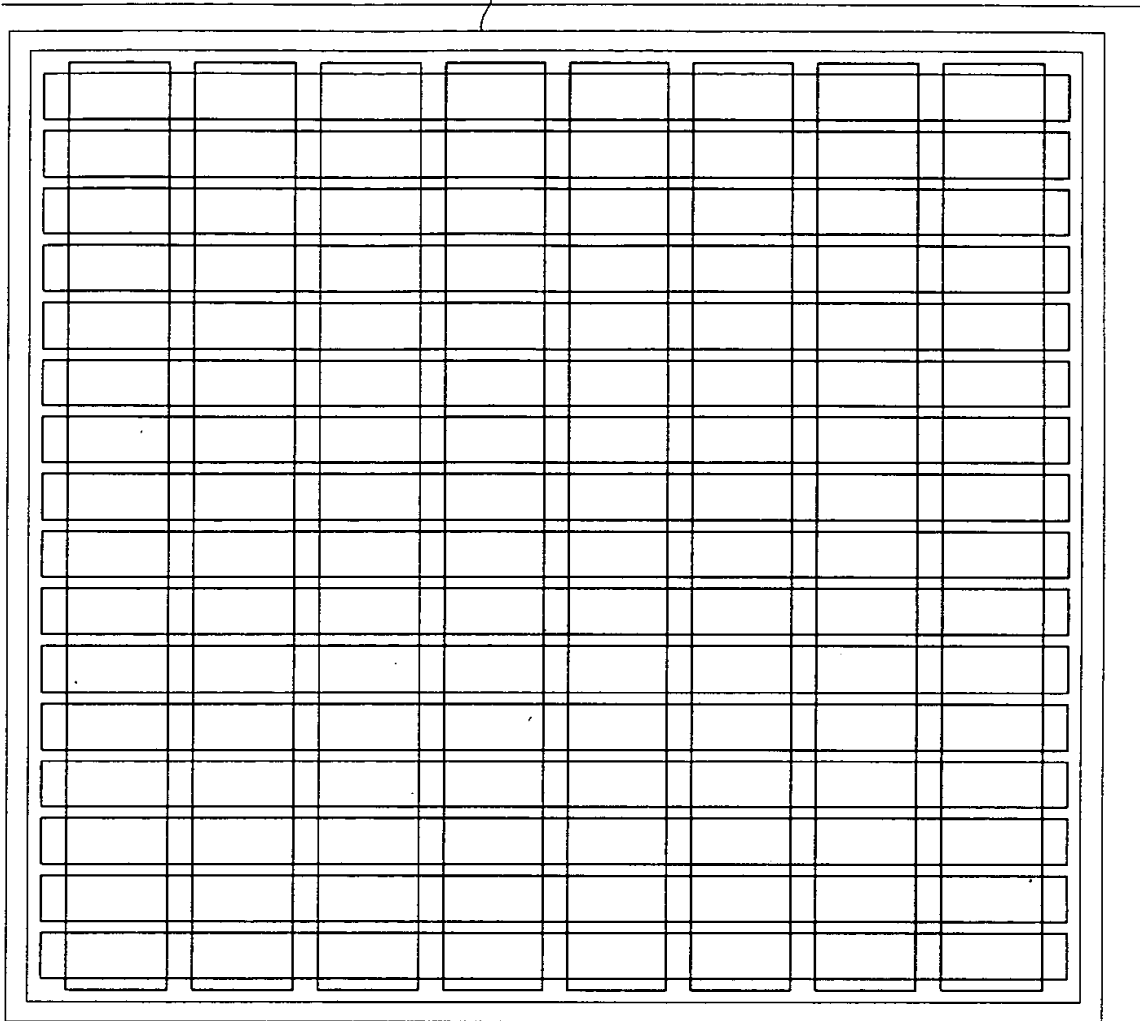
TO
FIG.
33E3

FIG. 33E1

TO FIG. 33E1

27

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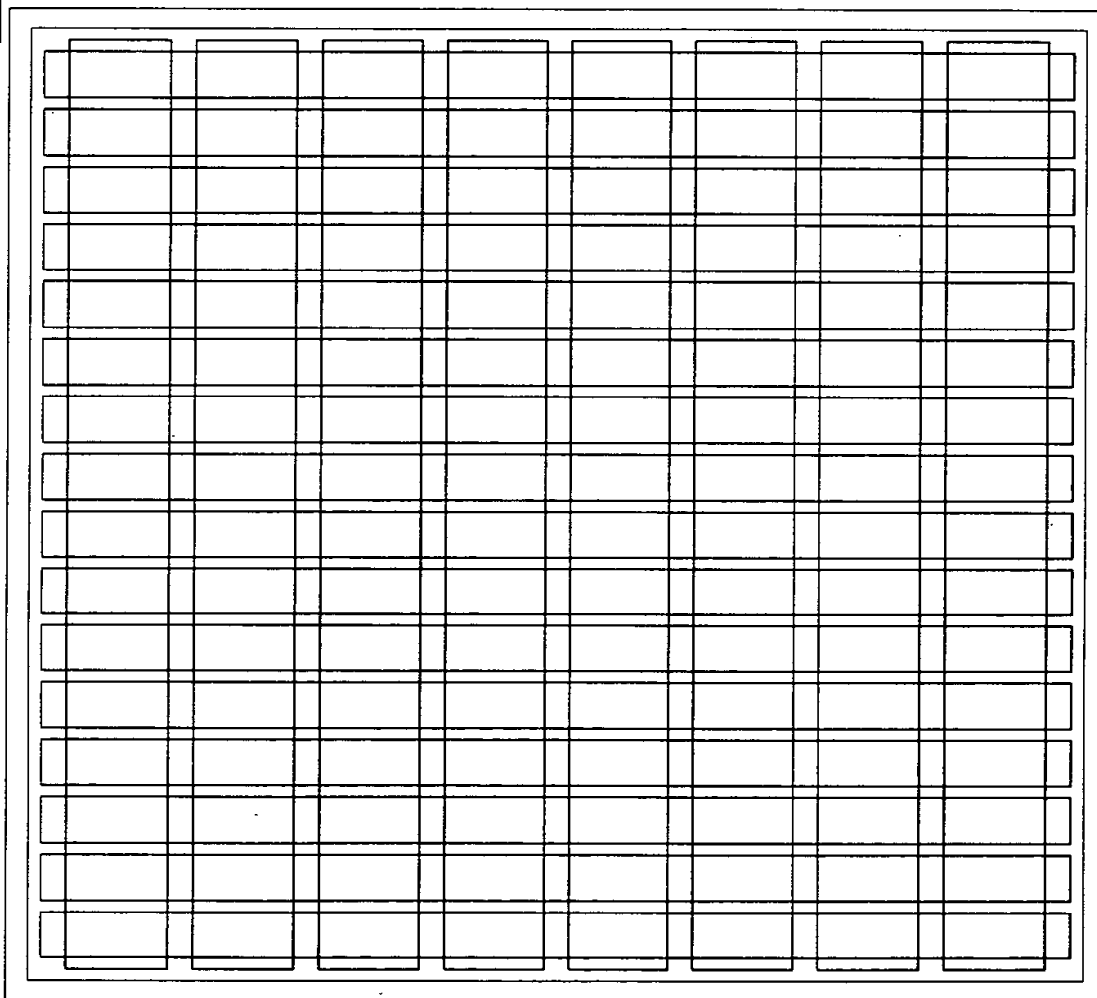


200

FIG. 33E2

TO FIG. 33E4

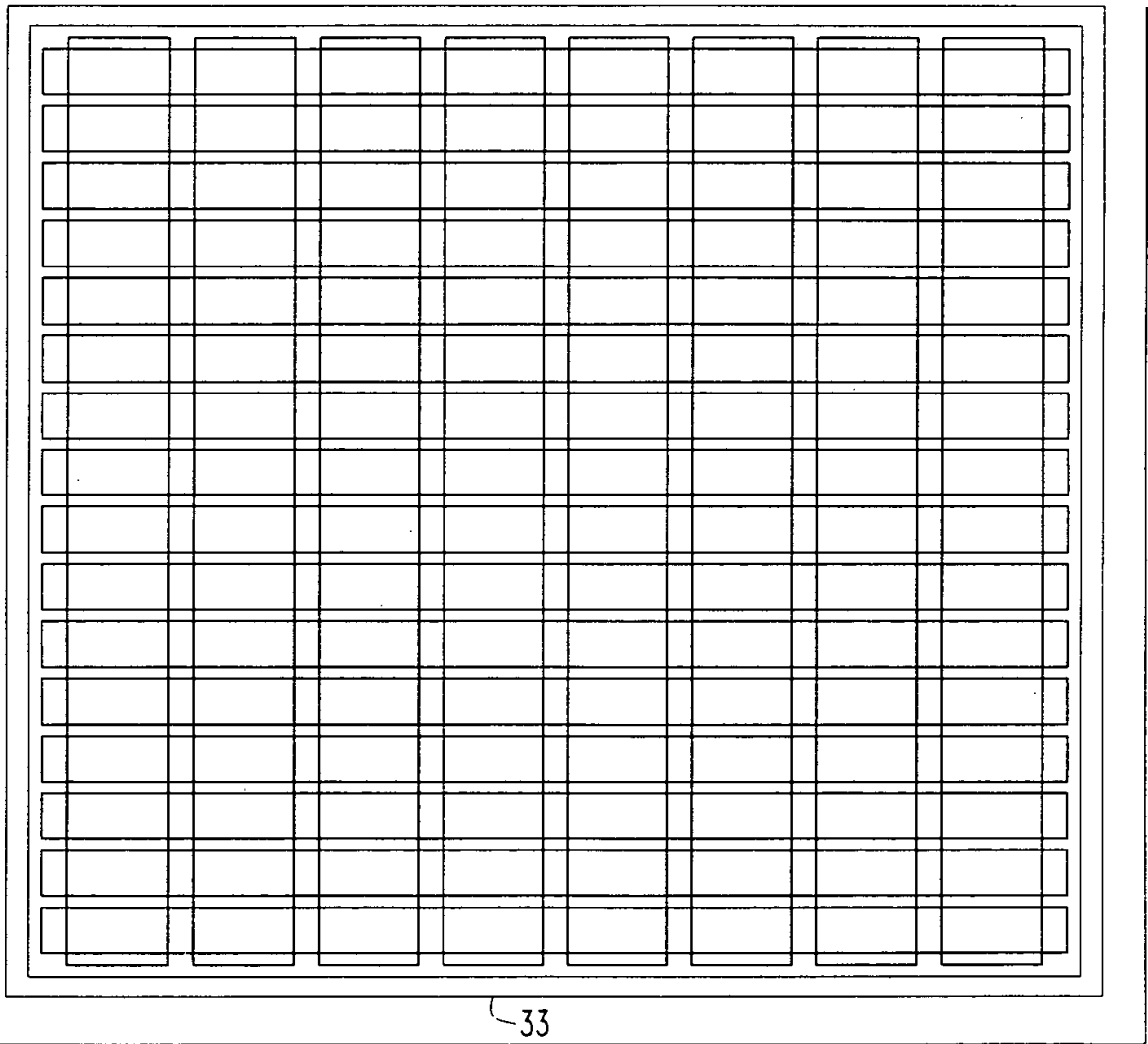
TO
FIG.
33E1



31

FIG. 33E3

TO FIG. 33E4



TO FIG. 33E3

FIG. 33E4

TO
FIG.
33E2

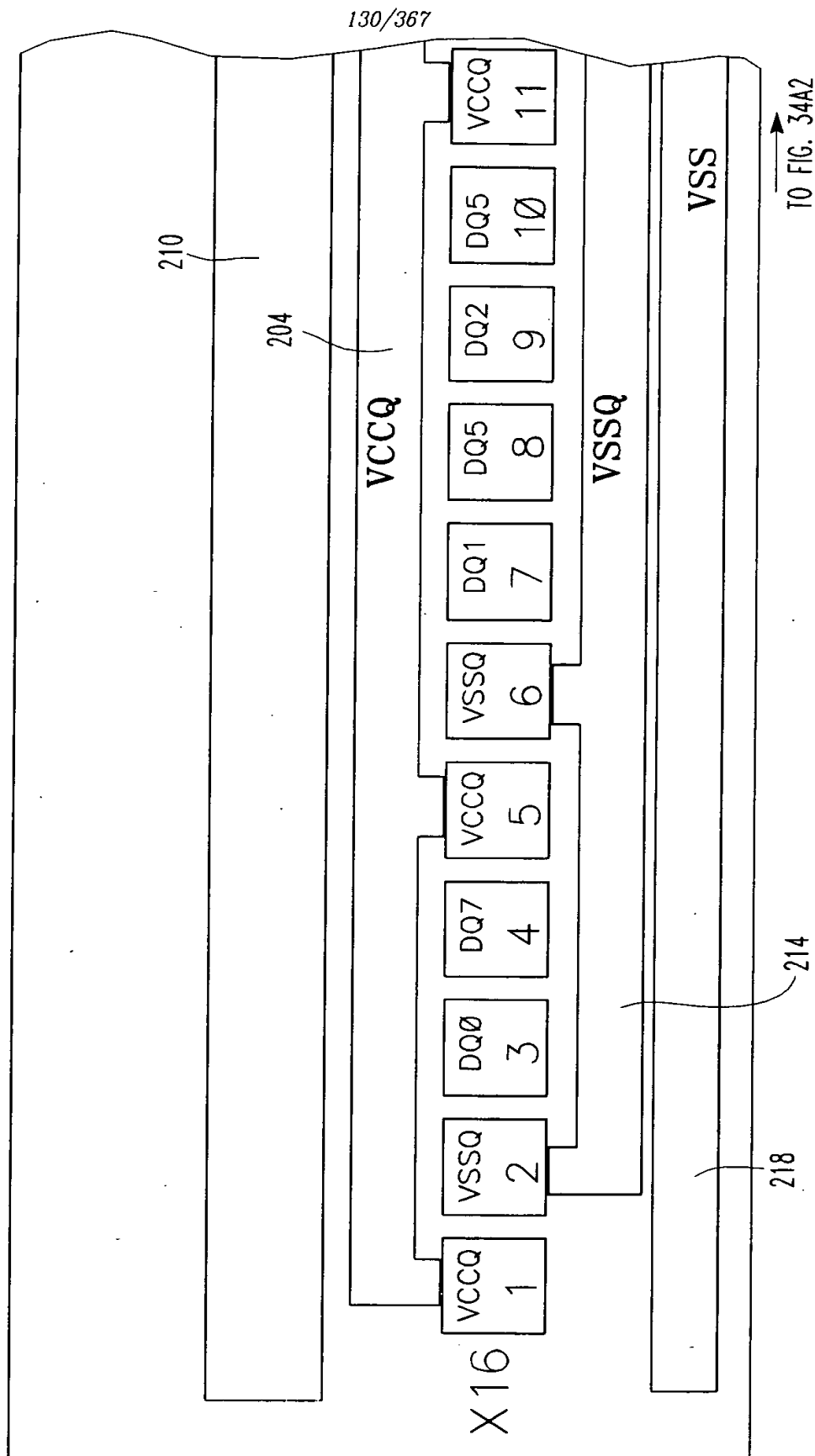
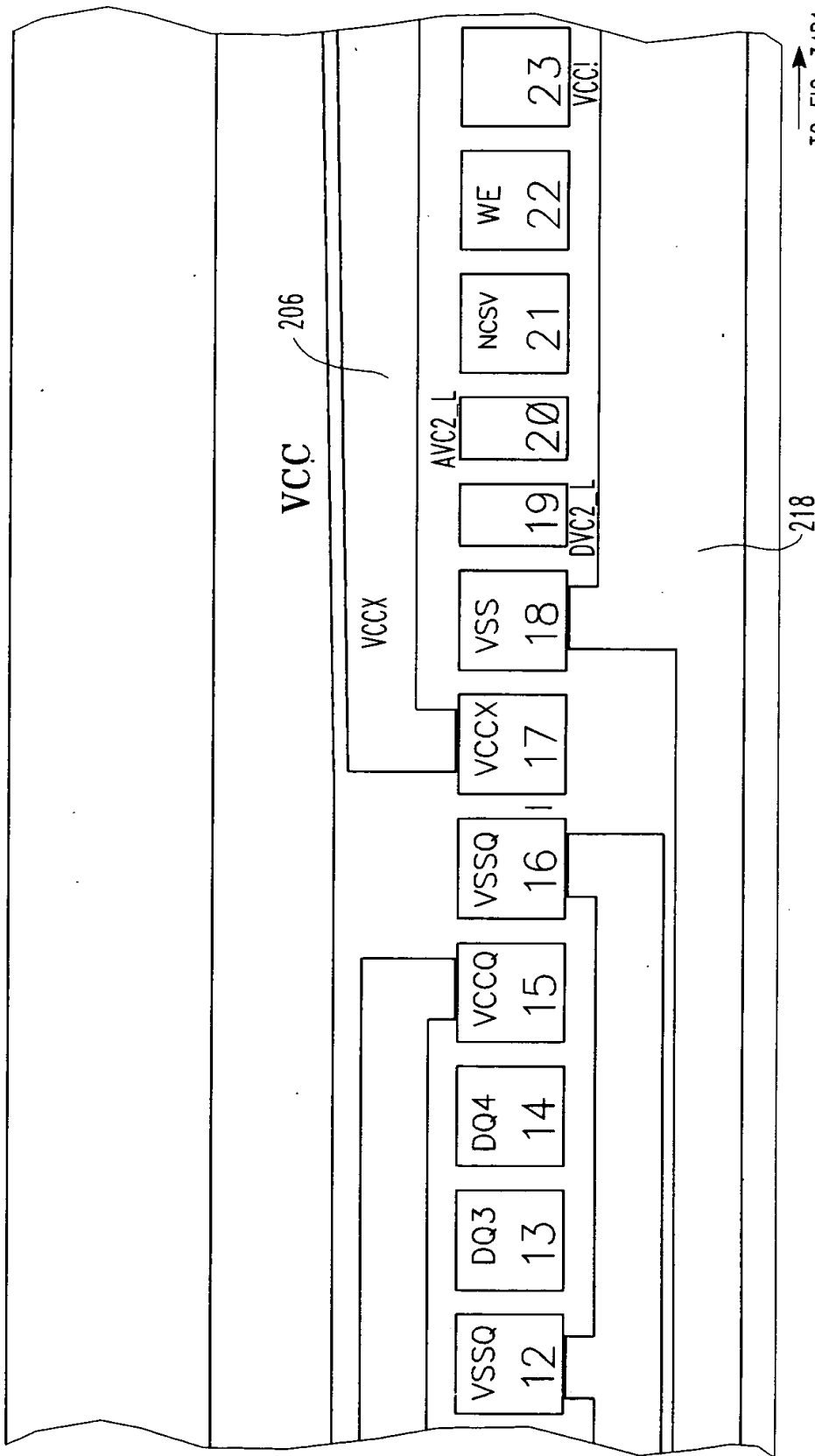


FIG. 34A1

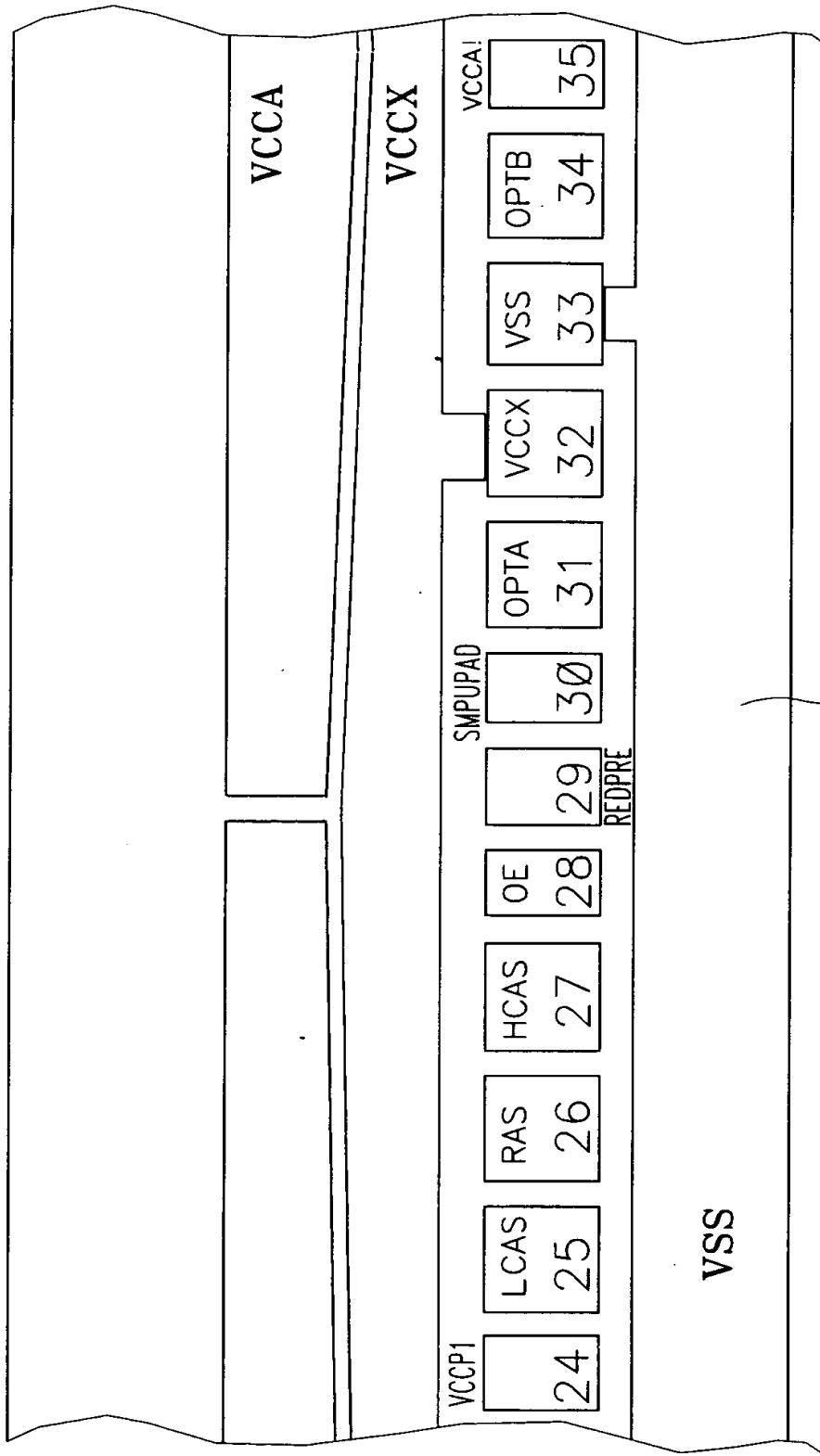
TO FIG. 34A1
←



TO FIG. 34B1
→

FIG. 34A2

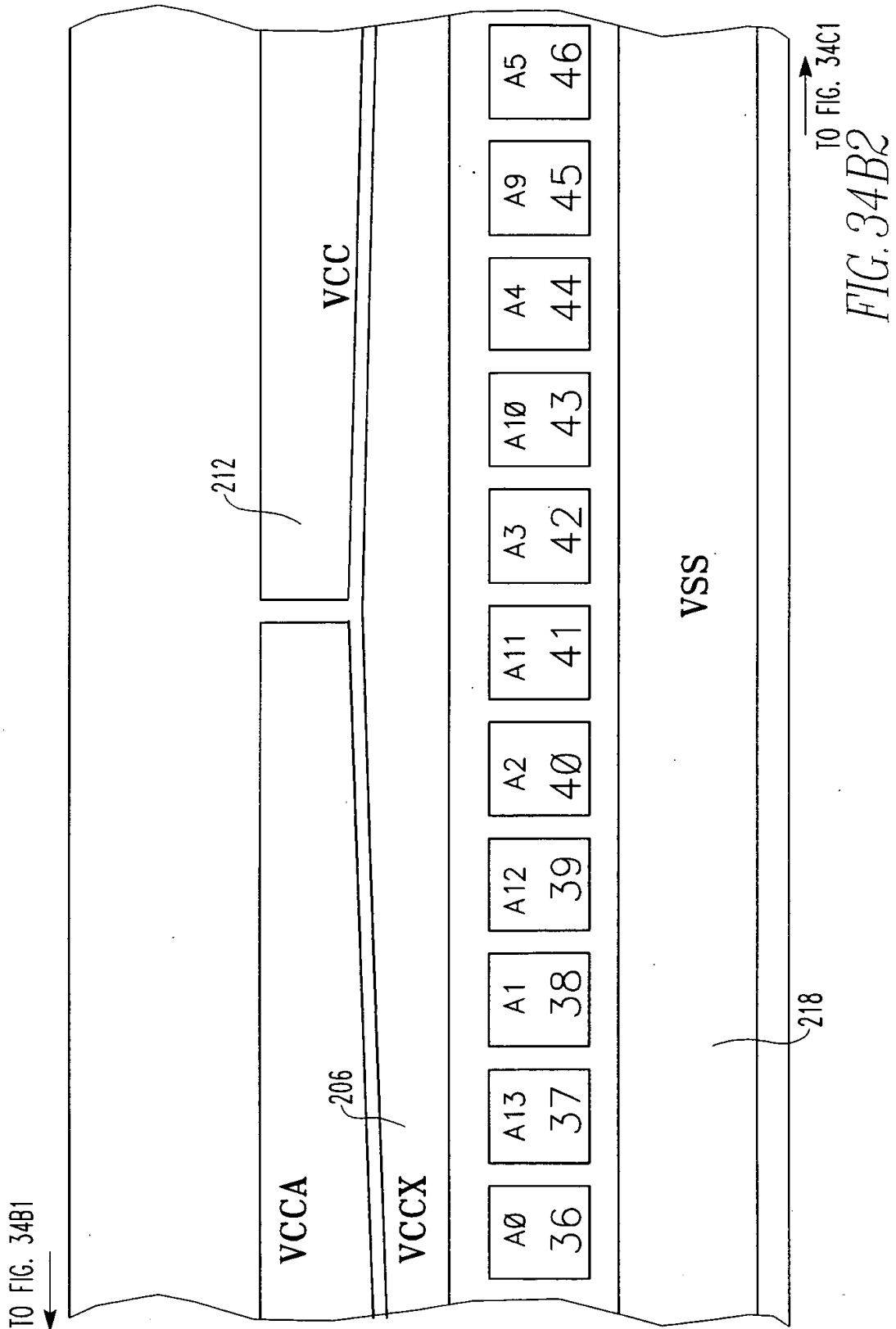
TO FIG. 34A2



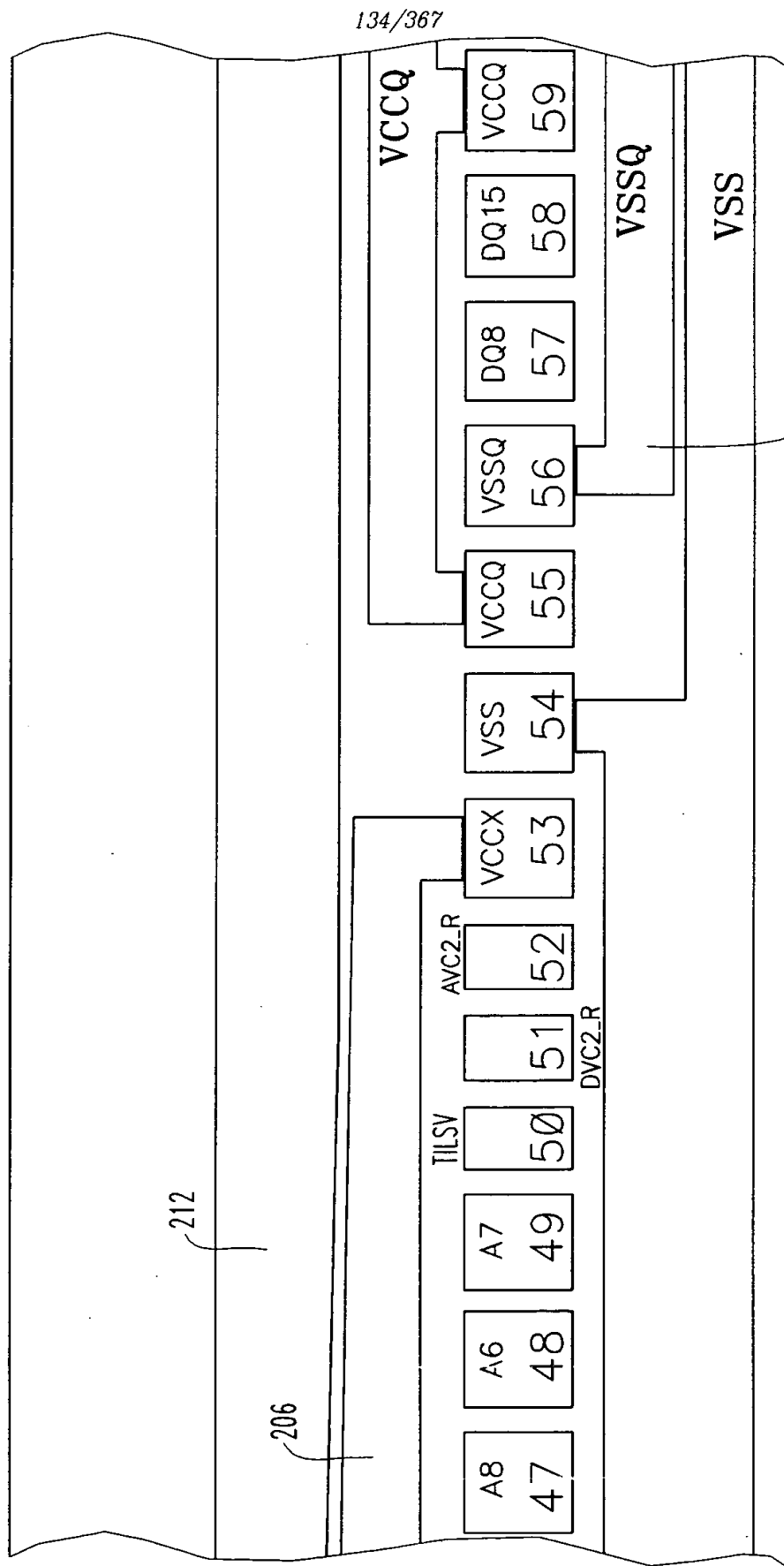
218

TO FIG. 34B2

FIG. 34B1



TO FIG. 34B2



TO FIG. 34C2

FIG. 34C1

TO FIG. 34C1
←

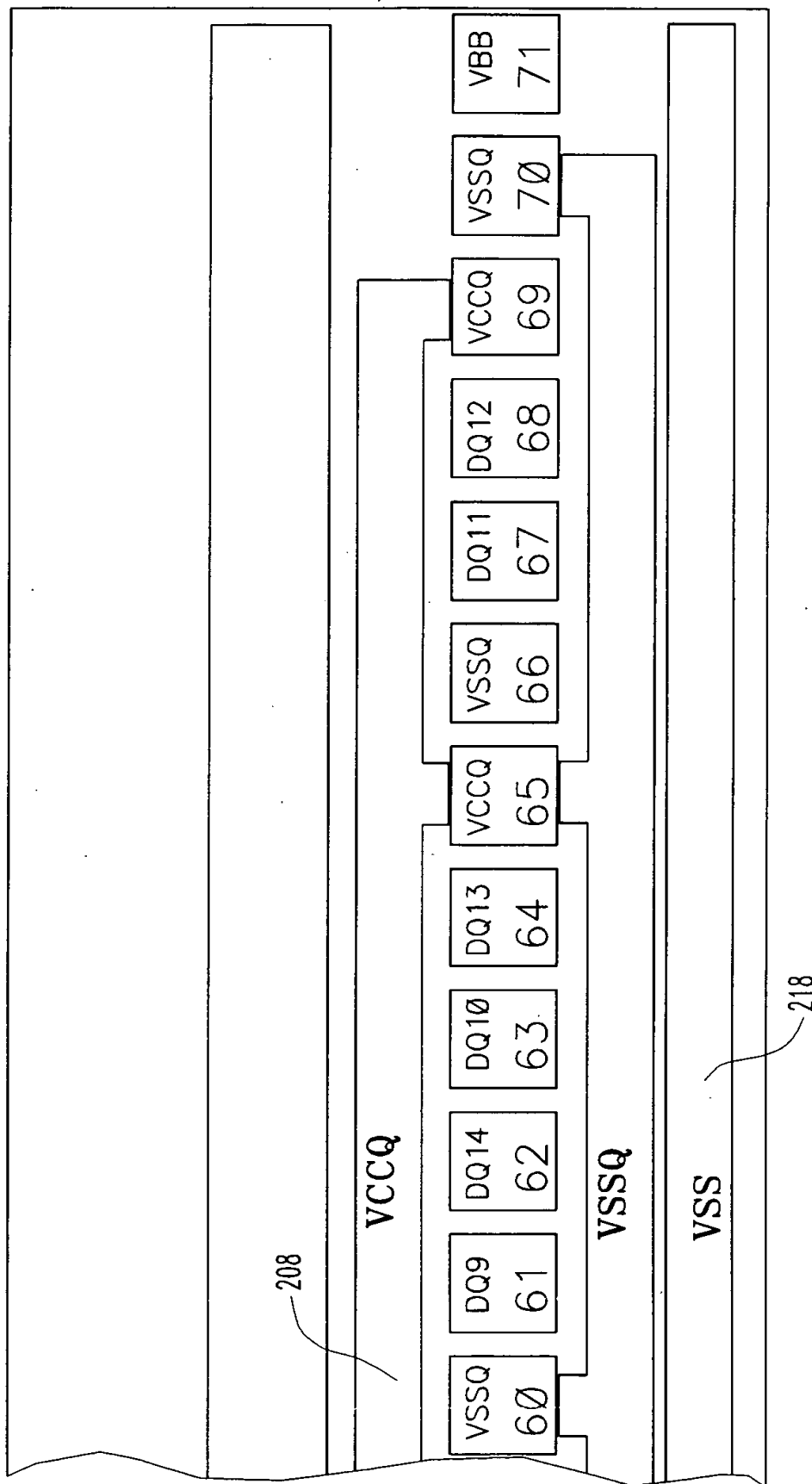


FIG. 34C2

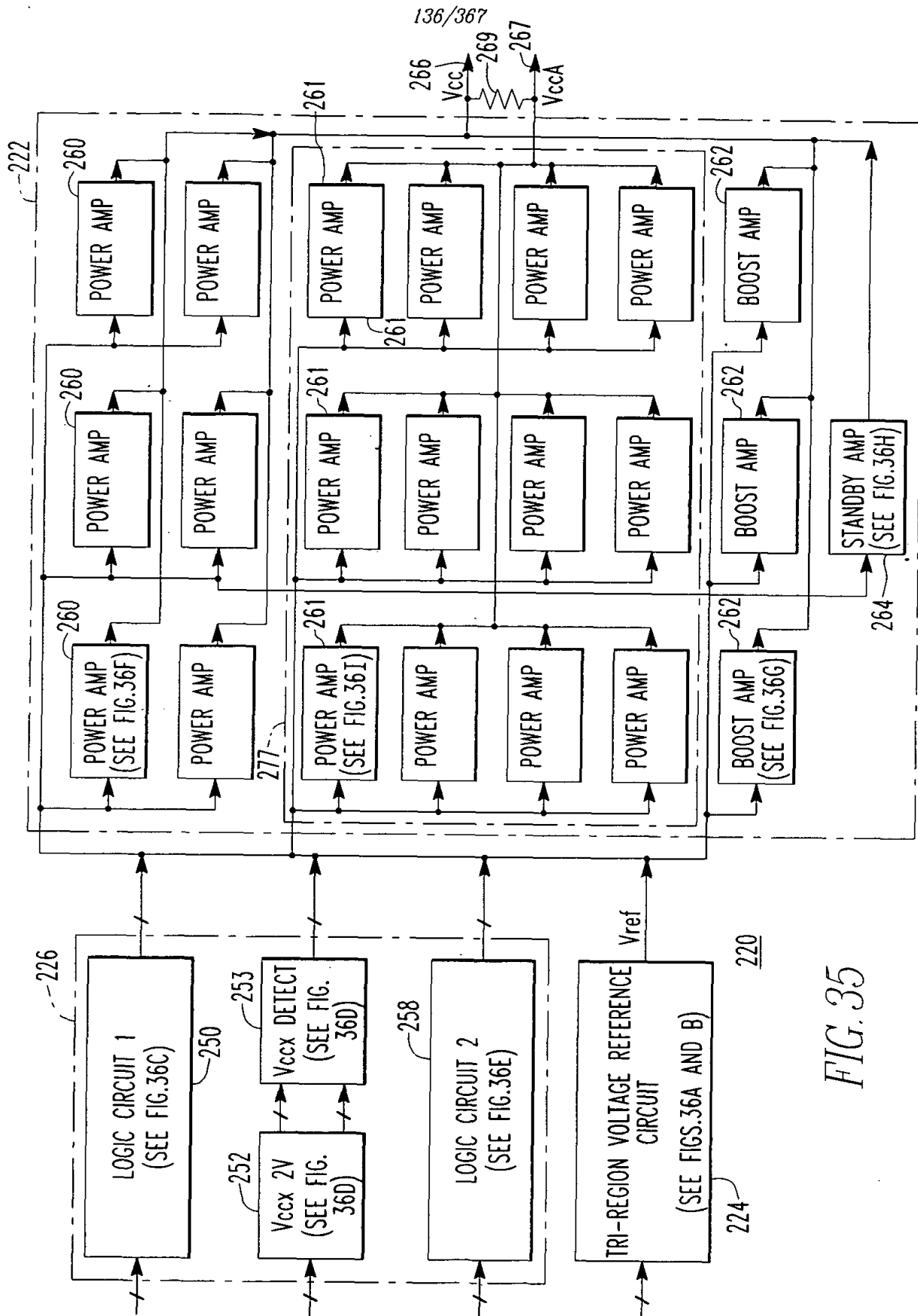


FIG. 35

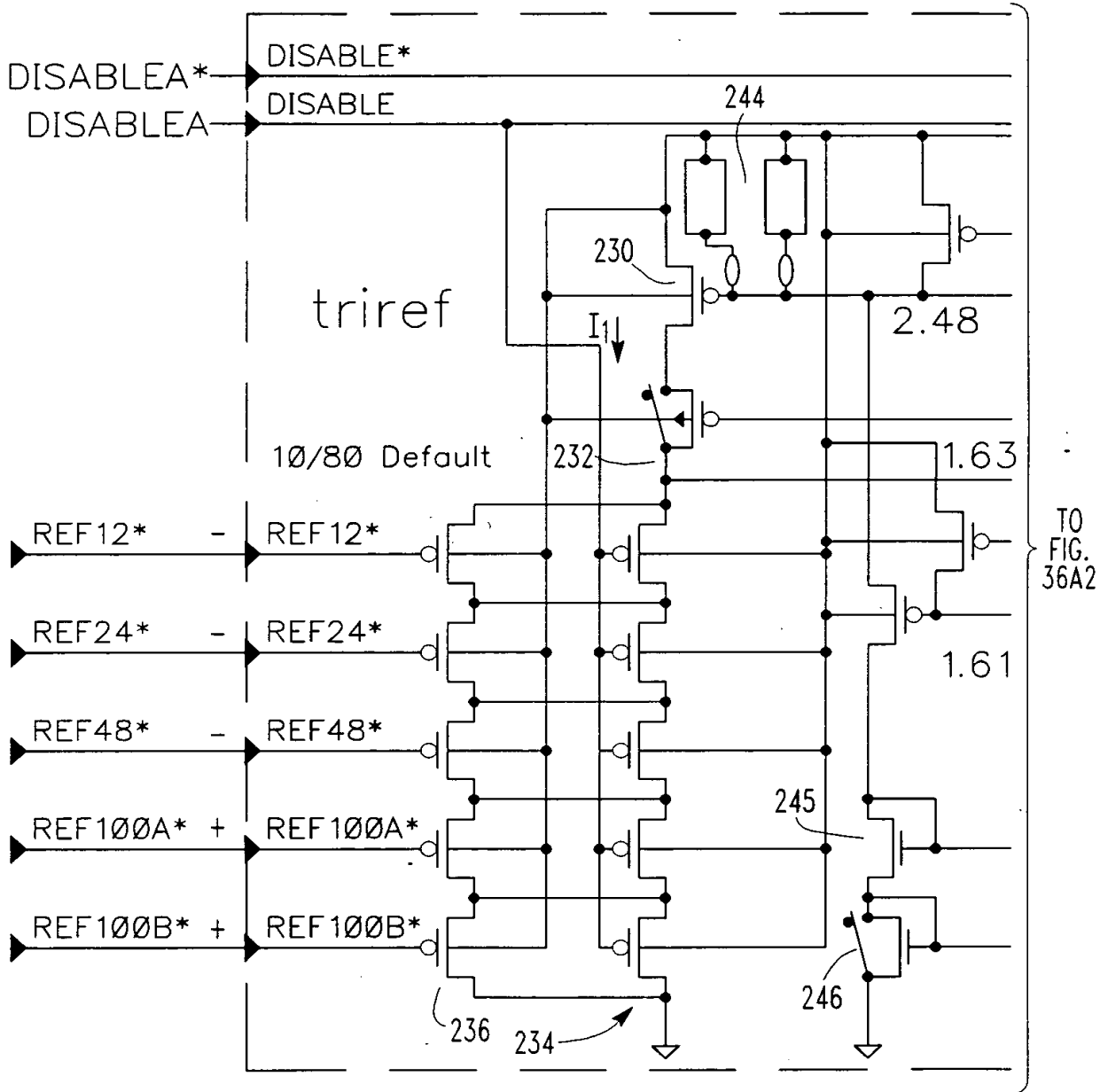


FIG. 36A1

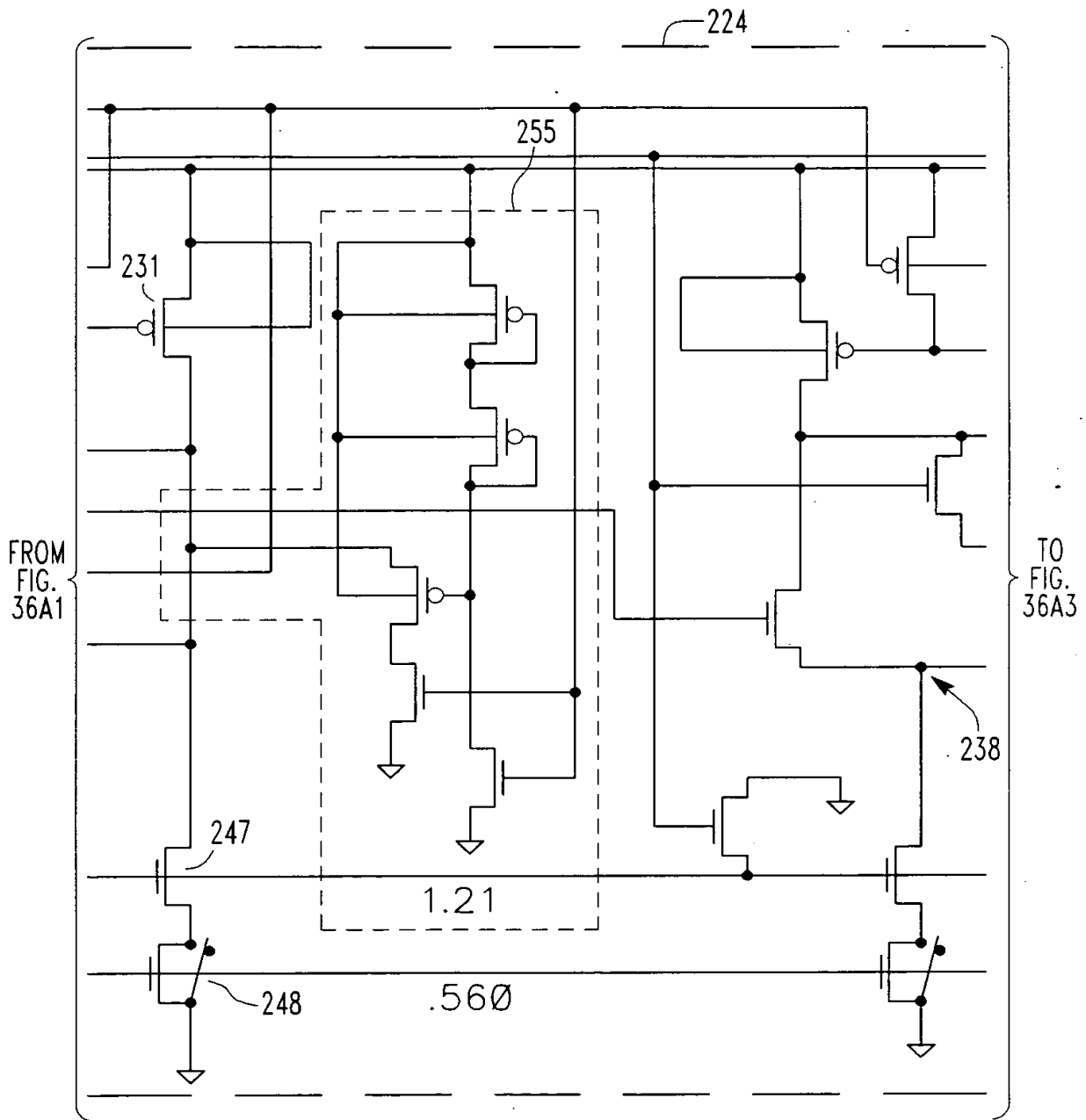


FIG. 36A2

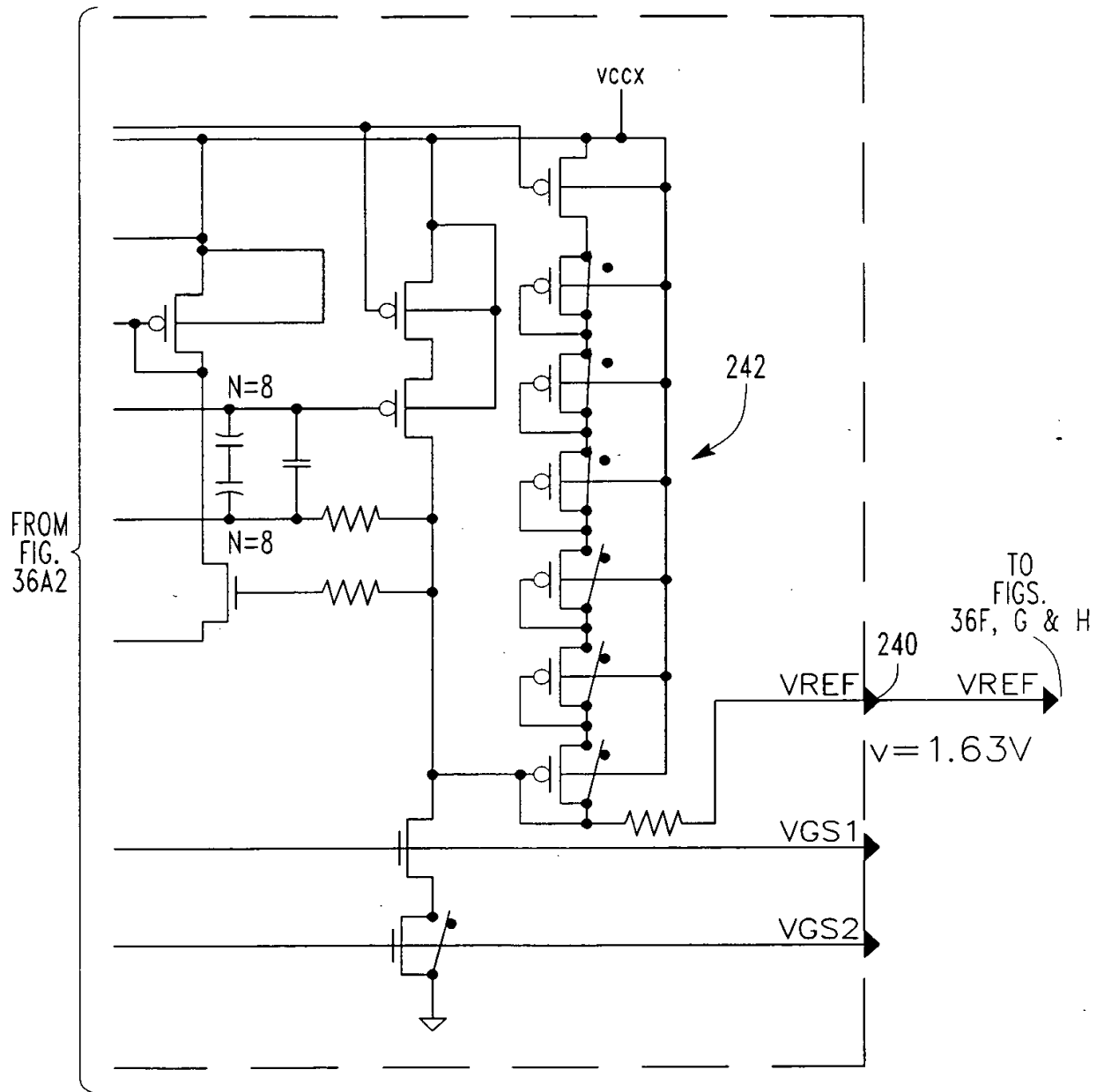


FIG. 36A3

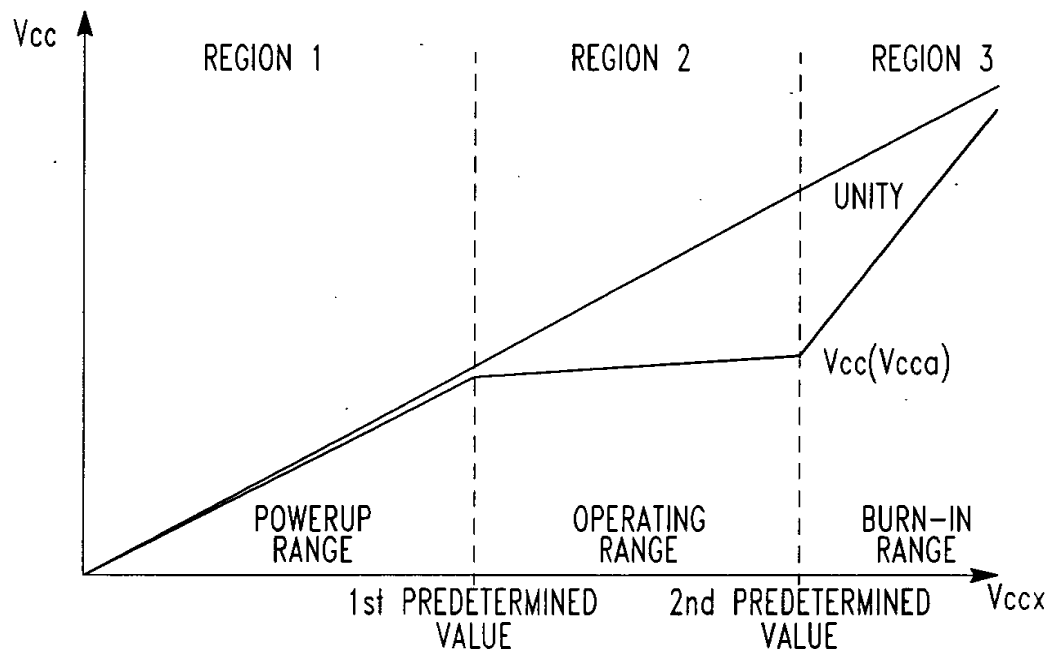


FIG. 36B

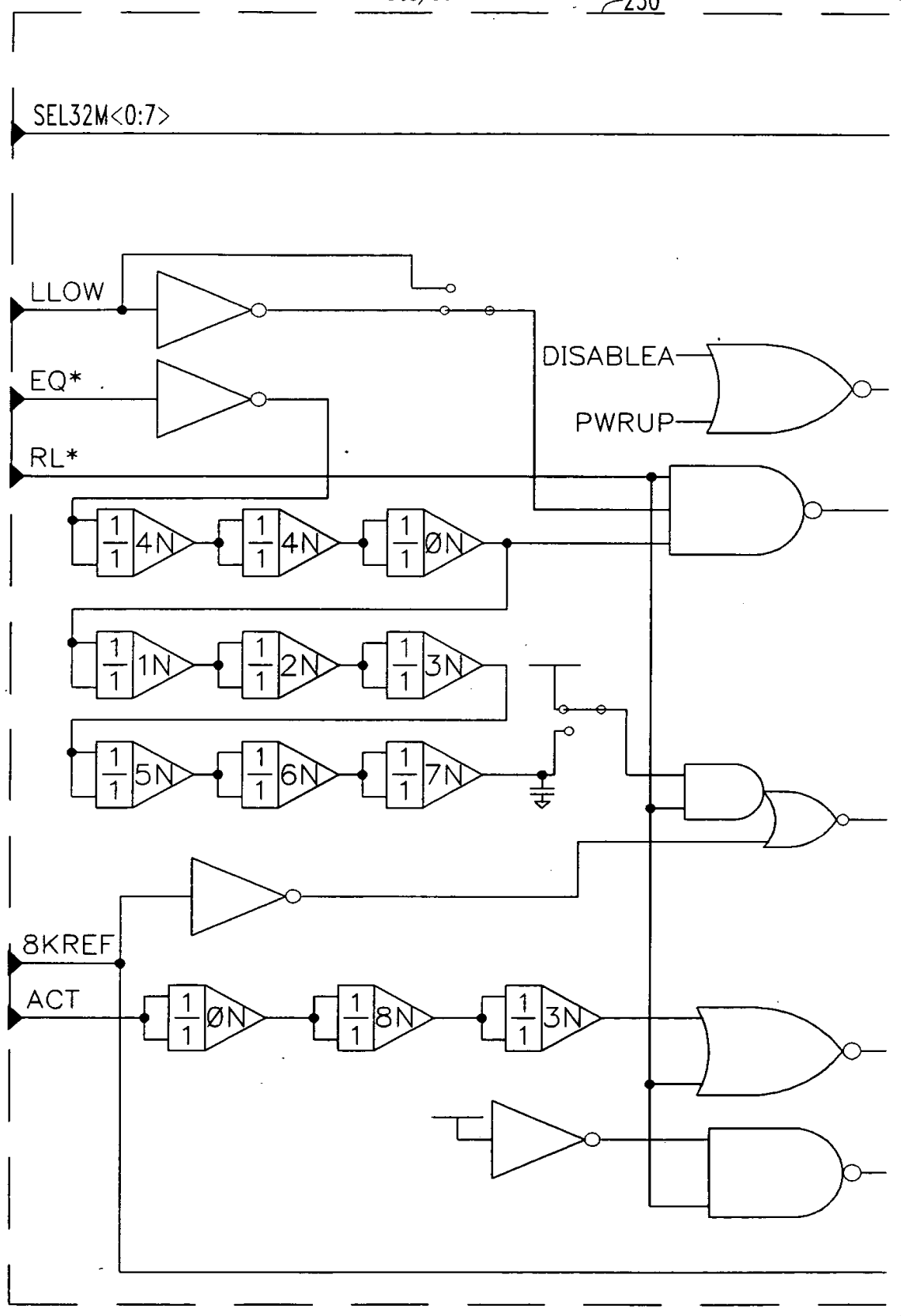
TO
FIG.
36C2

FIG. 36C1

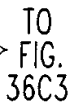
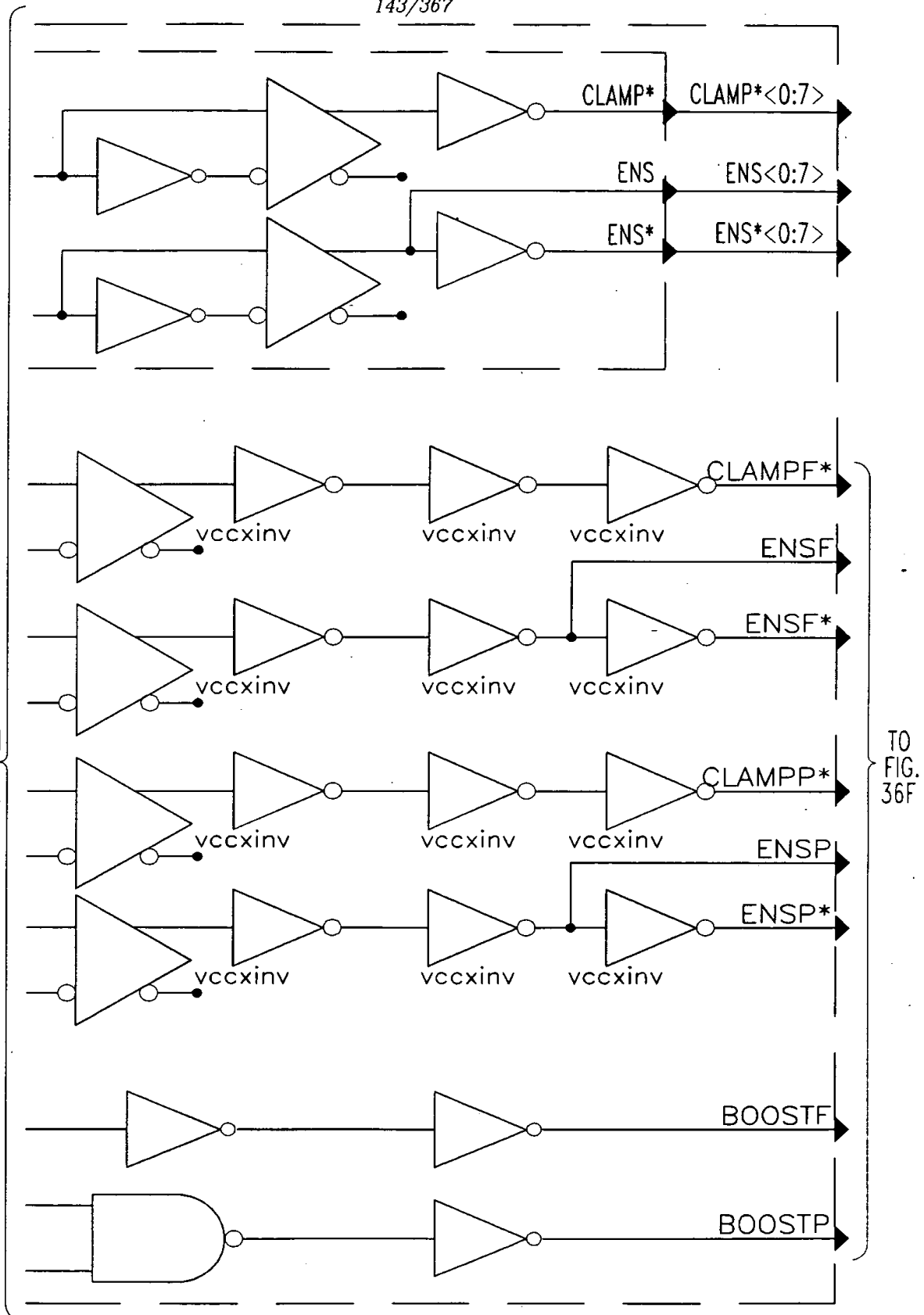


FIG. 36C2



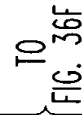
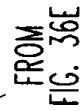


FIG. 36D

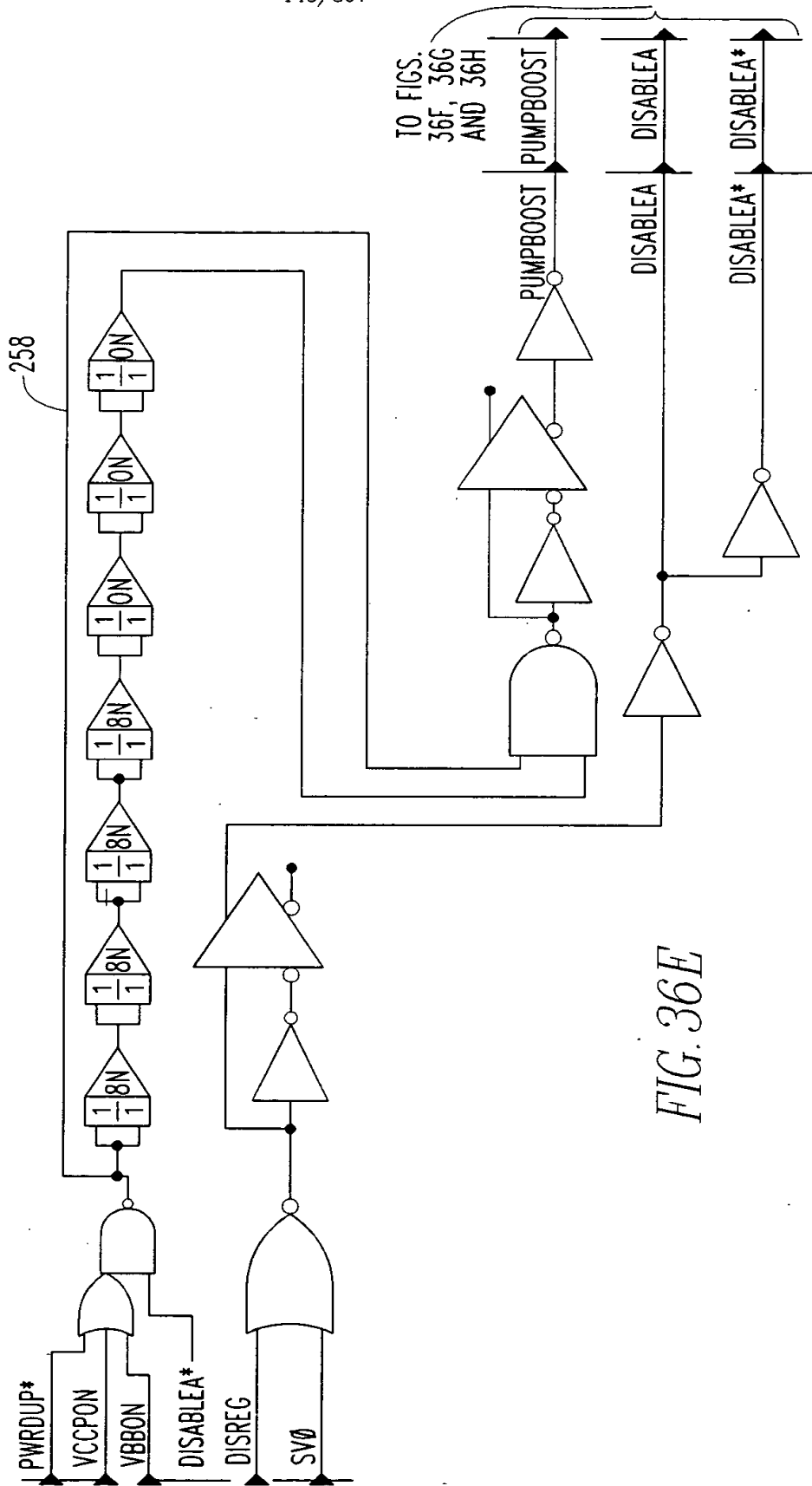


FIG. 36E

FIG. 36E

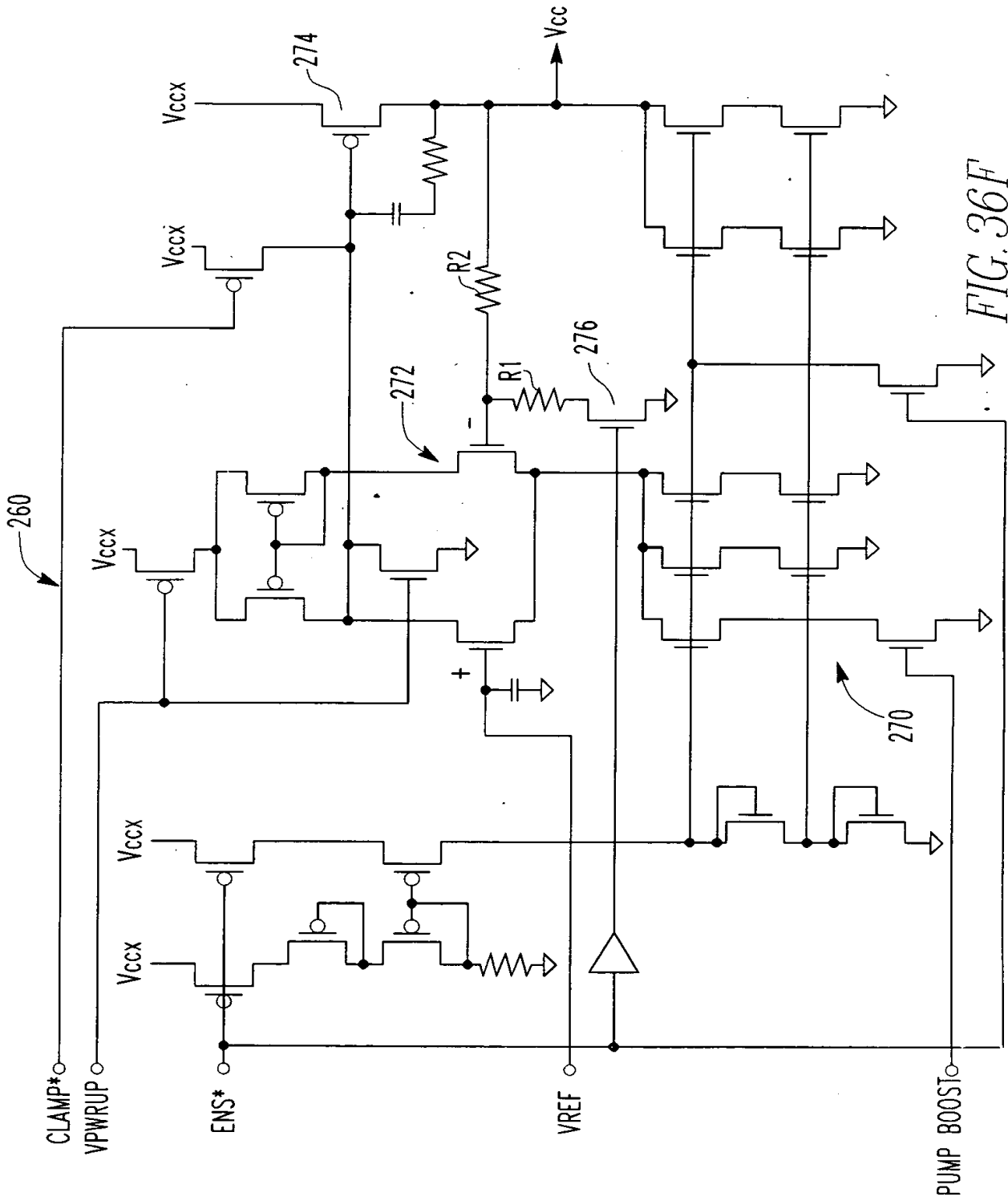


FIG. 36F

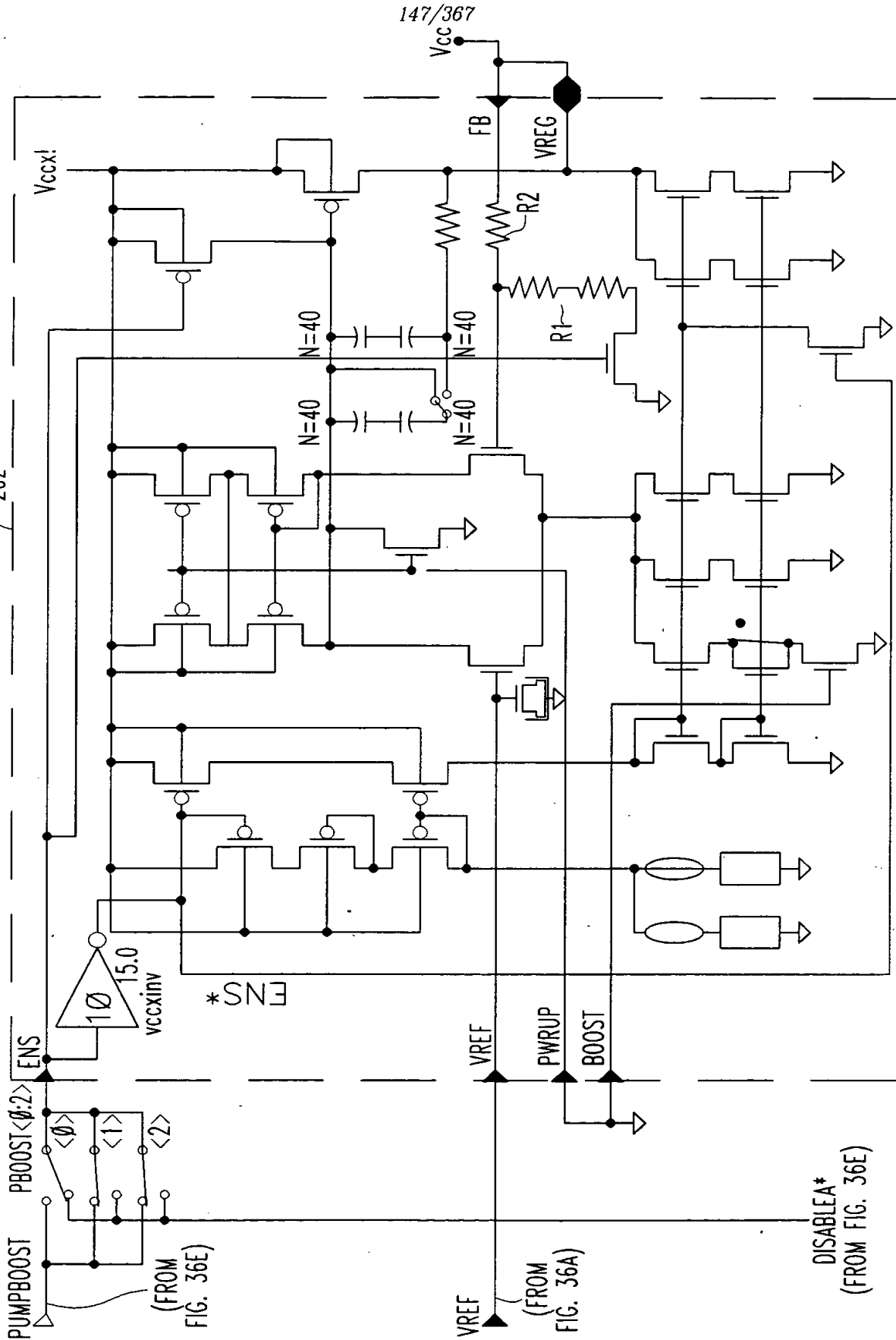


FIG. 36G

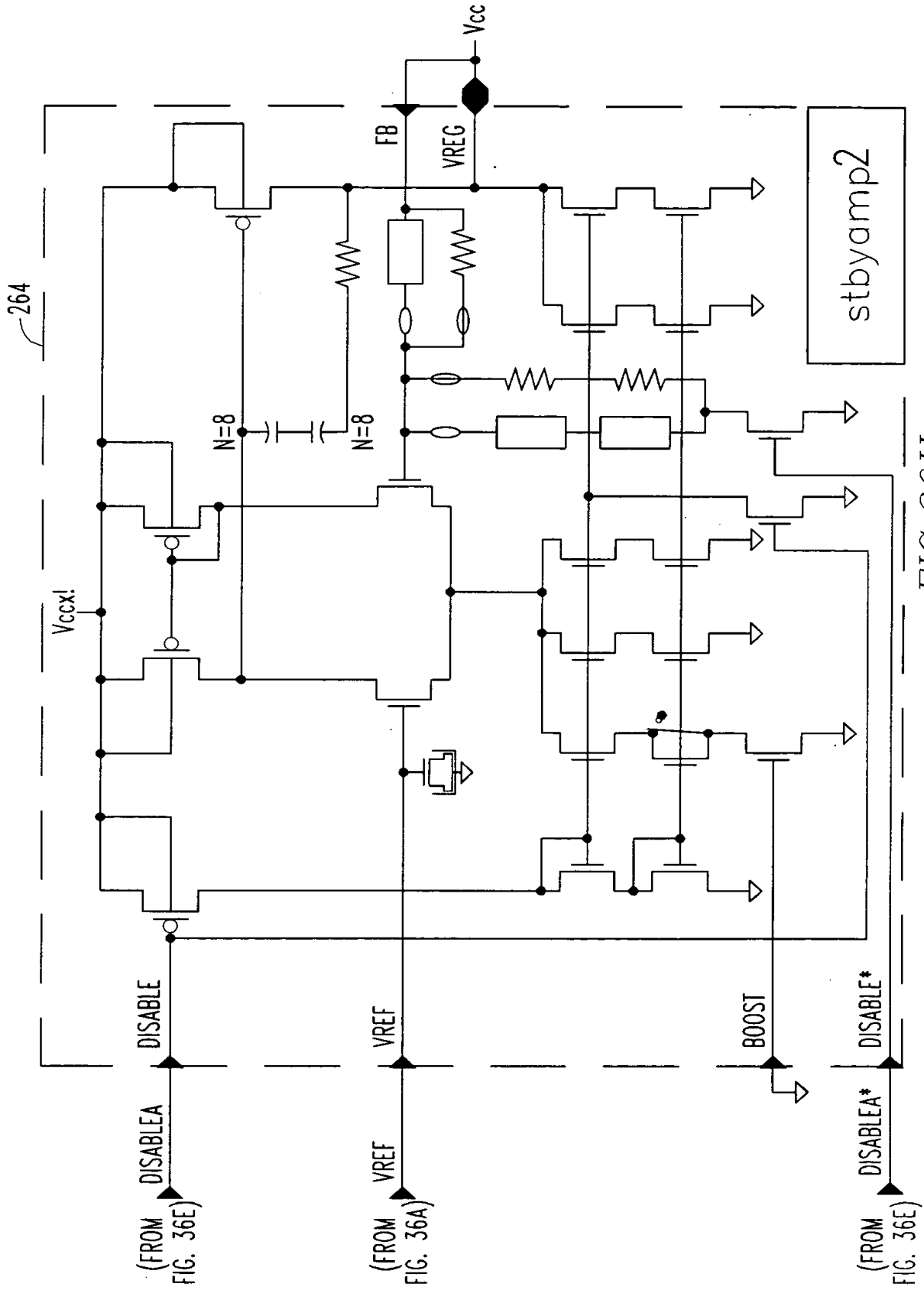


FIG. 36H

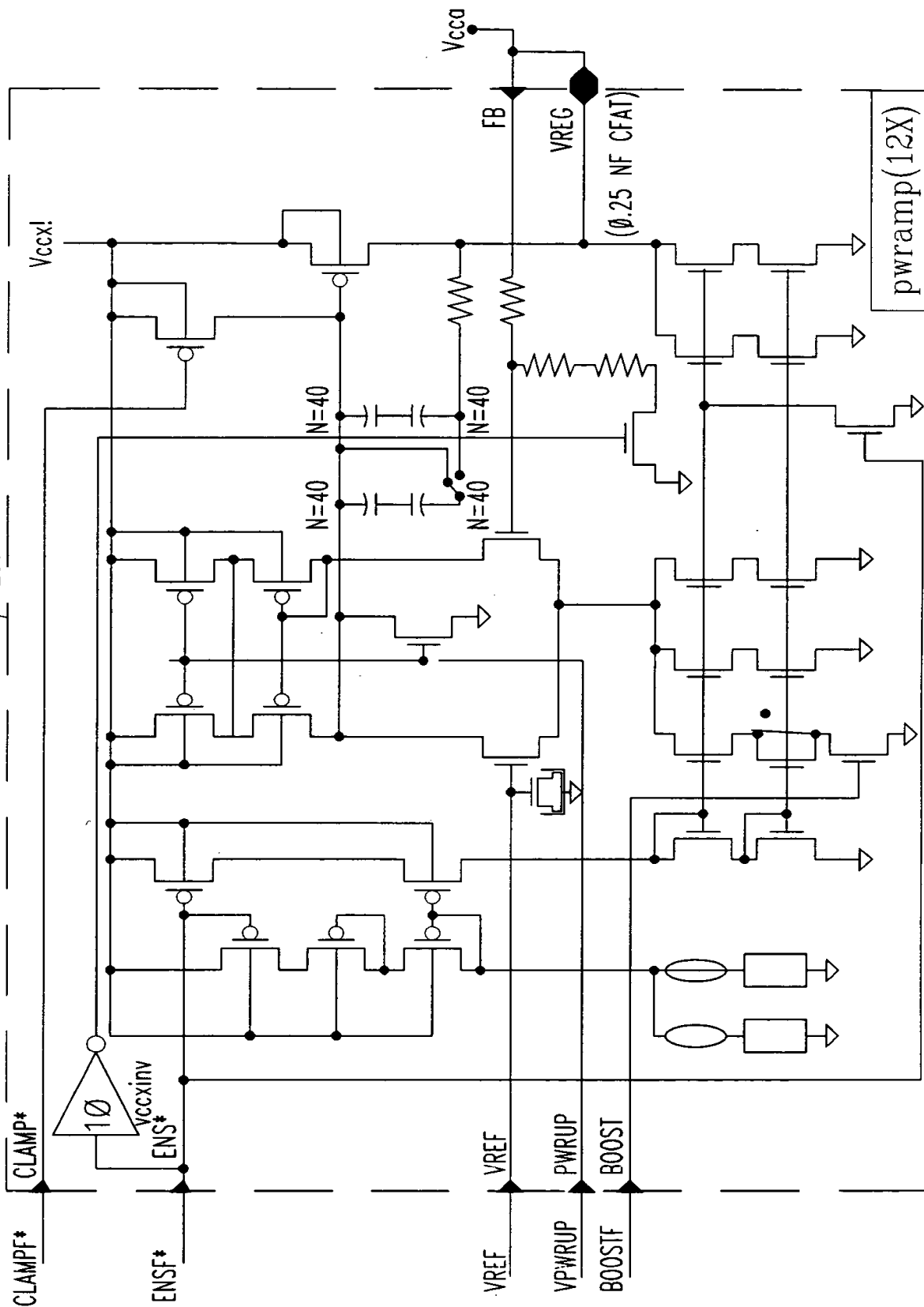


FIG. 361

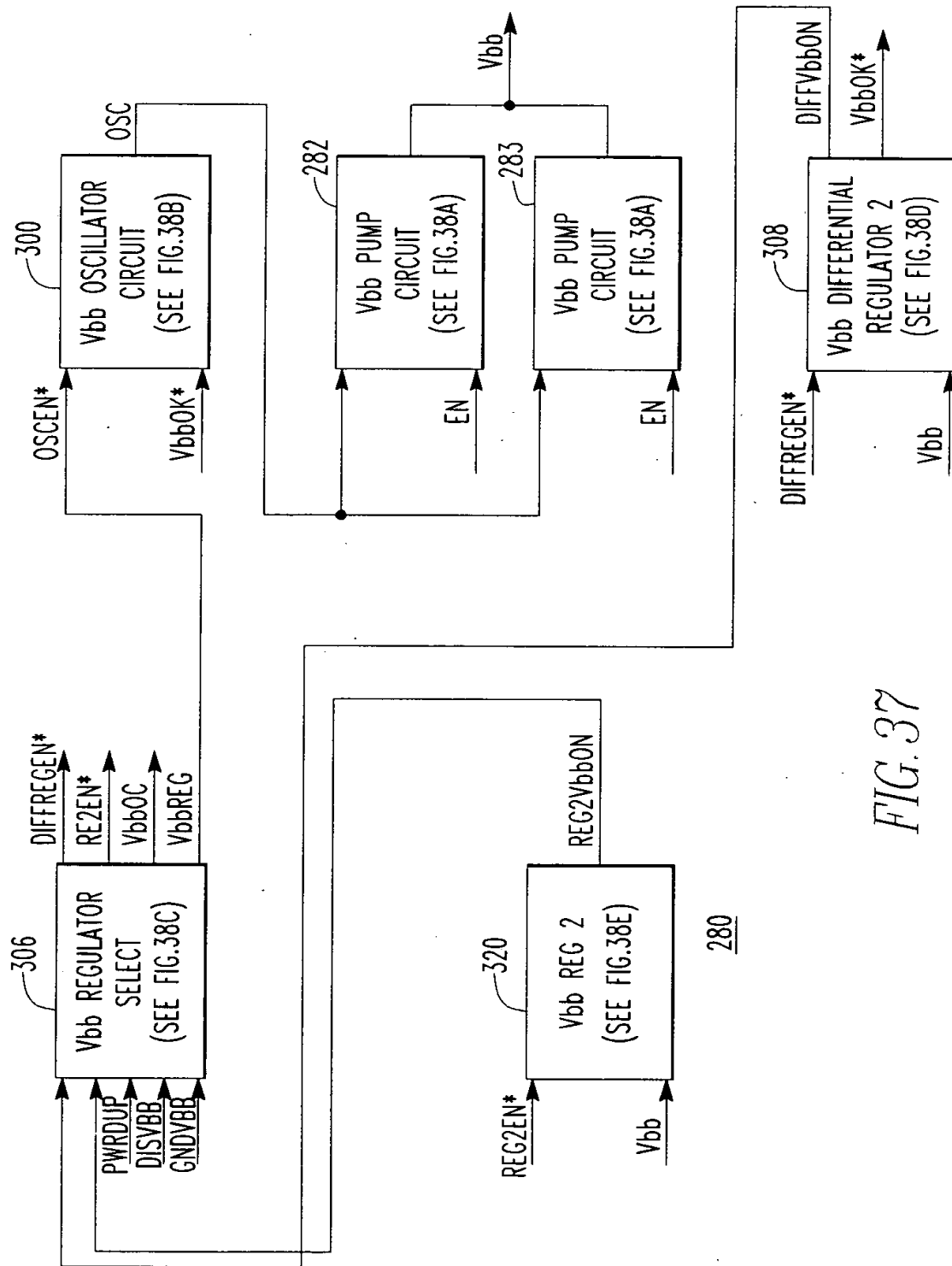


FIG. 37

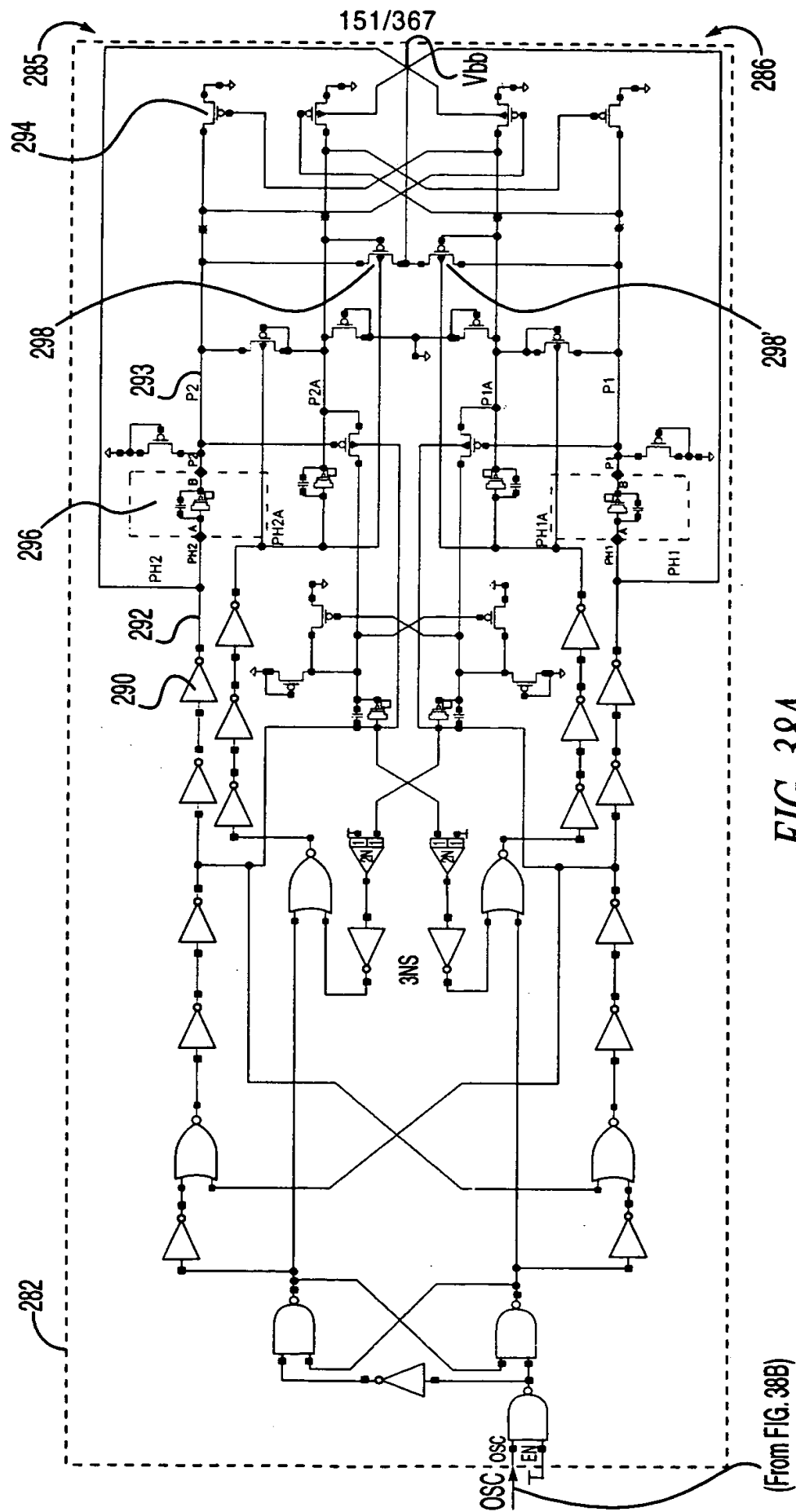


FIG. 38A

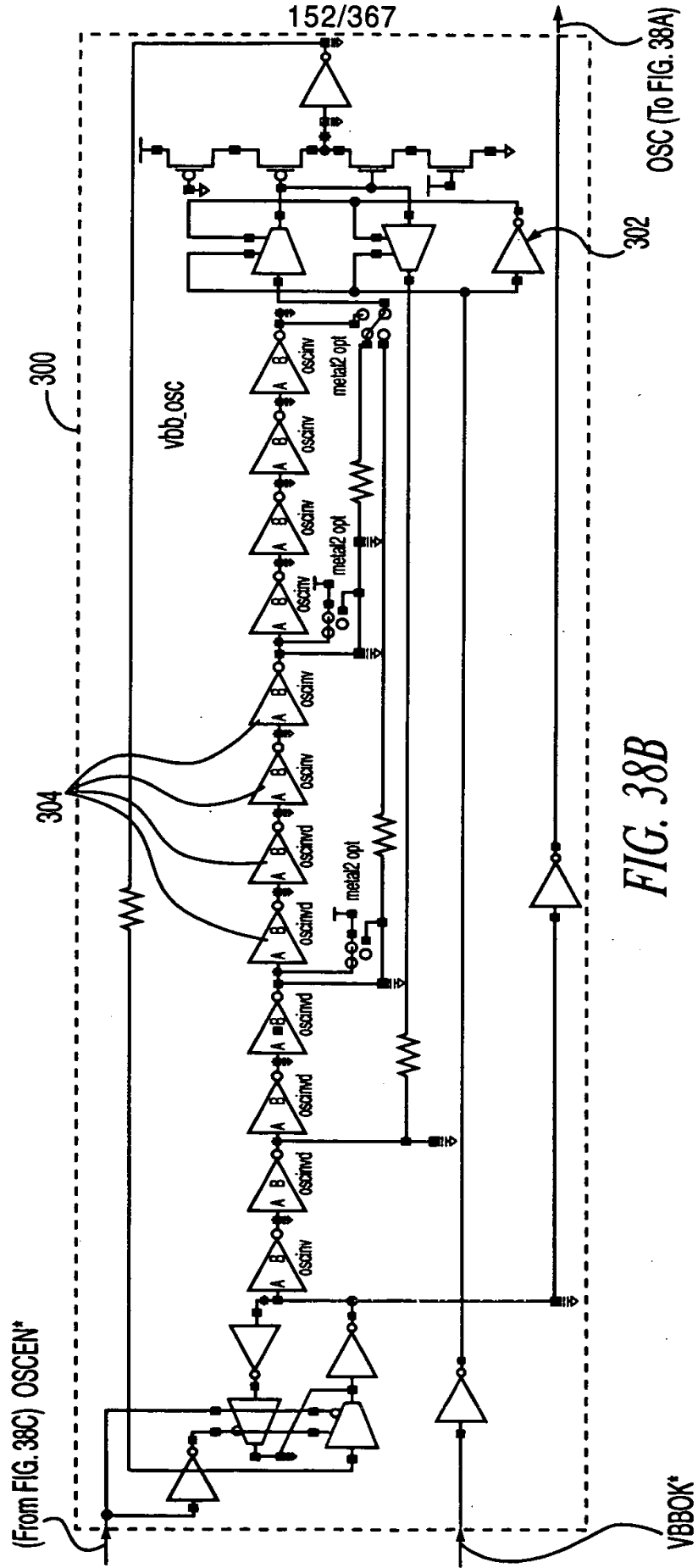
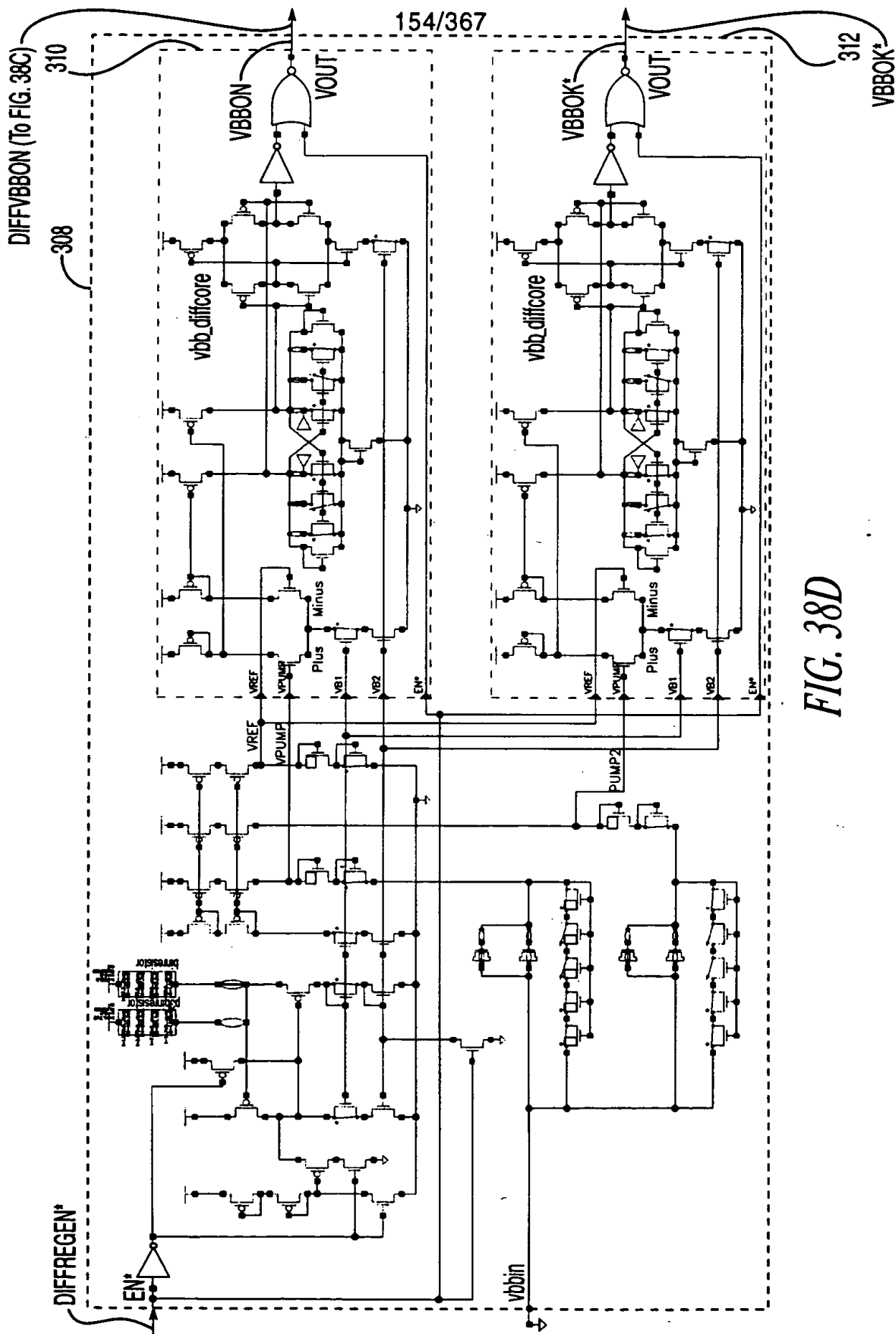




FIG. 38C



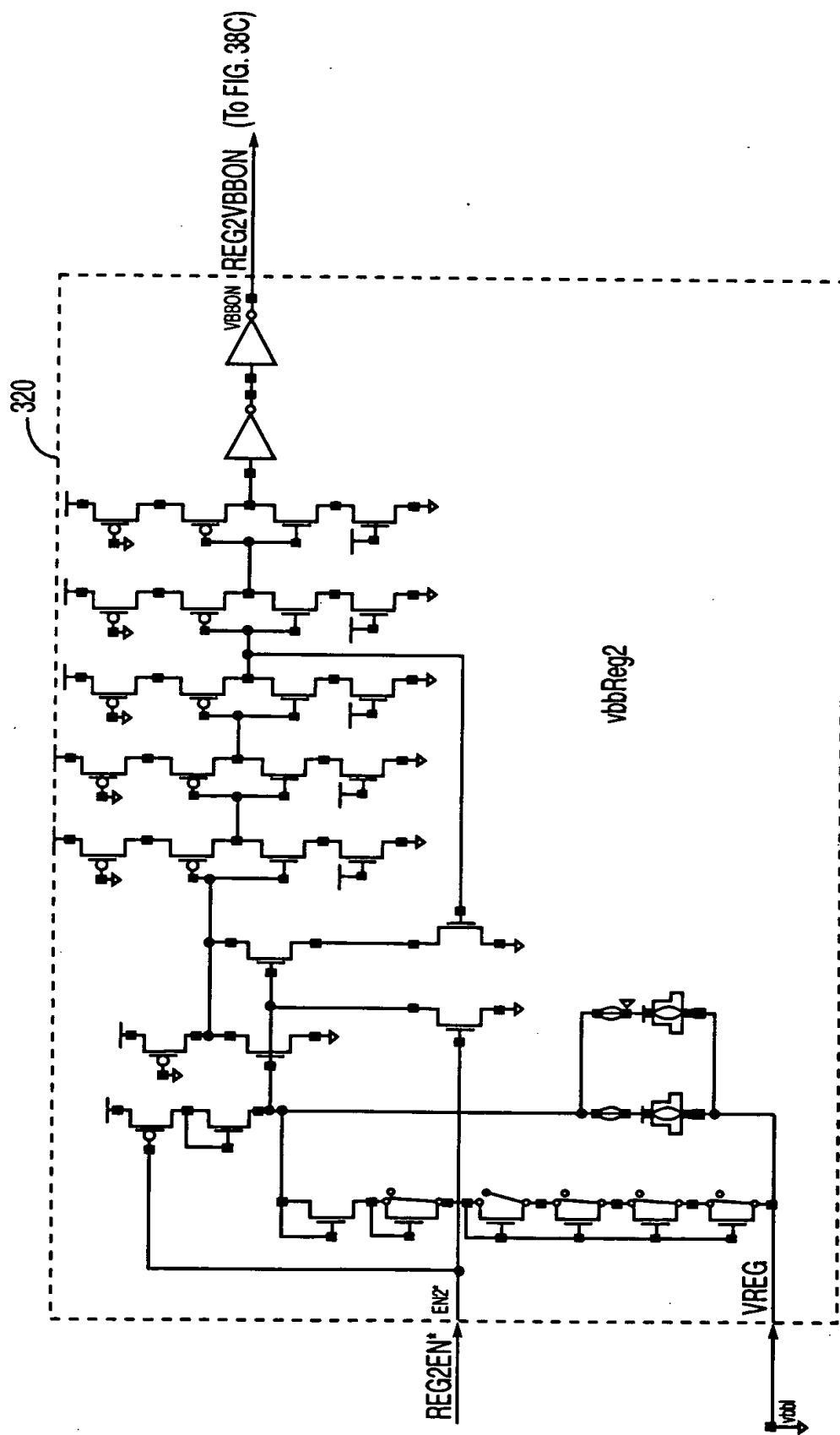


FIG. 38E

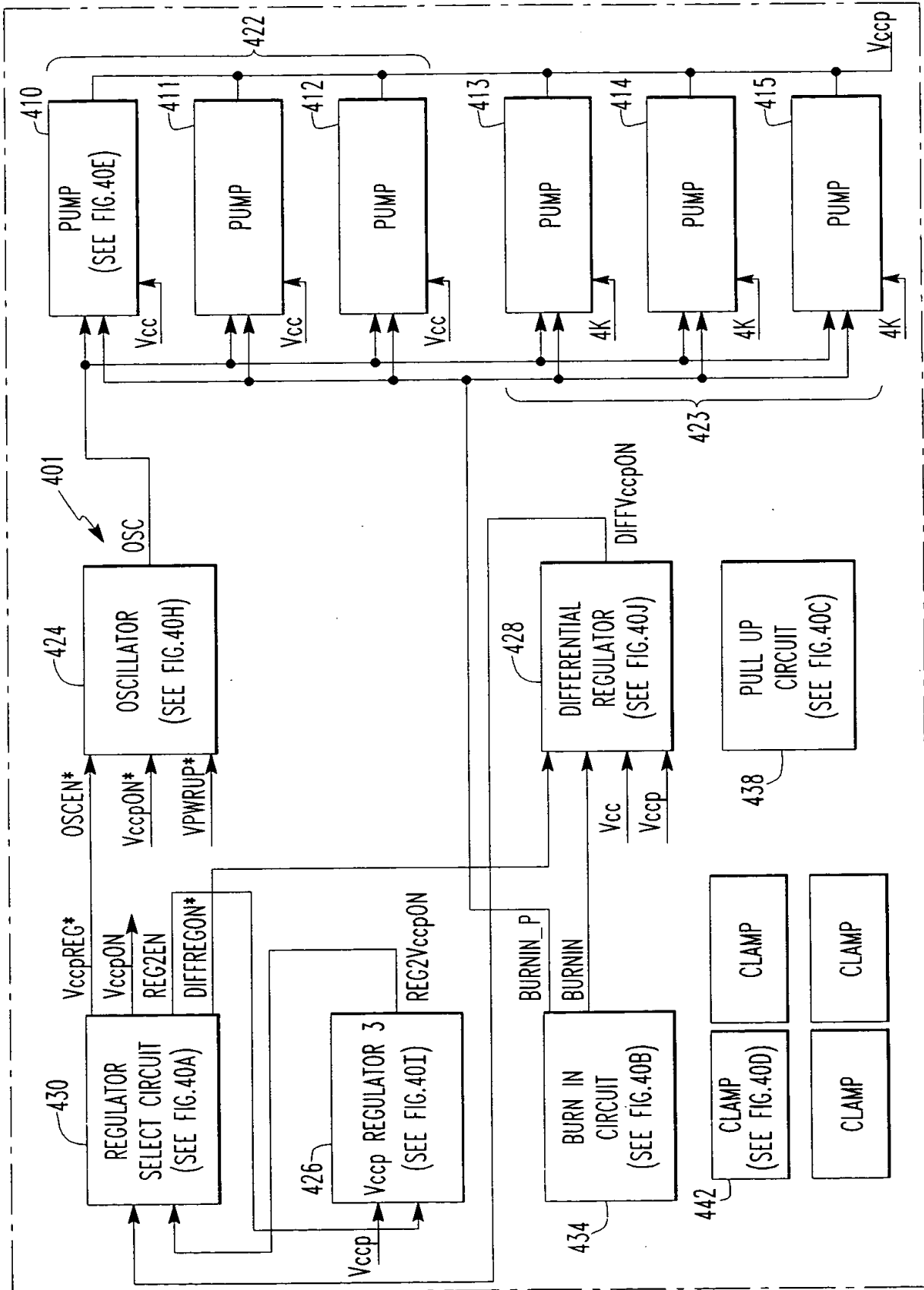


FIG. 39

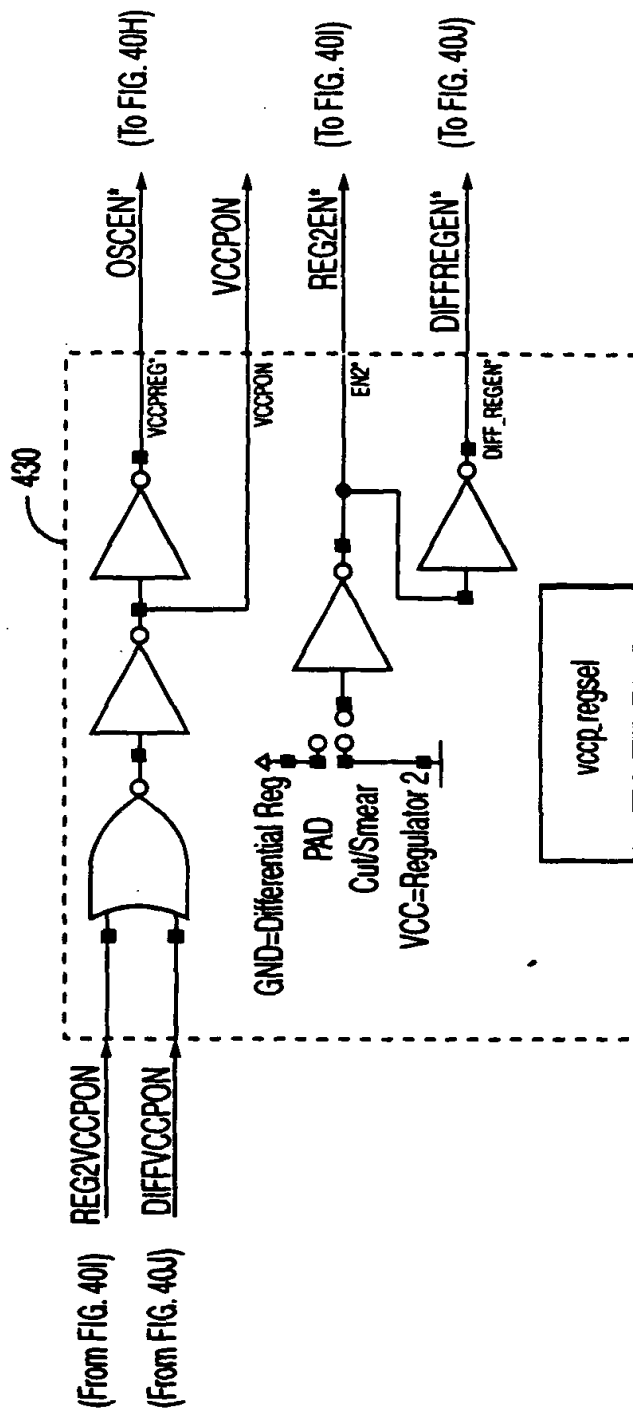


FIG. 40A

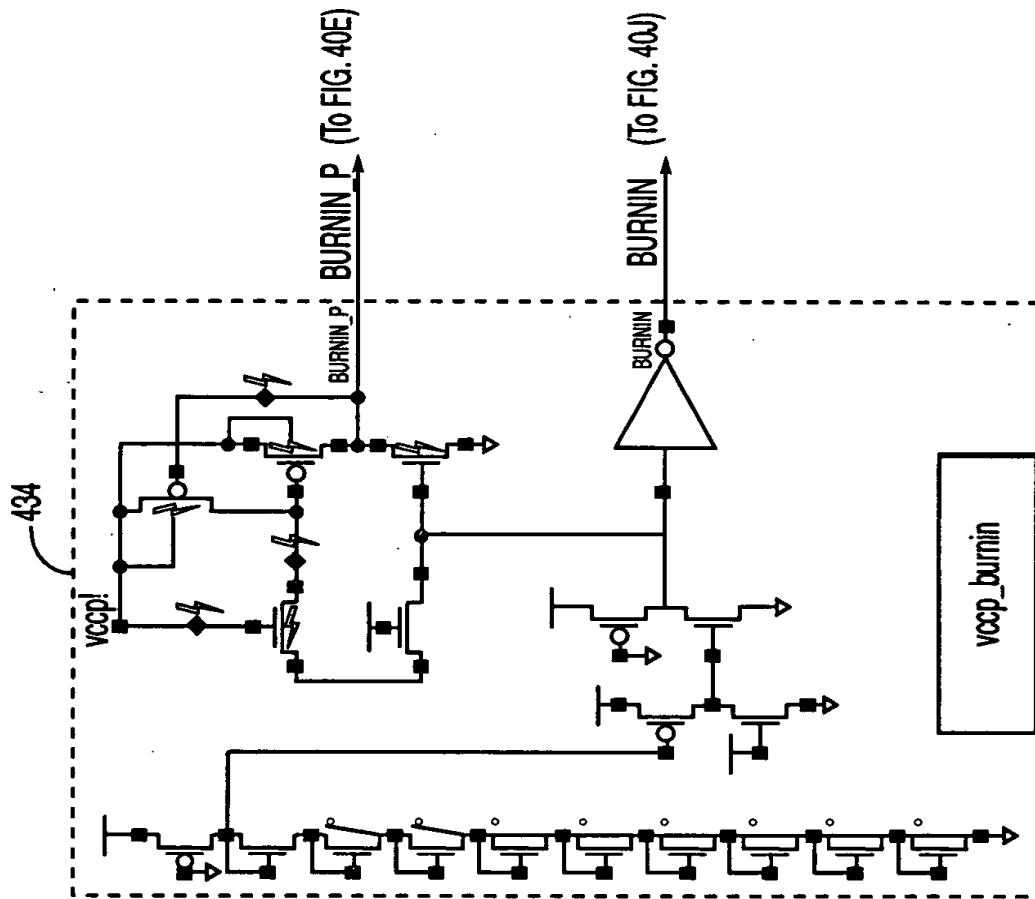


FIG. 40B

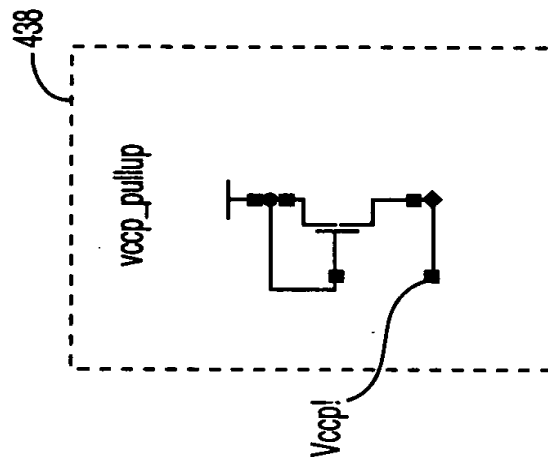


FIG. 40C

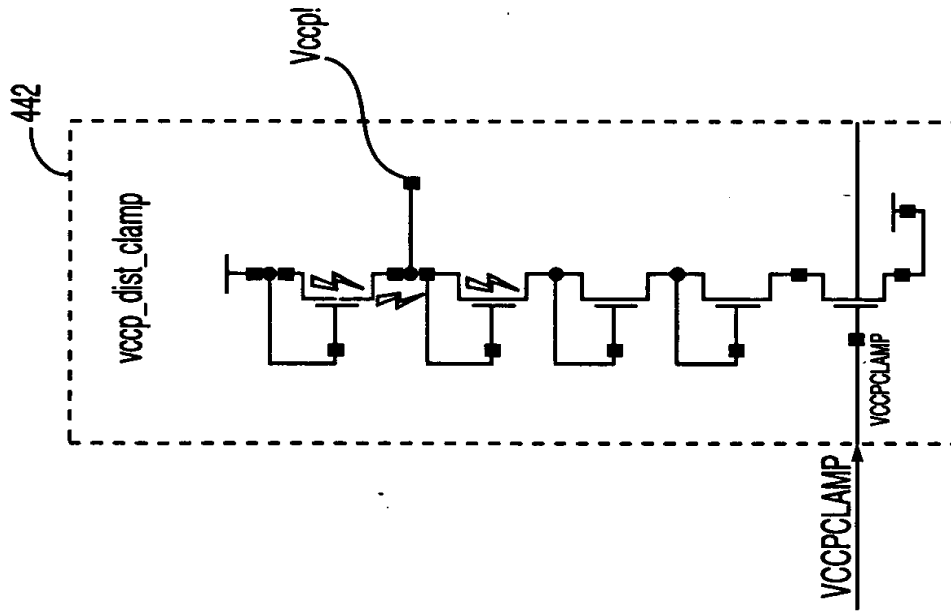


FIG. 40D

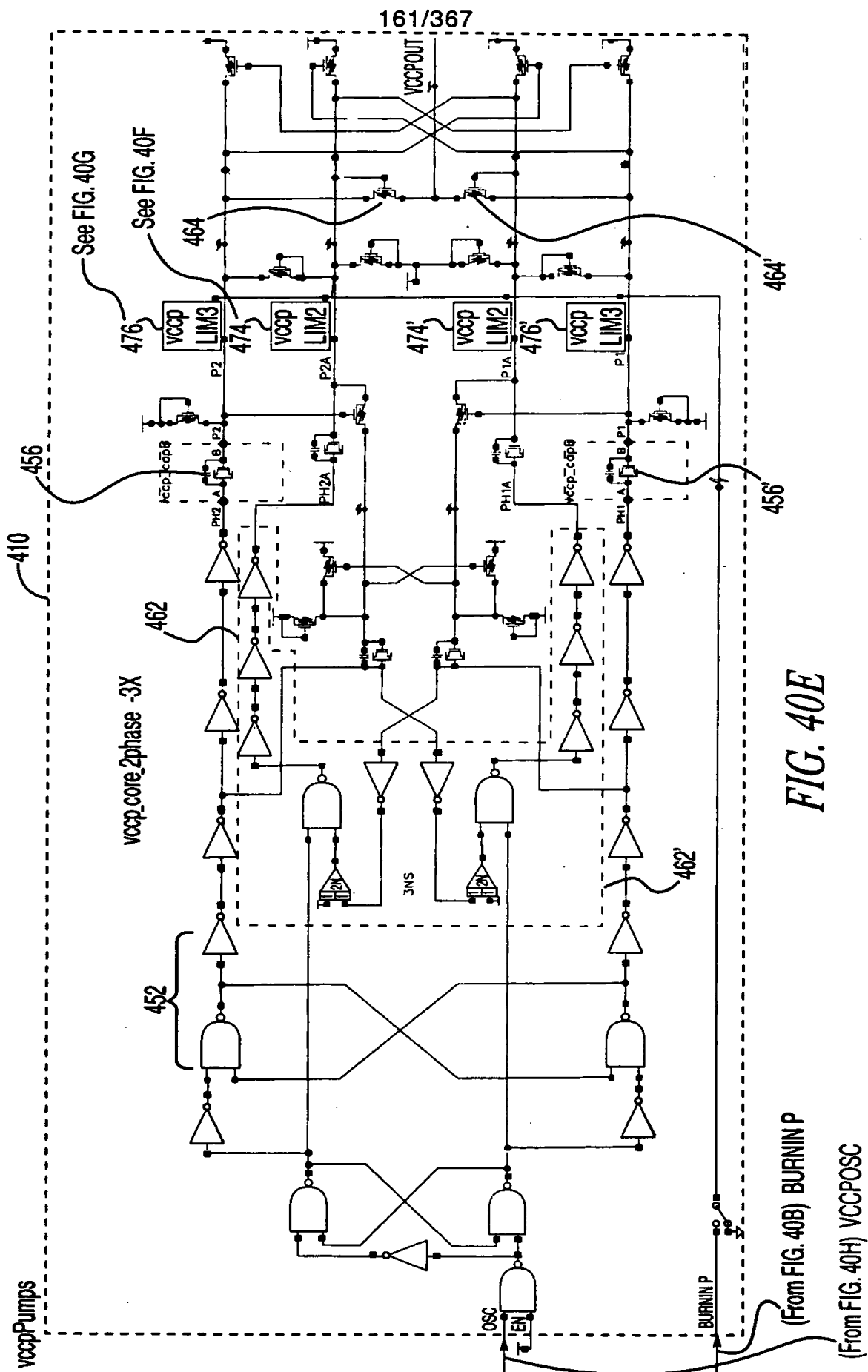


FIG. 40E

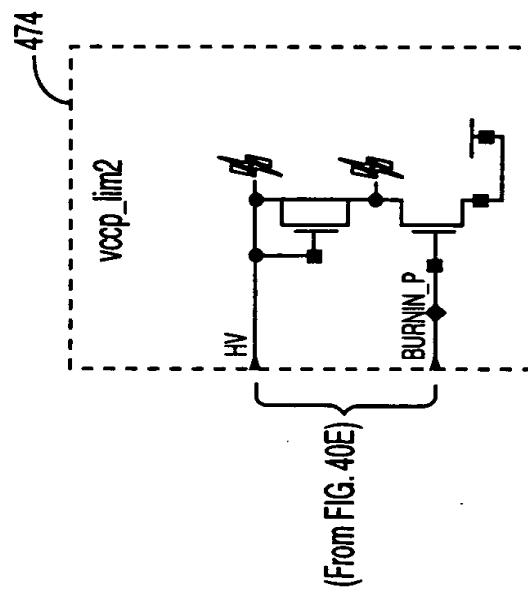


FIG. 40F

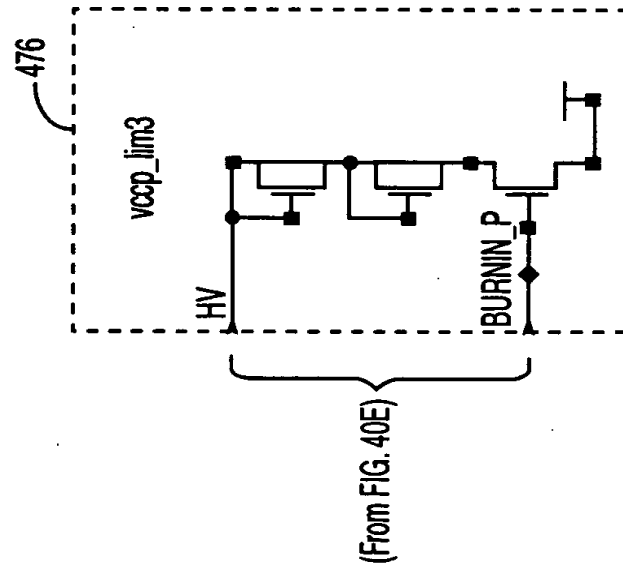


FIG. 40G

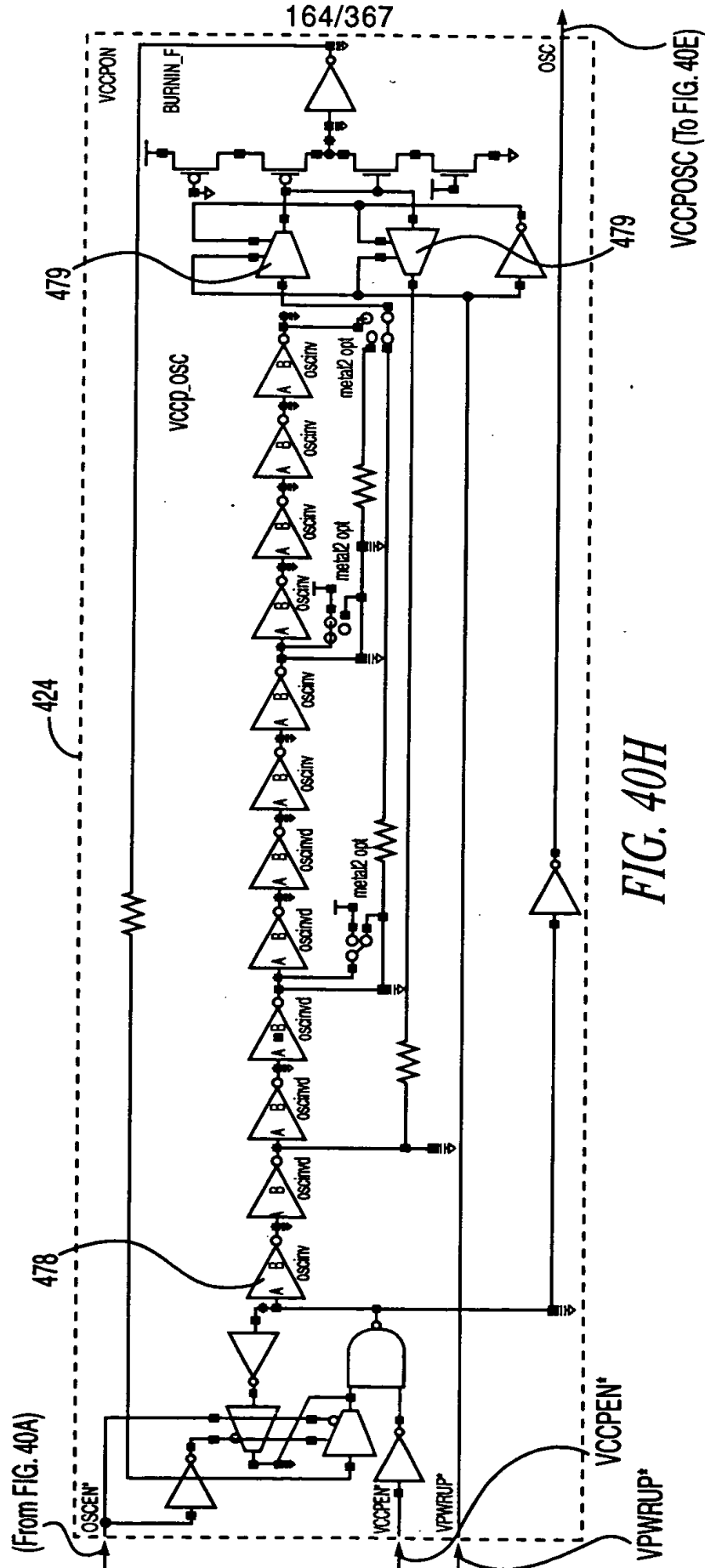


FIG. 40H

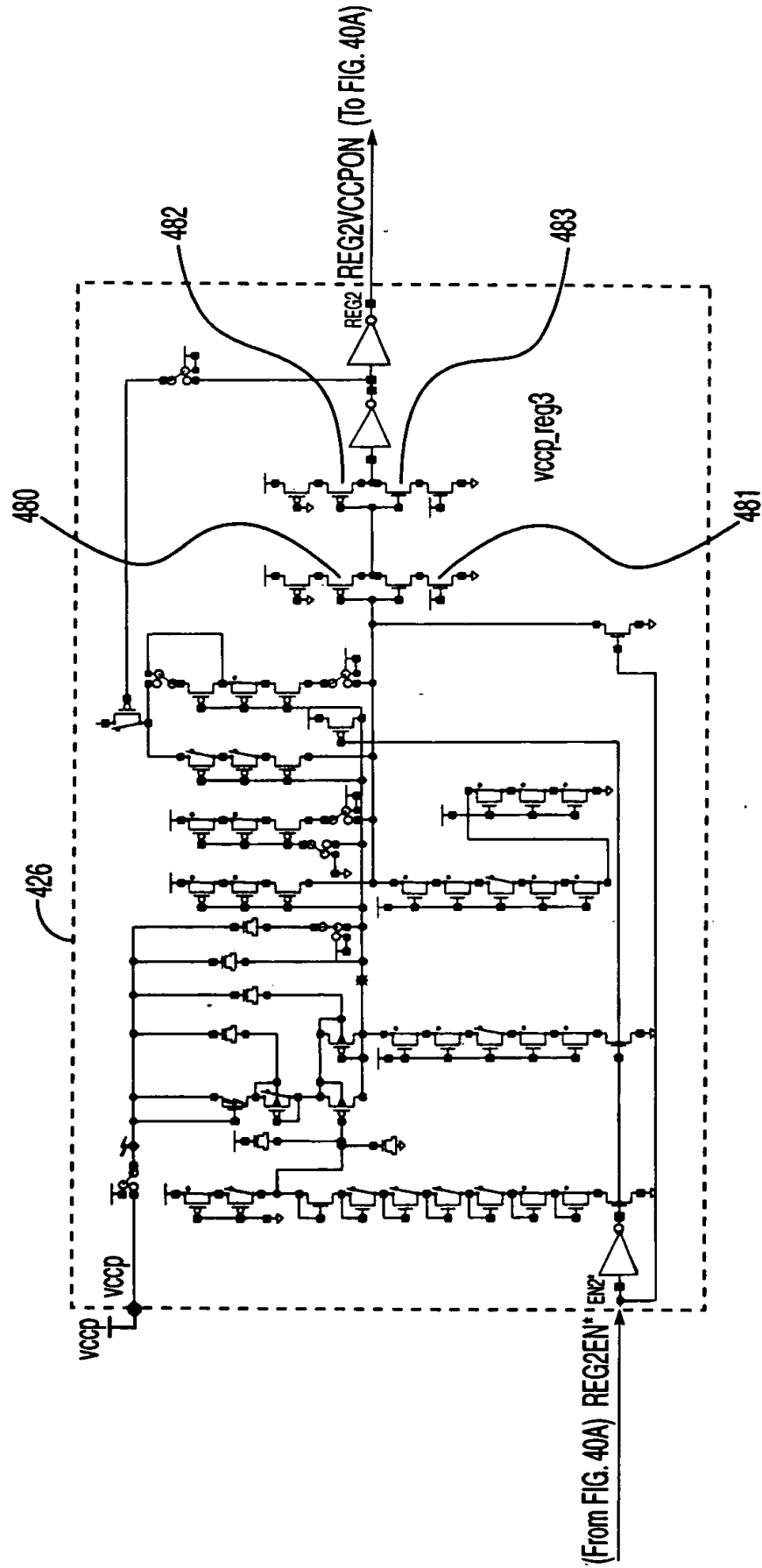


FIG. 40I

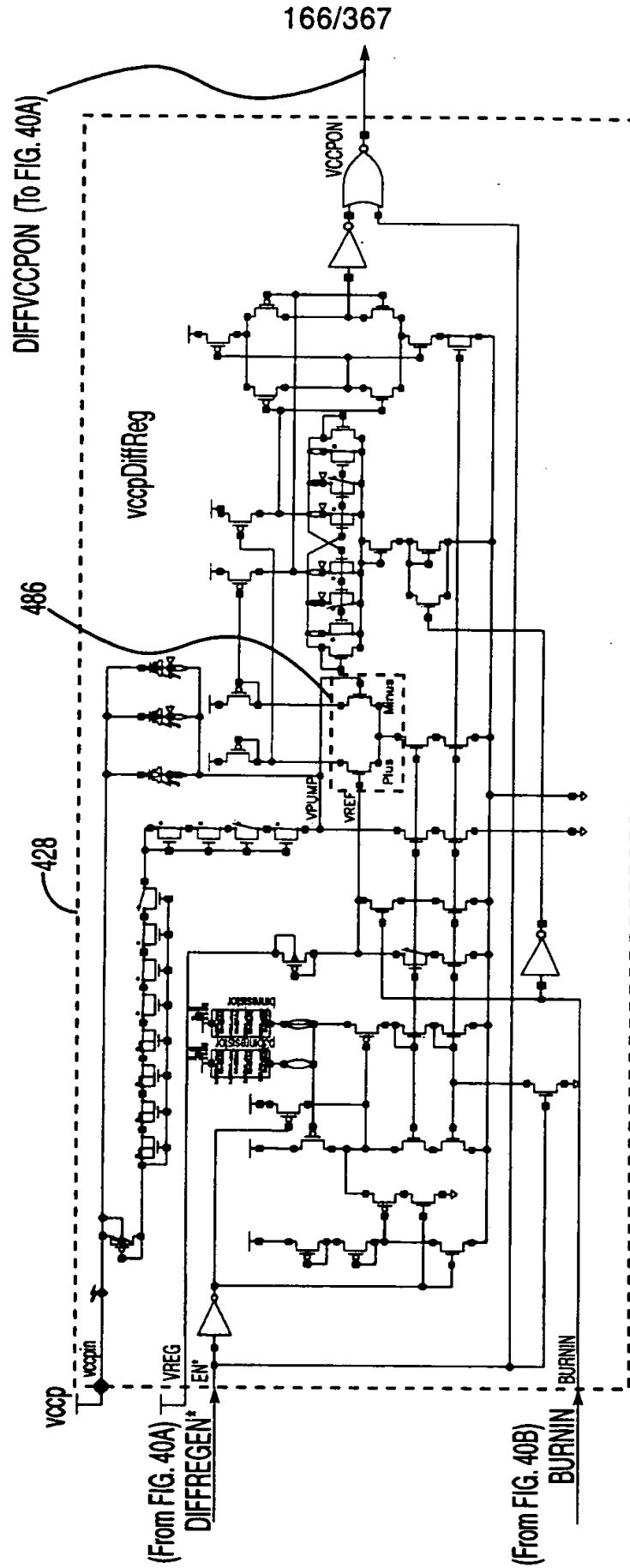


FIG. 40J

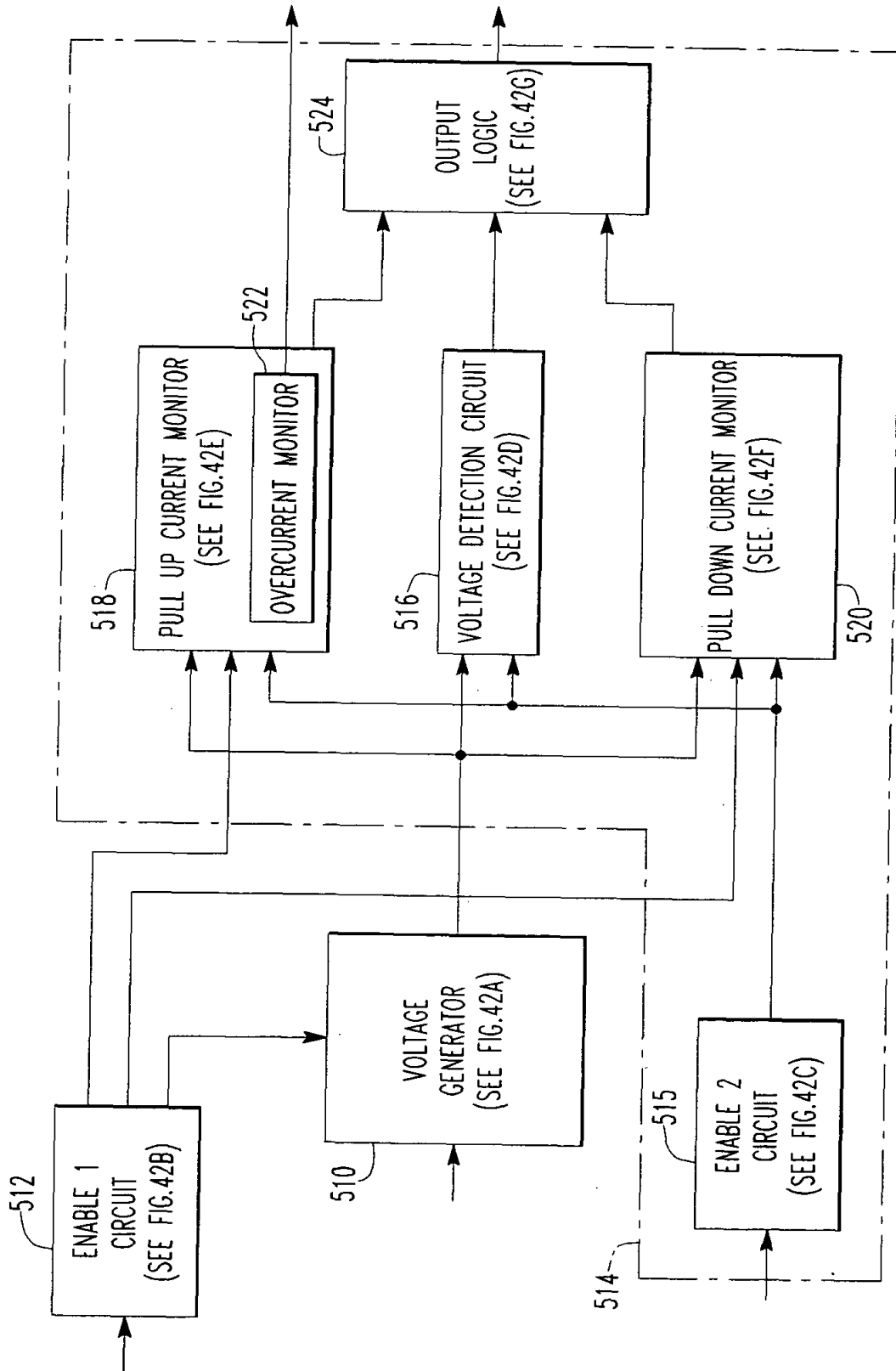


FIG. 41

500

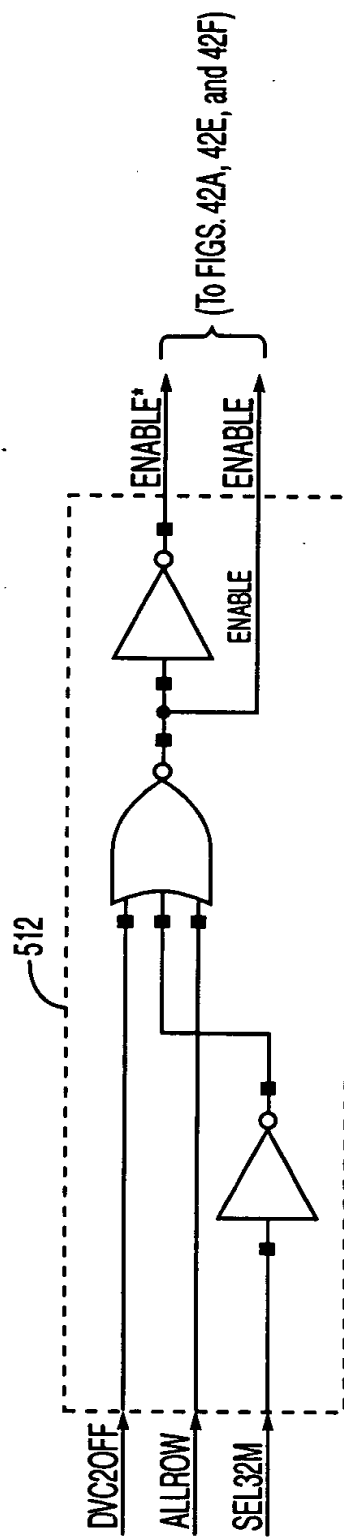


FIG. 42B

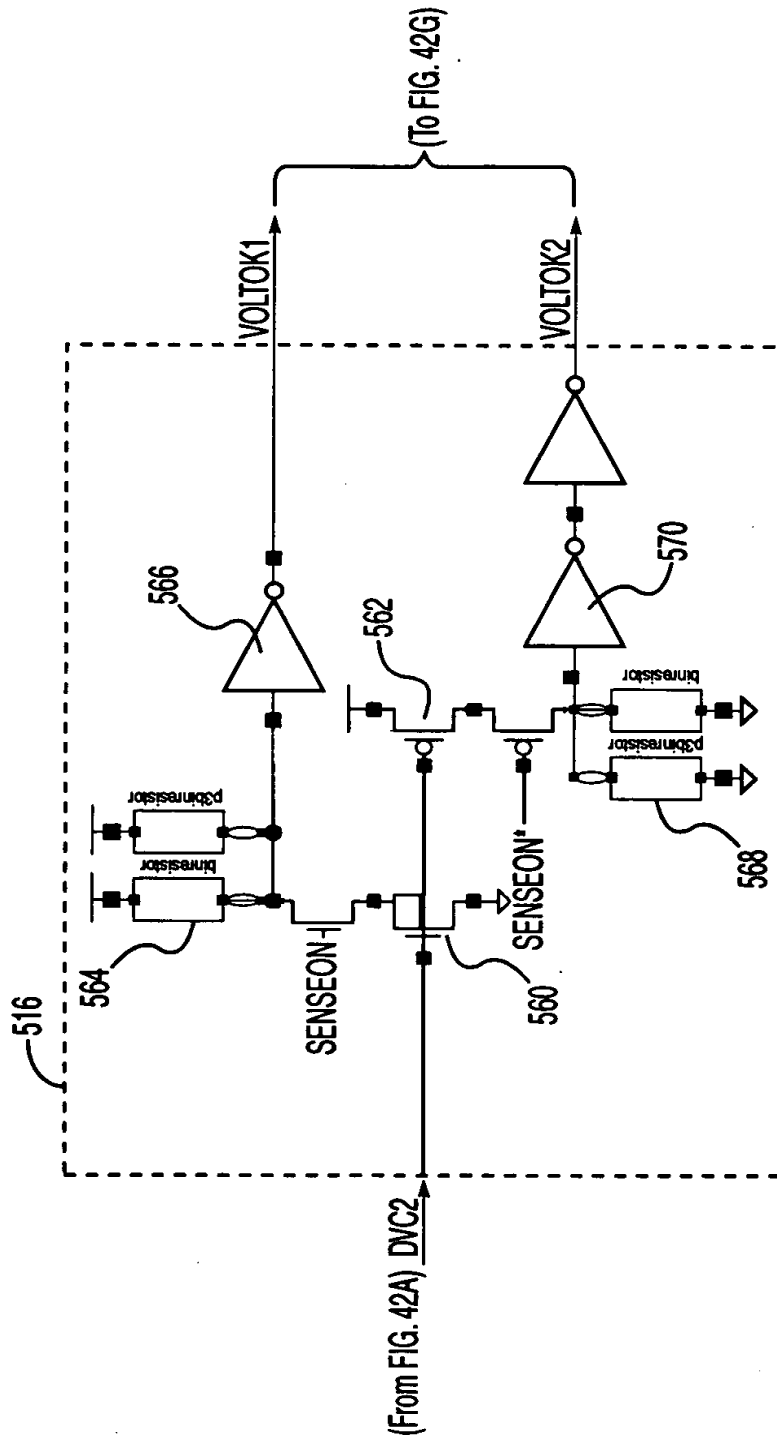


FIG. 42D

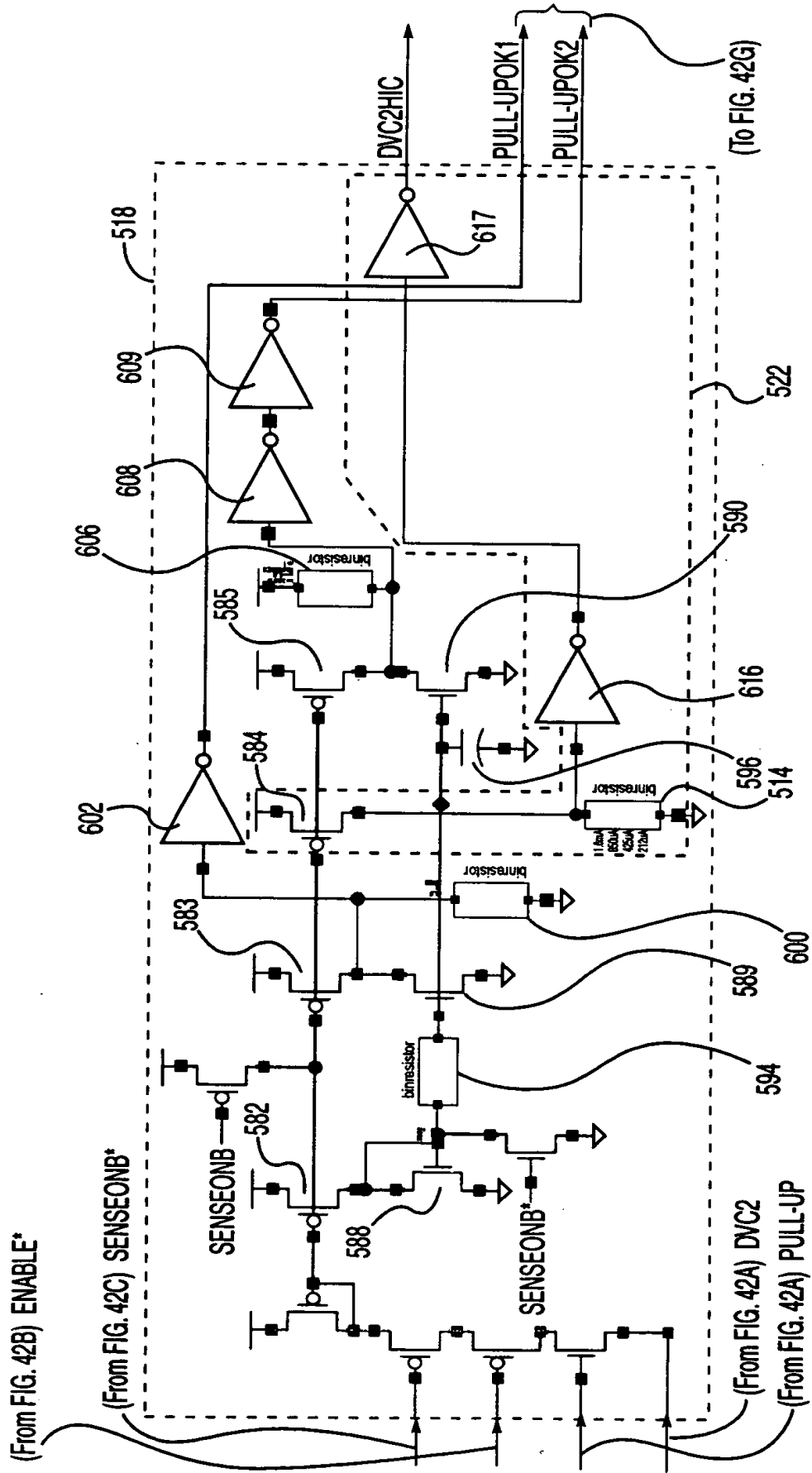


FIG. 42E

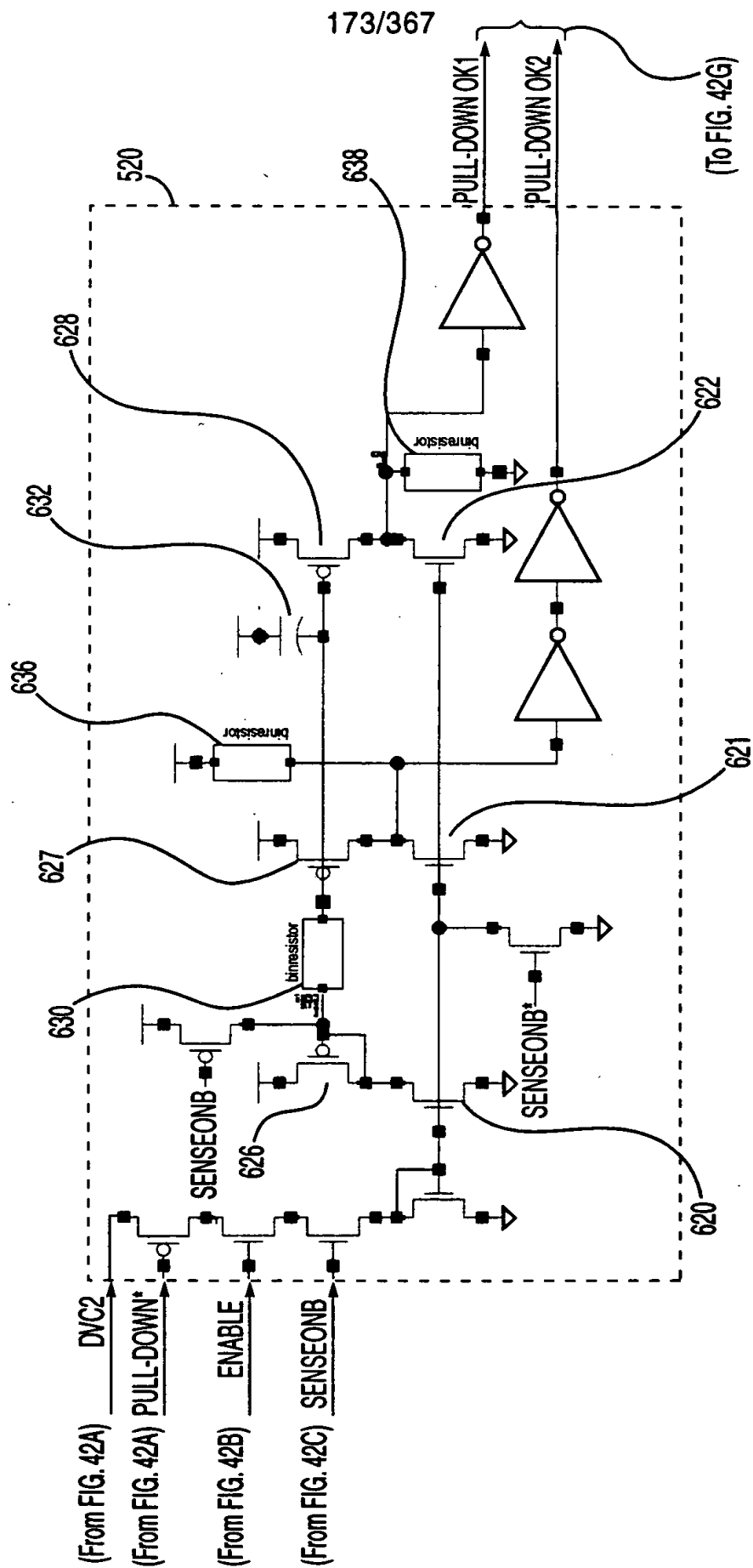


FIG. 42F

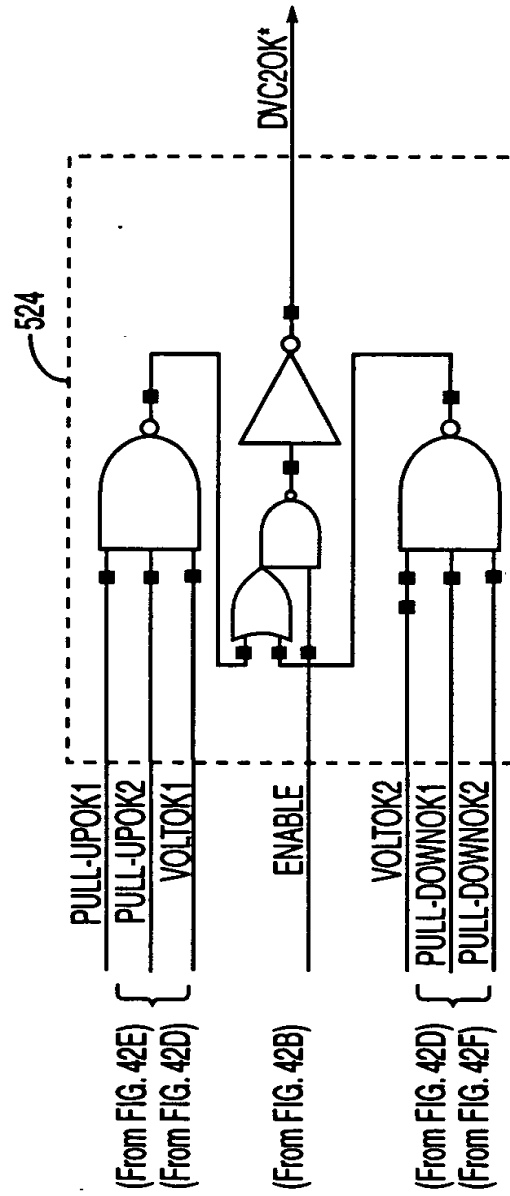


FIG. 42G

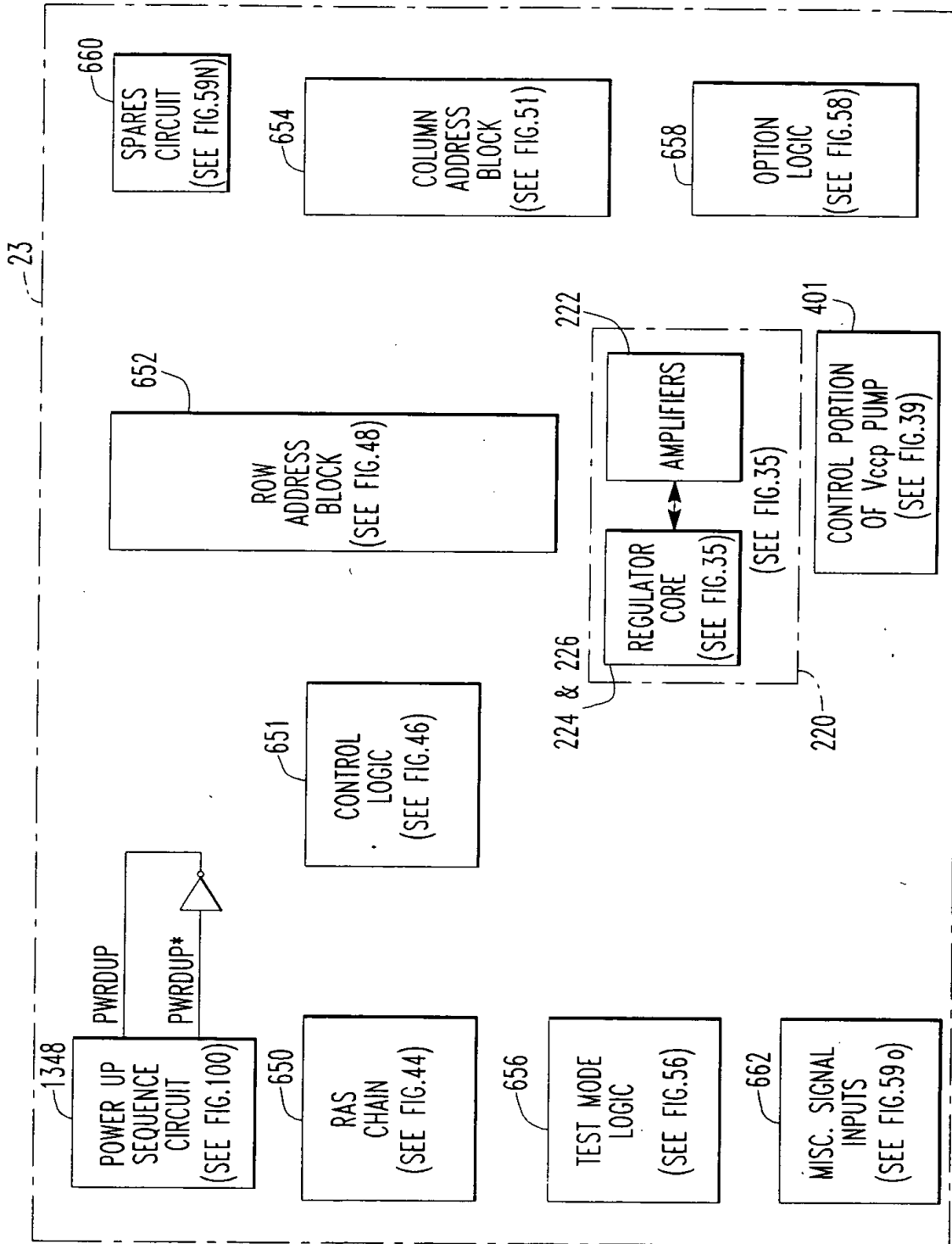


FIG. 43

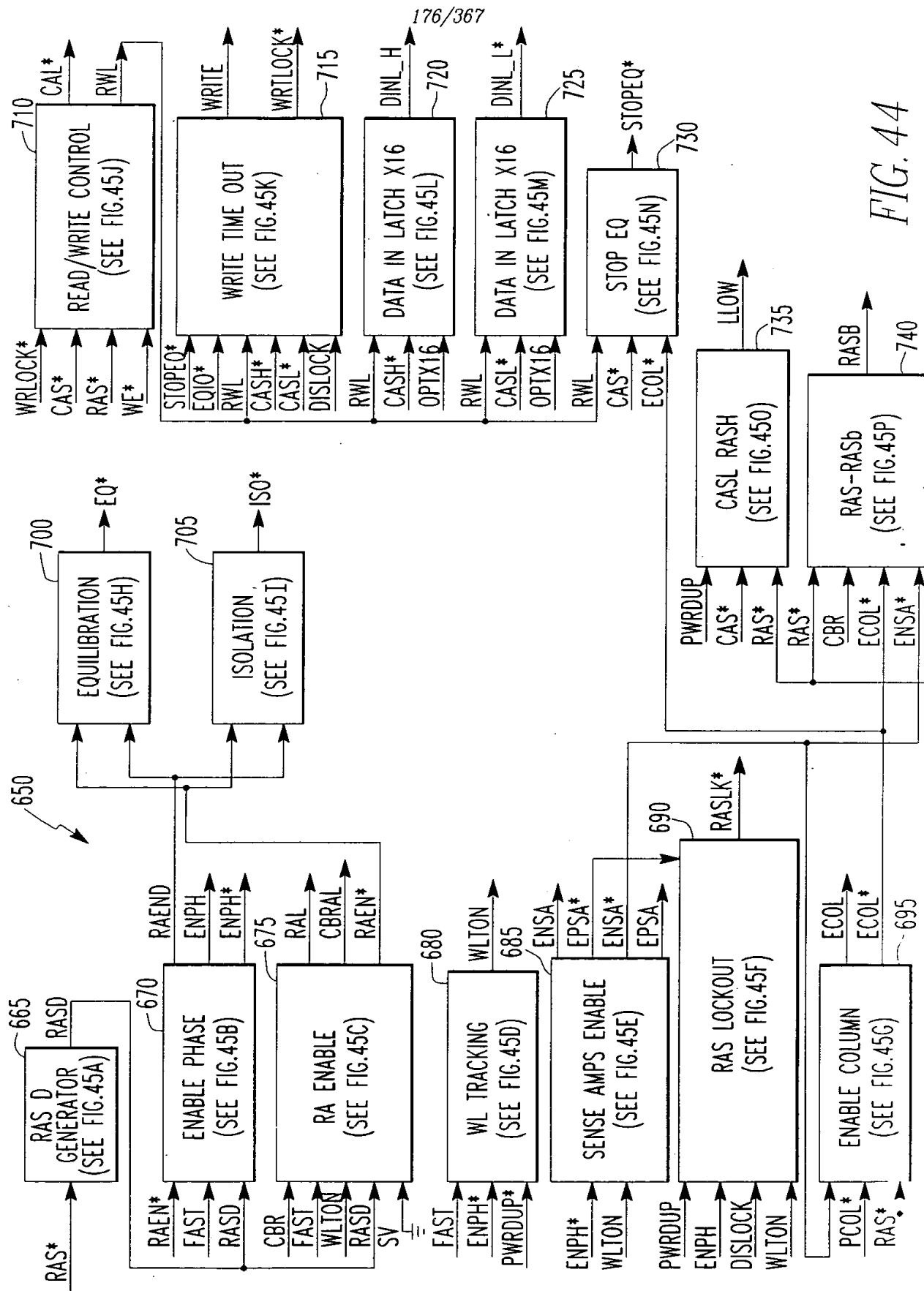
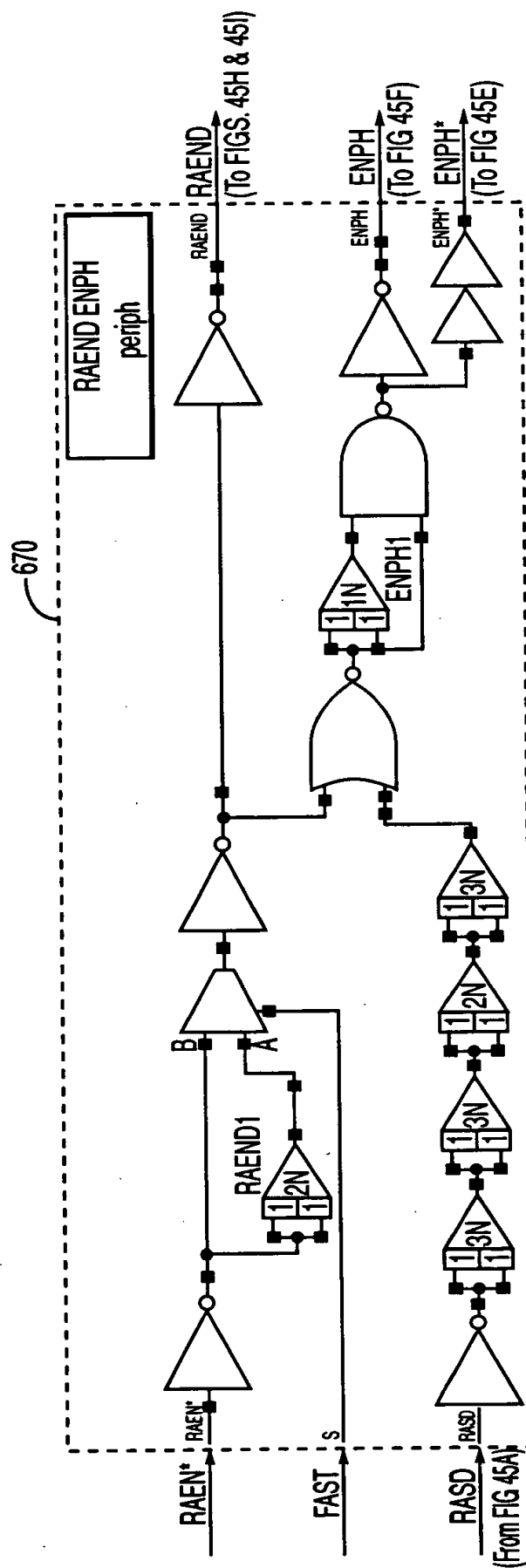


FIG. 44



FIG. 45A



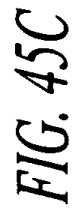
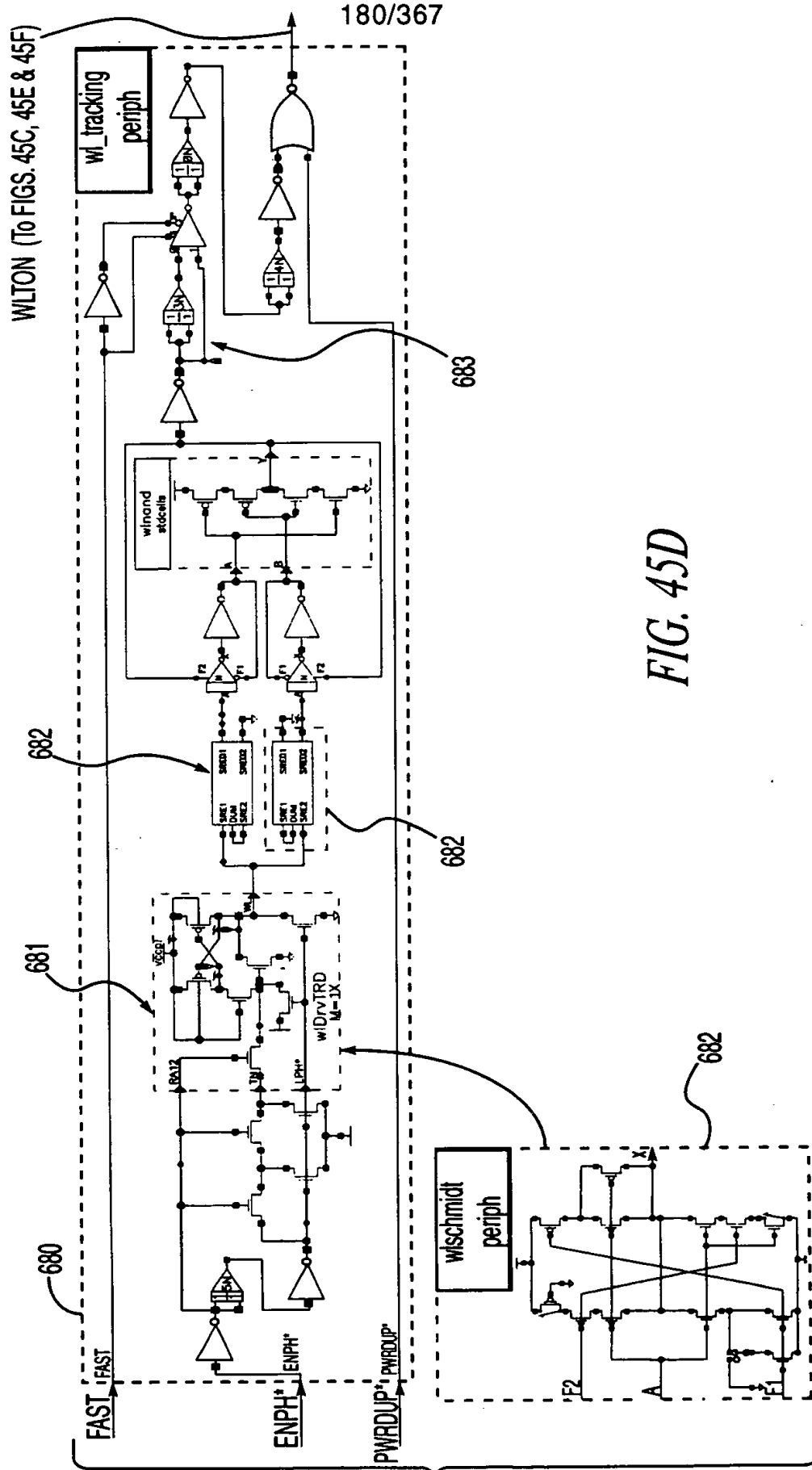


FIG. 45C



(From FIG. 45B)

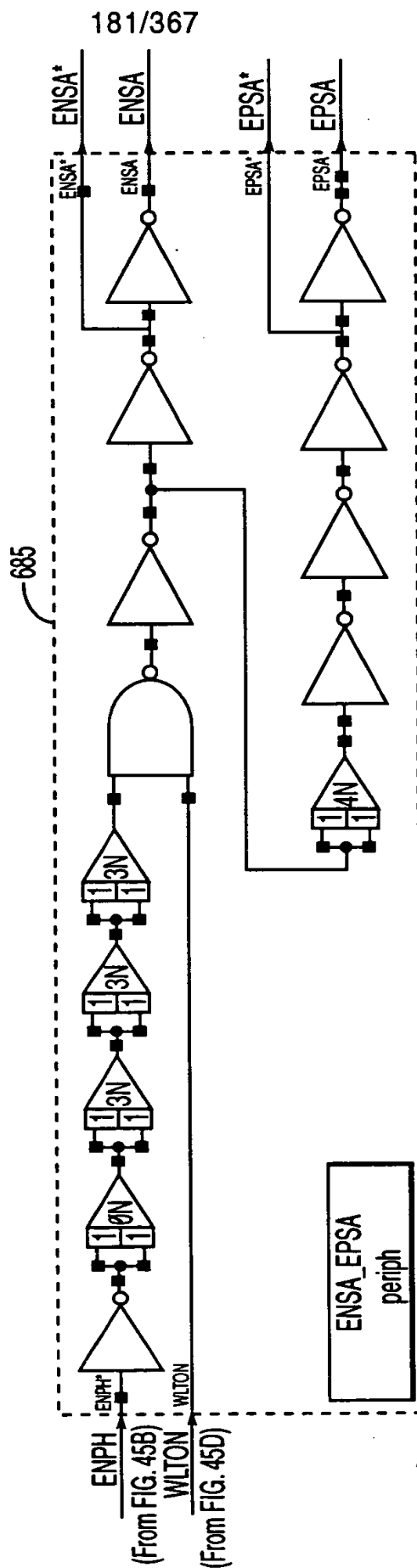


FIG. 45E

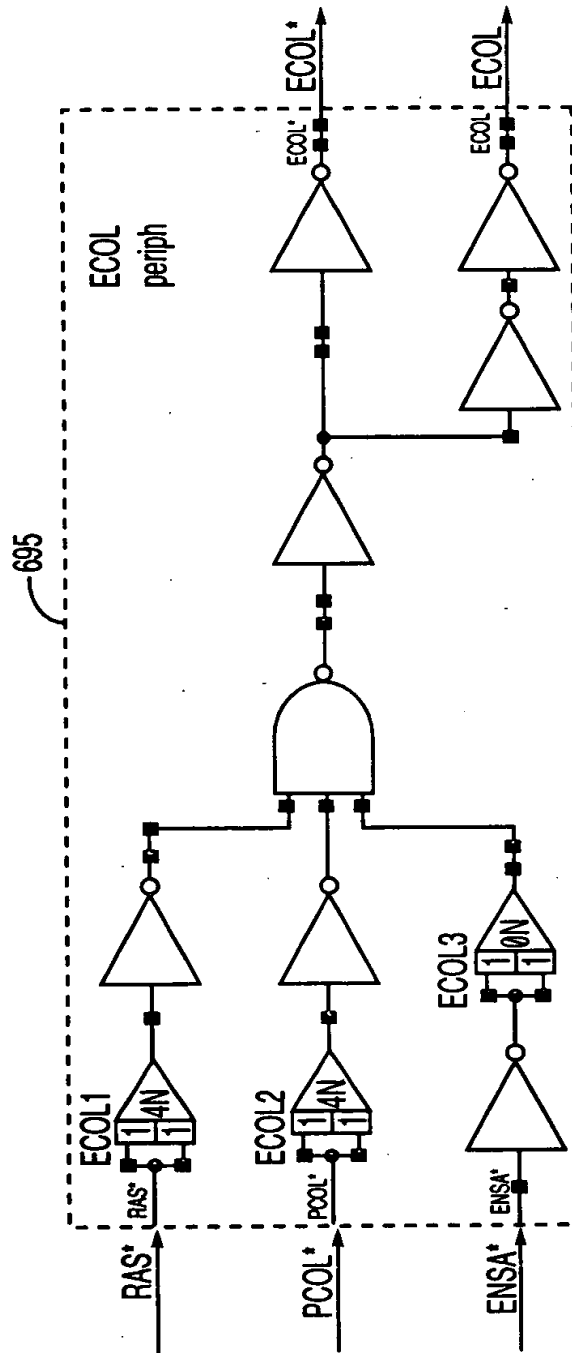


FIG. 45G

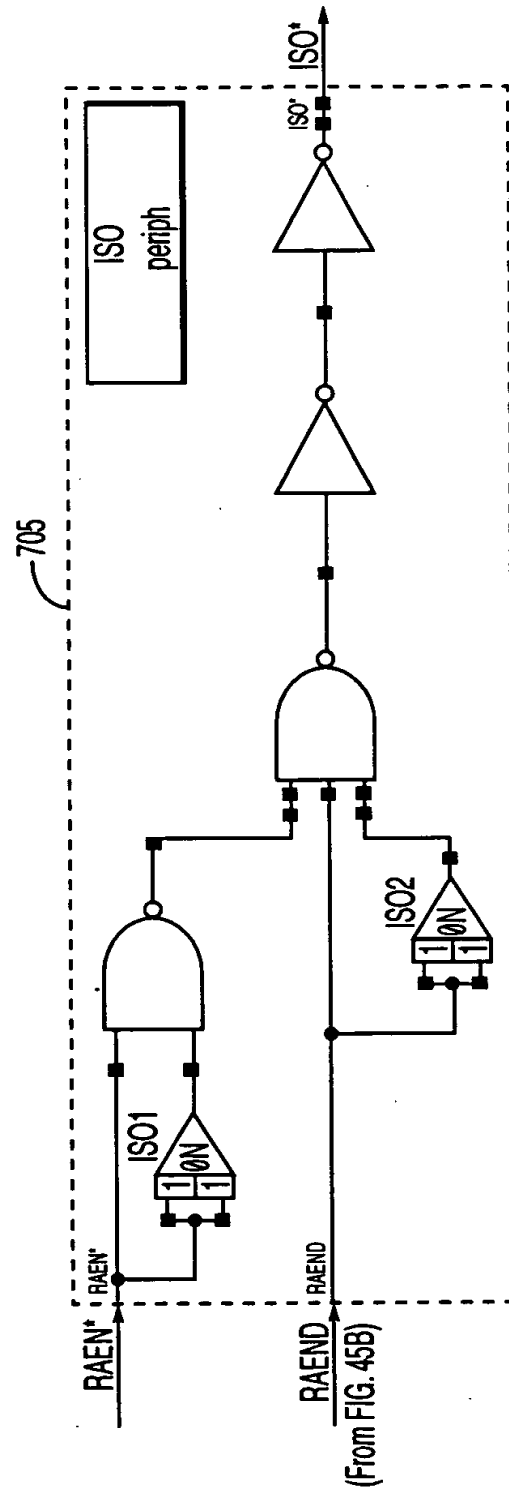


FIG. 45I



FIG. 45J

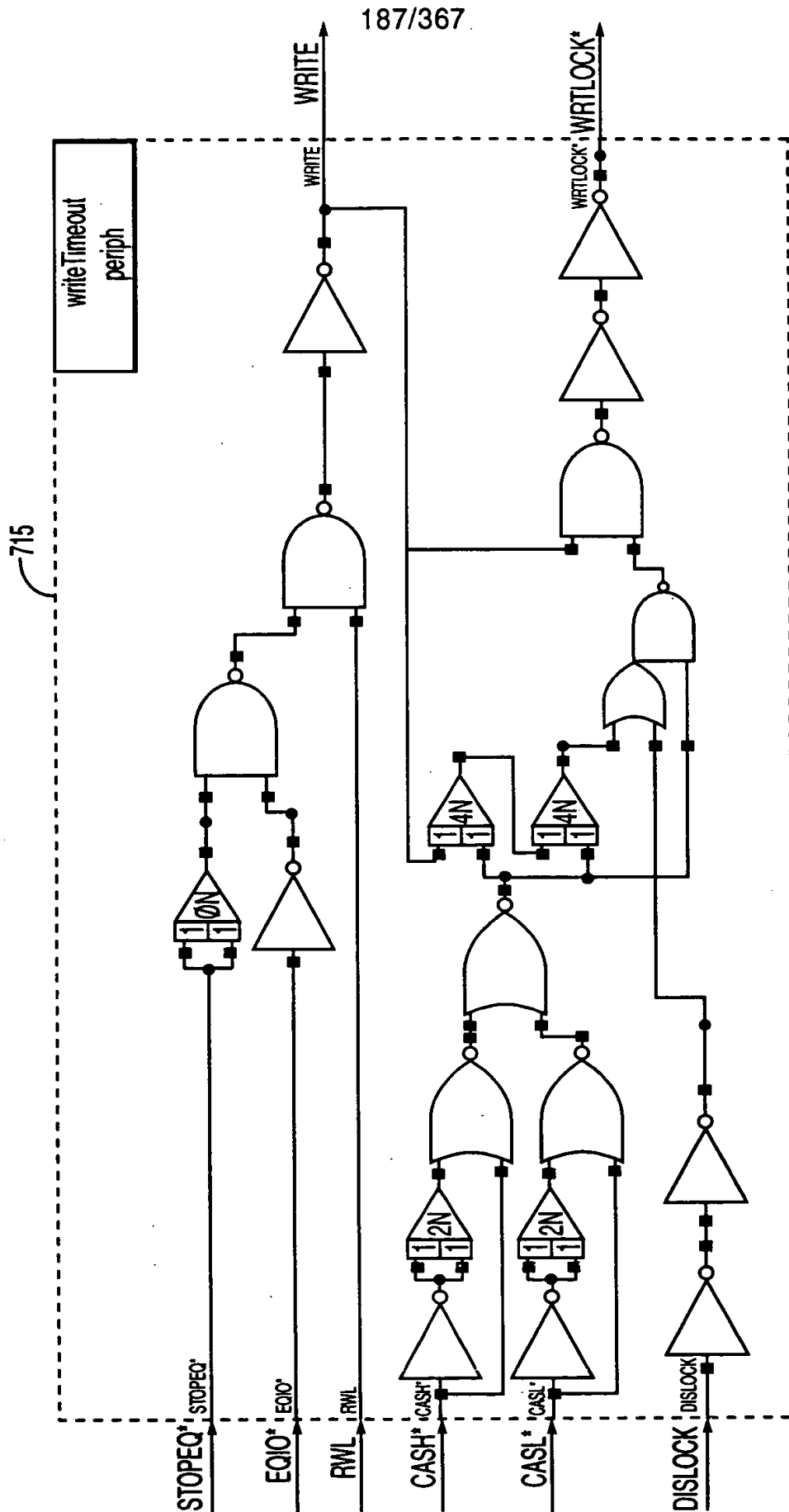


FIG. 45K

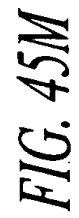


FIG. 45M

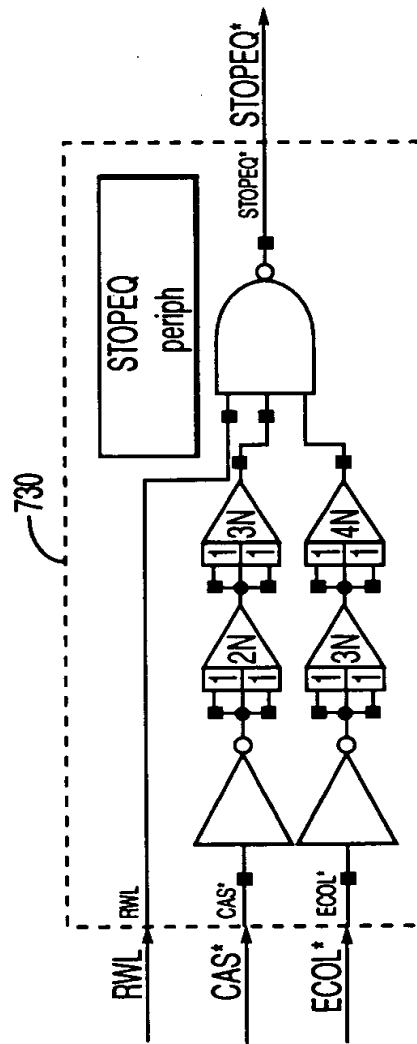


FIG. 45N

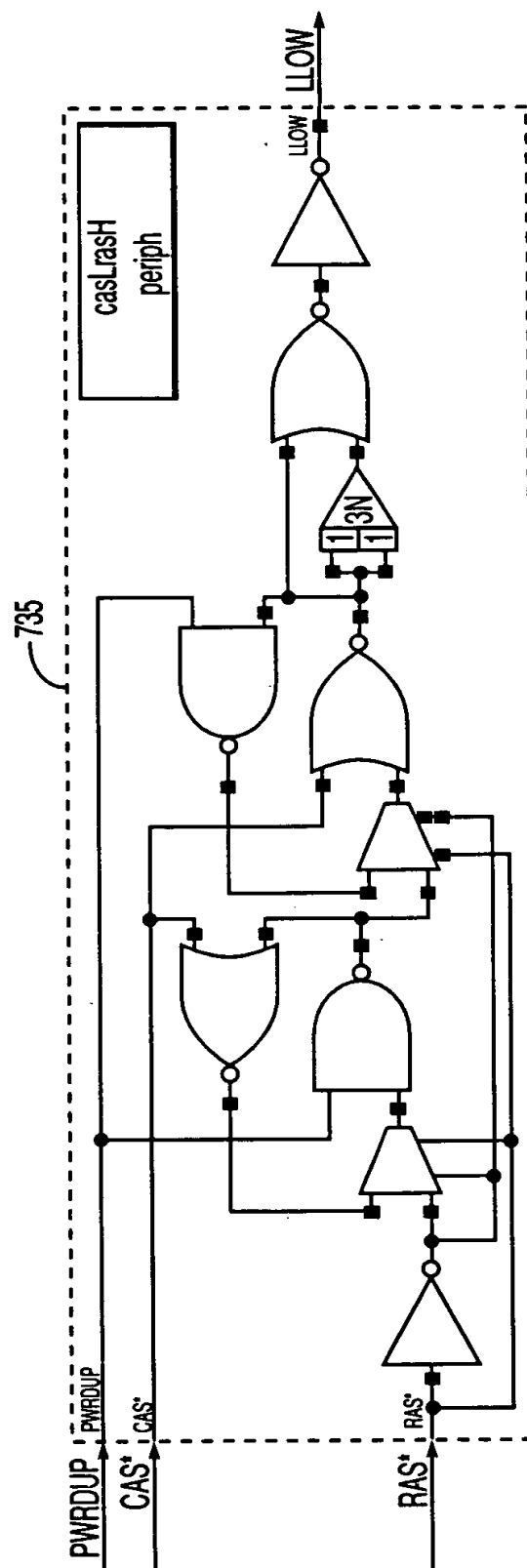


FIG. 450

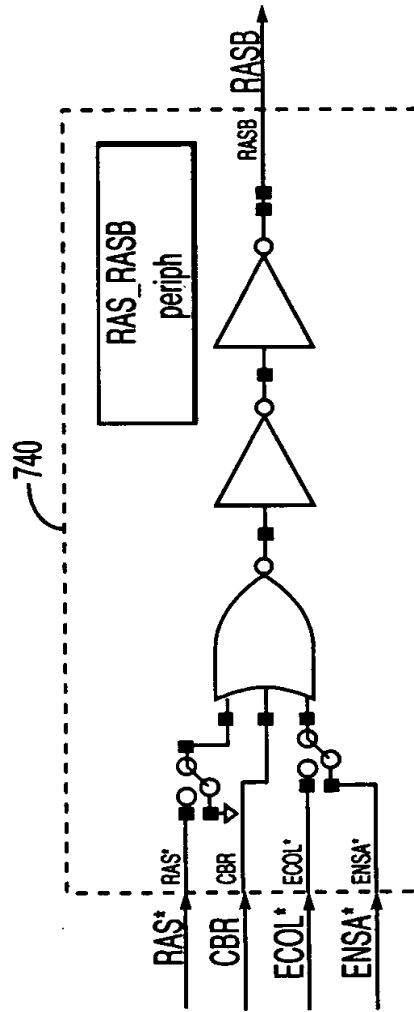


FIG. 45P

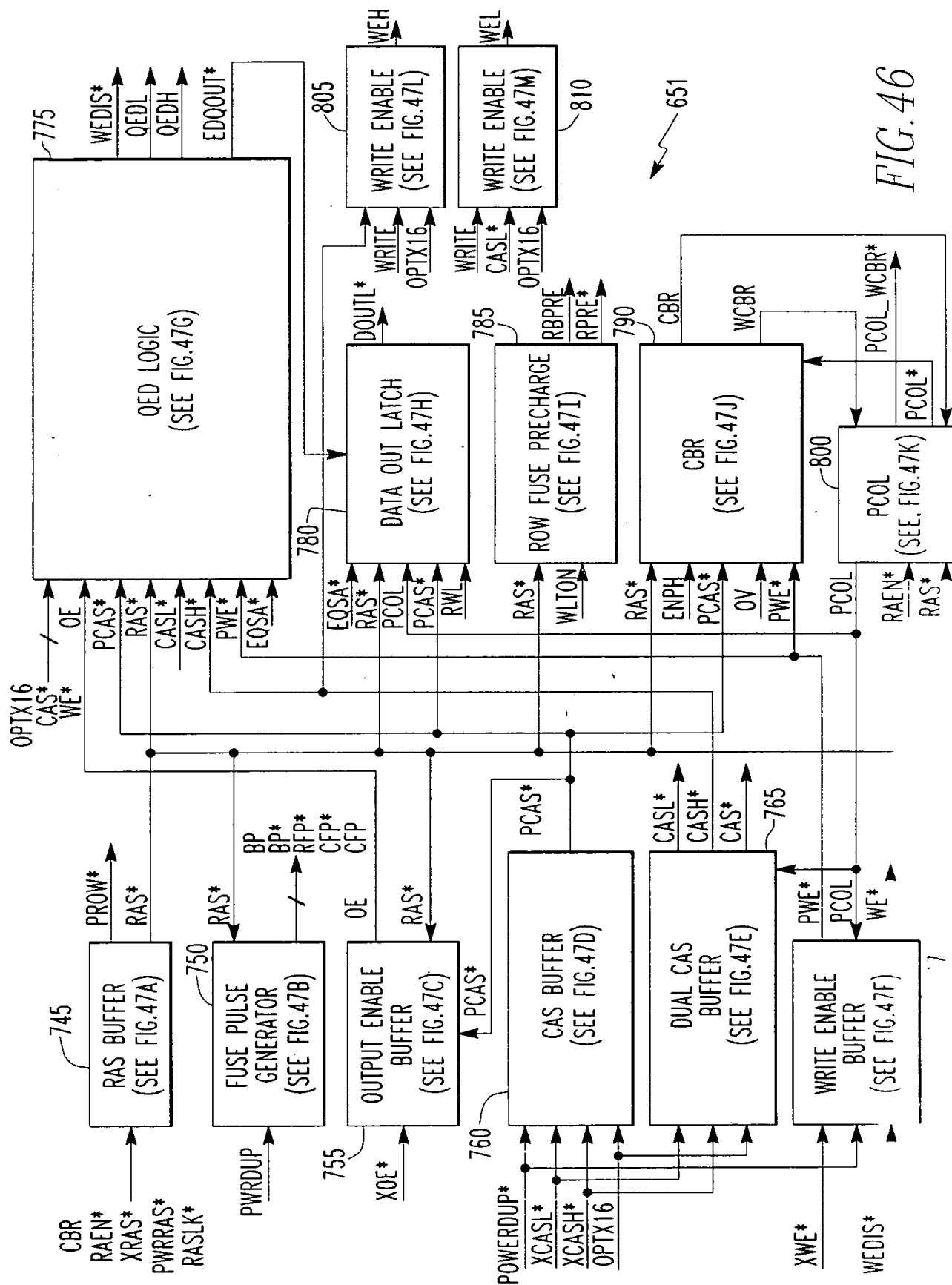


FIG. 46

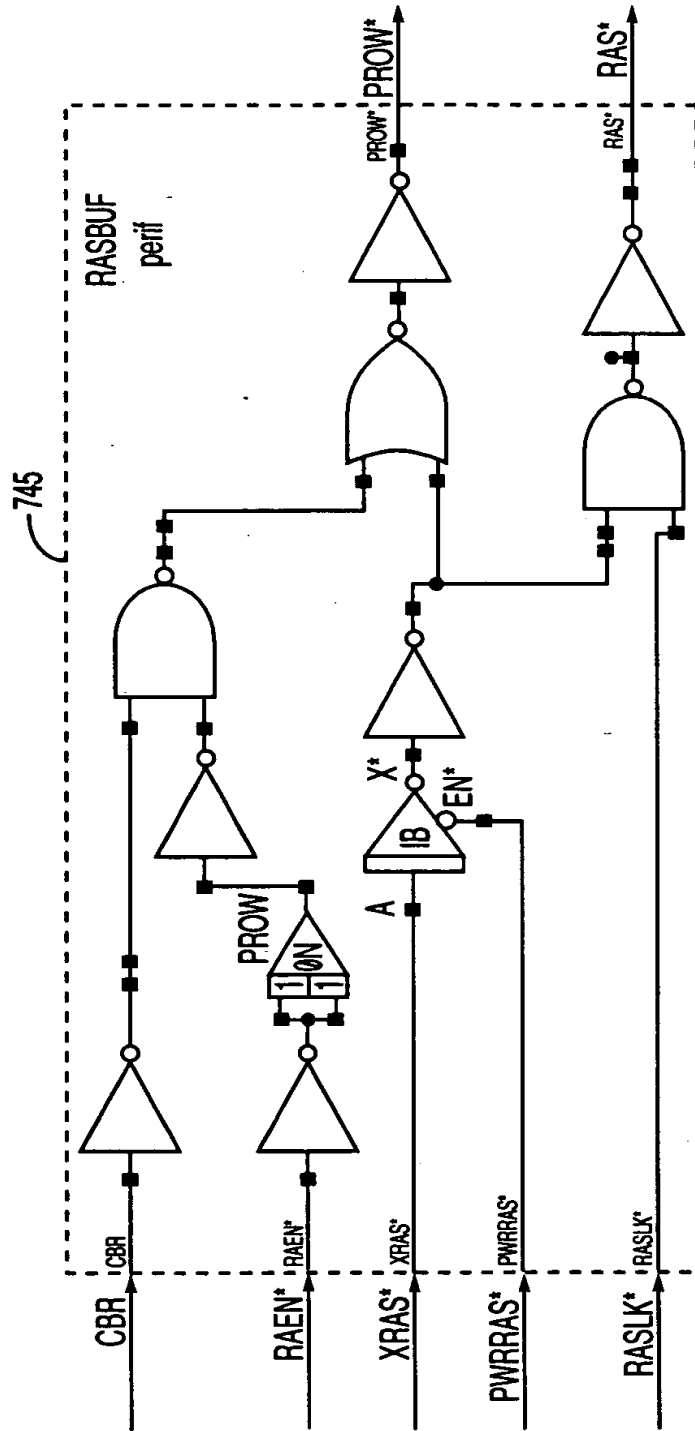


FIG. 47A

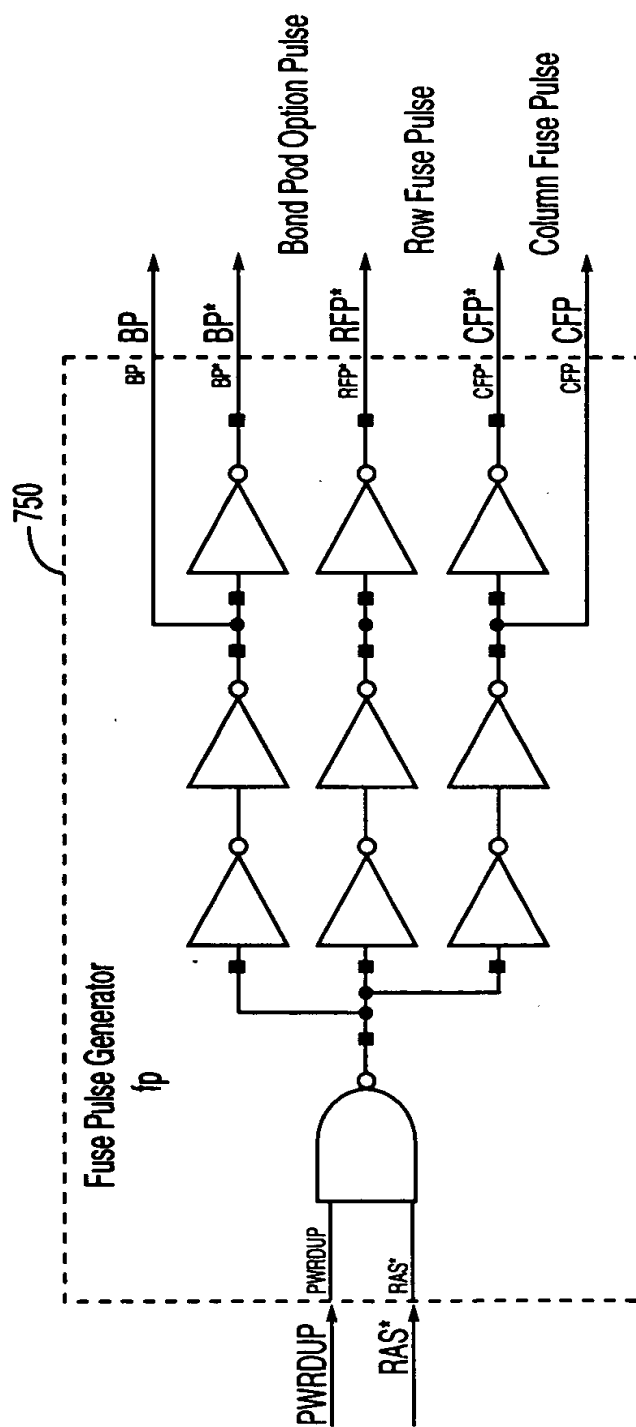


FIG. 47B

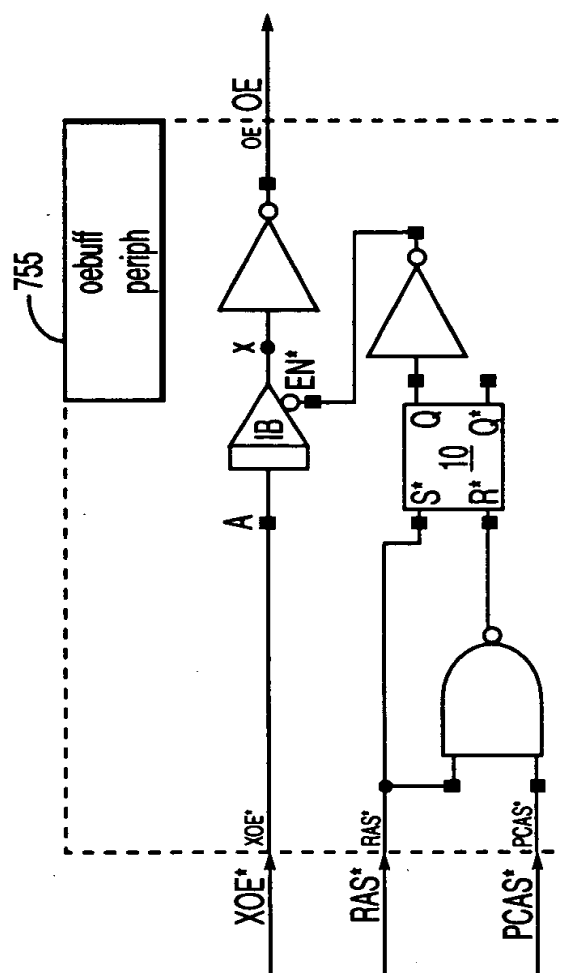


FIG. 47C



FIG. 47E

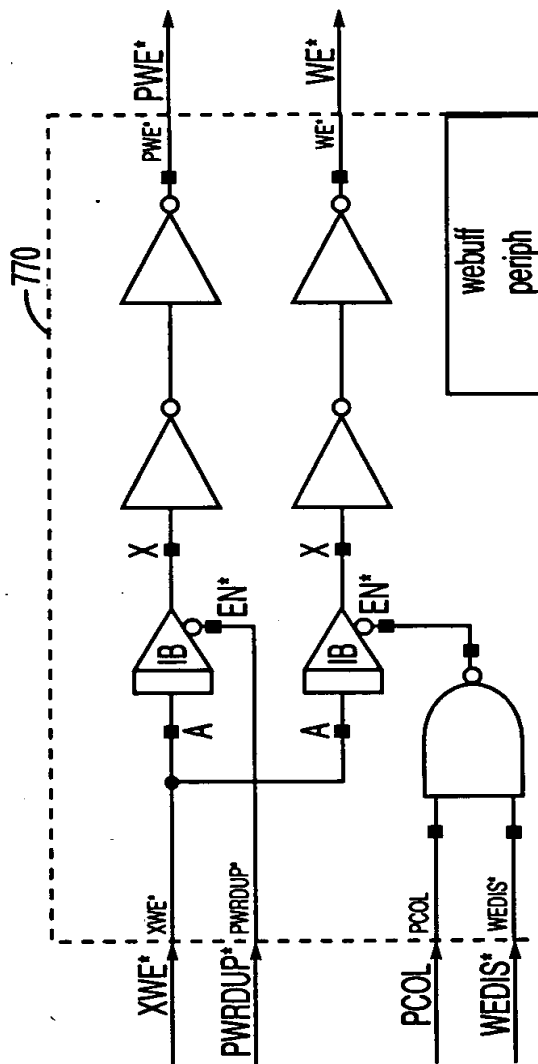


FIG. 47F

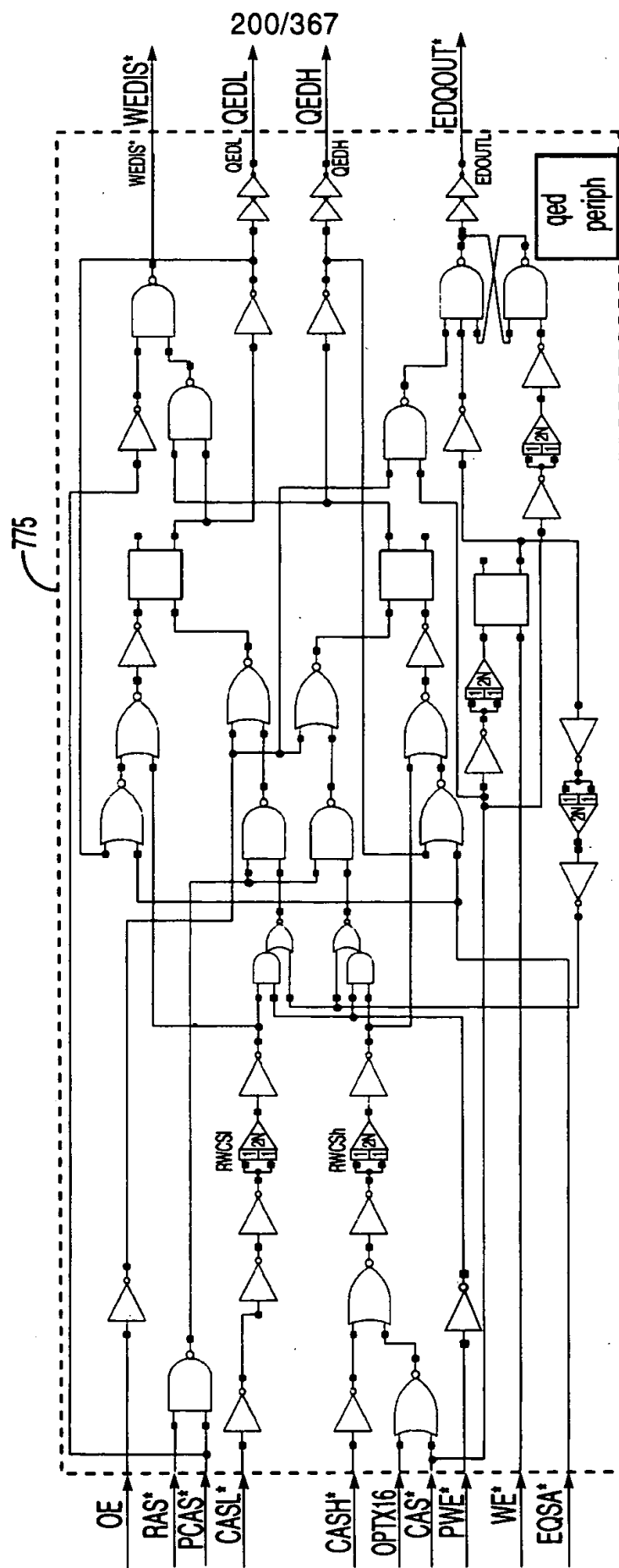
[illegible]

FIG. 47G

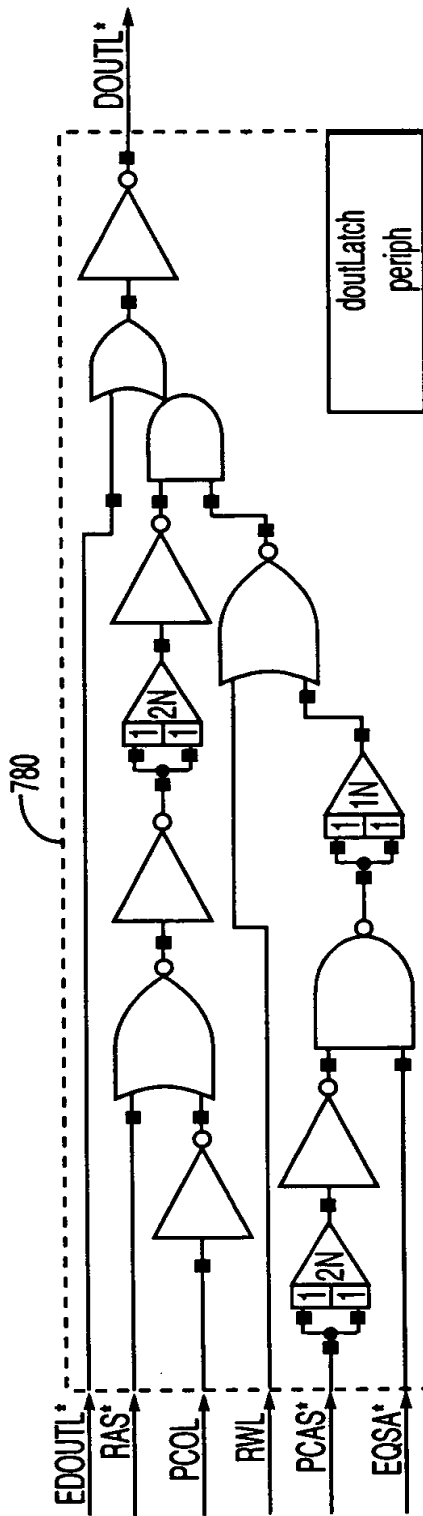


FIG. 47H

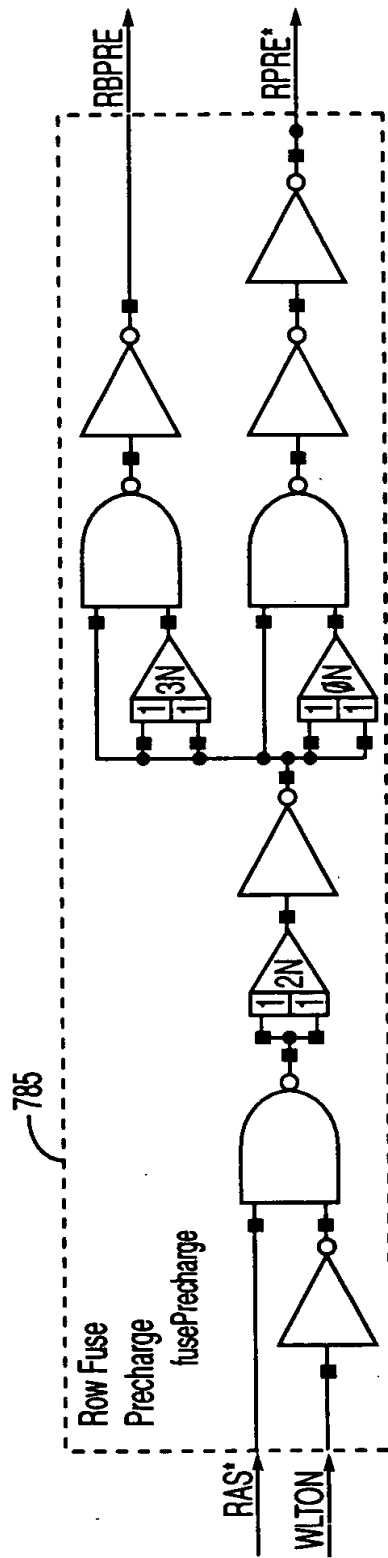


FIG. 471

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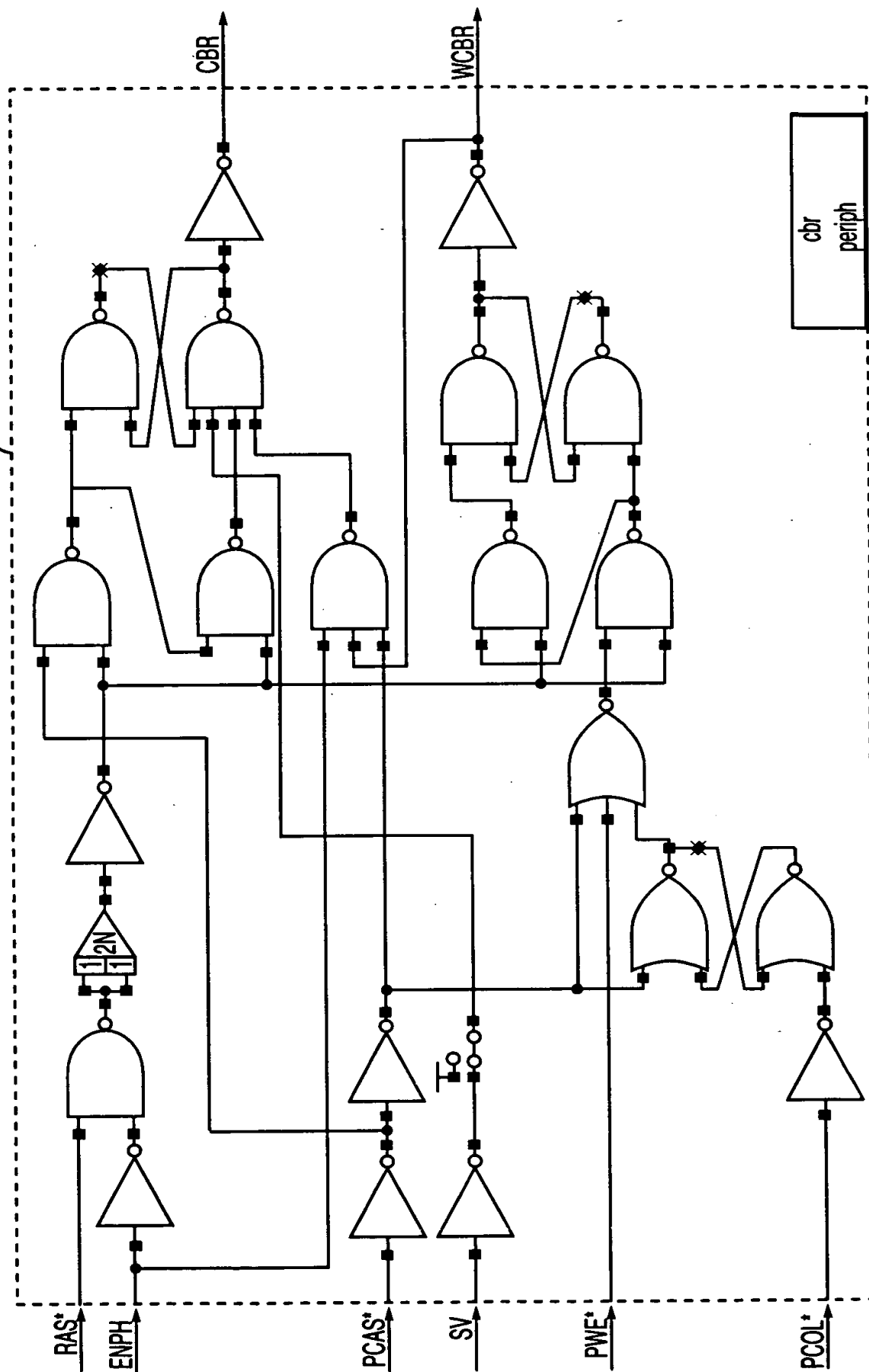


FIG. 47J

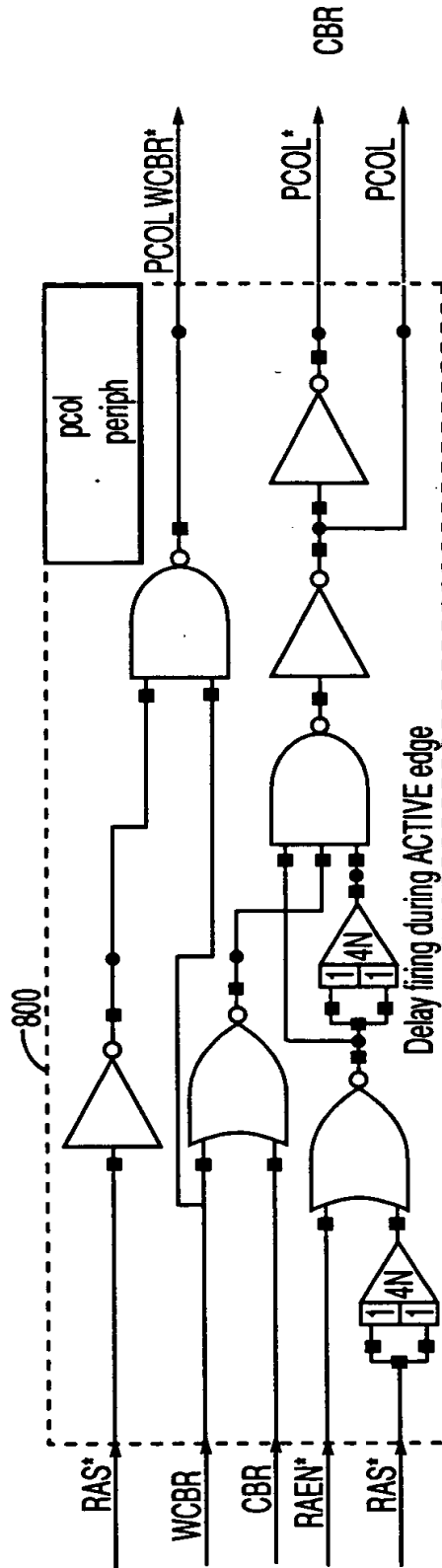


FIG. 47K



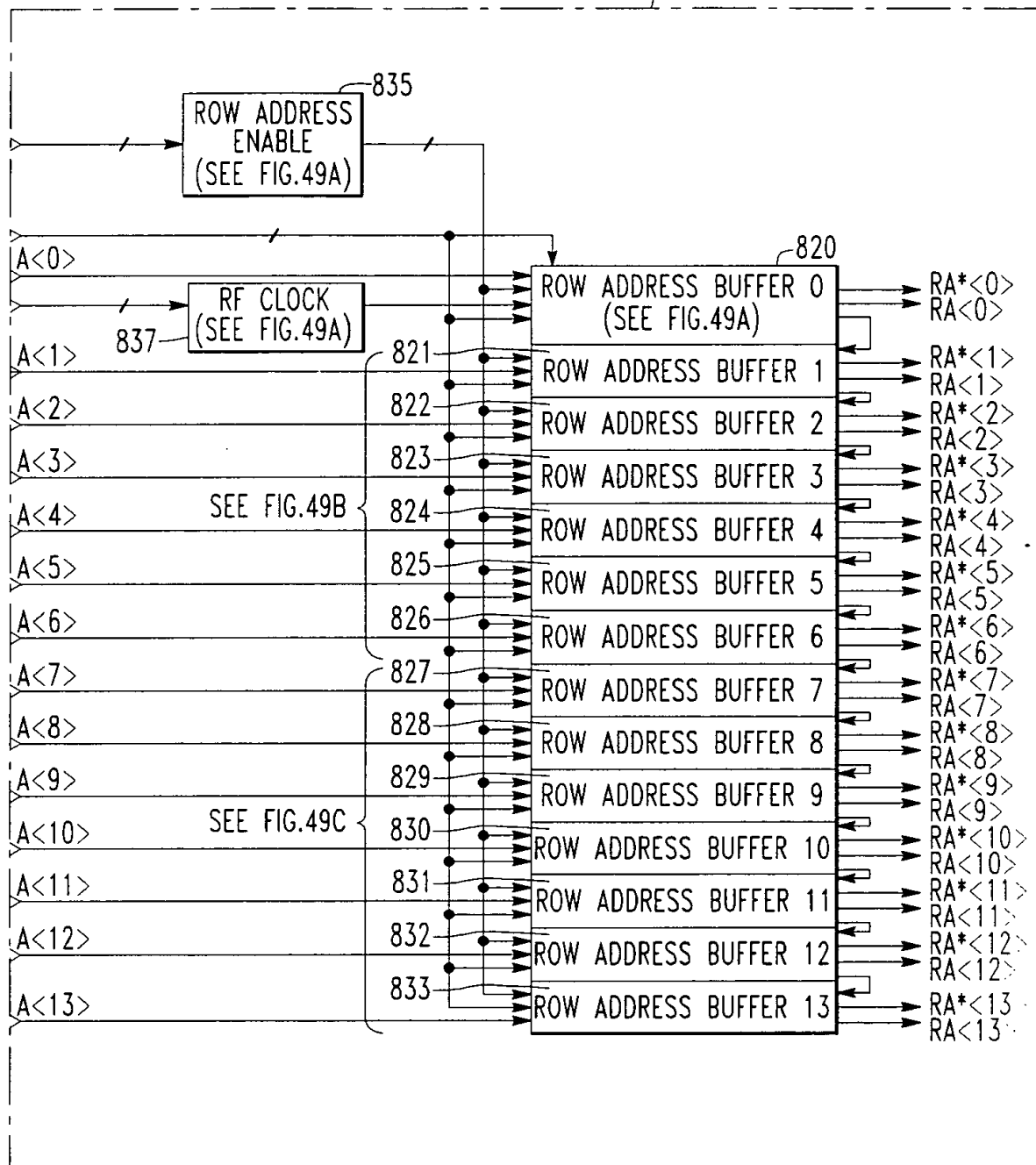


FIG. 48A

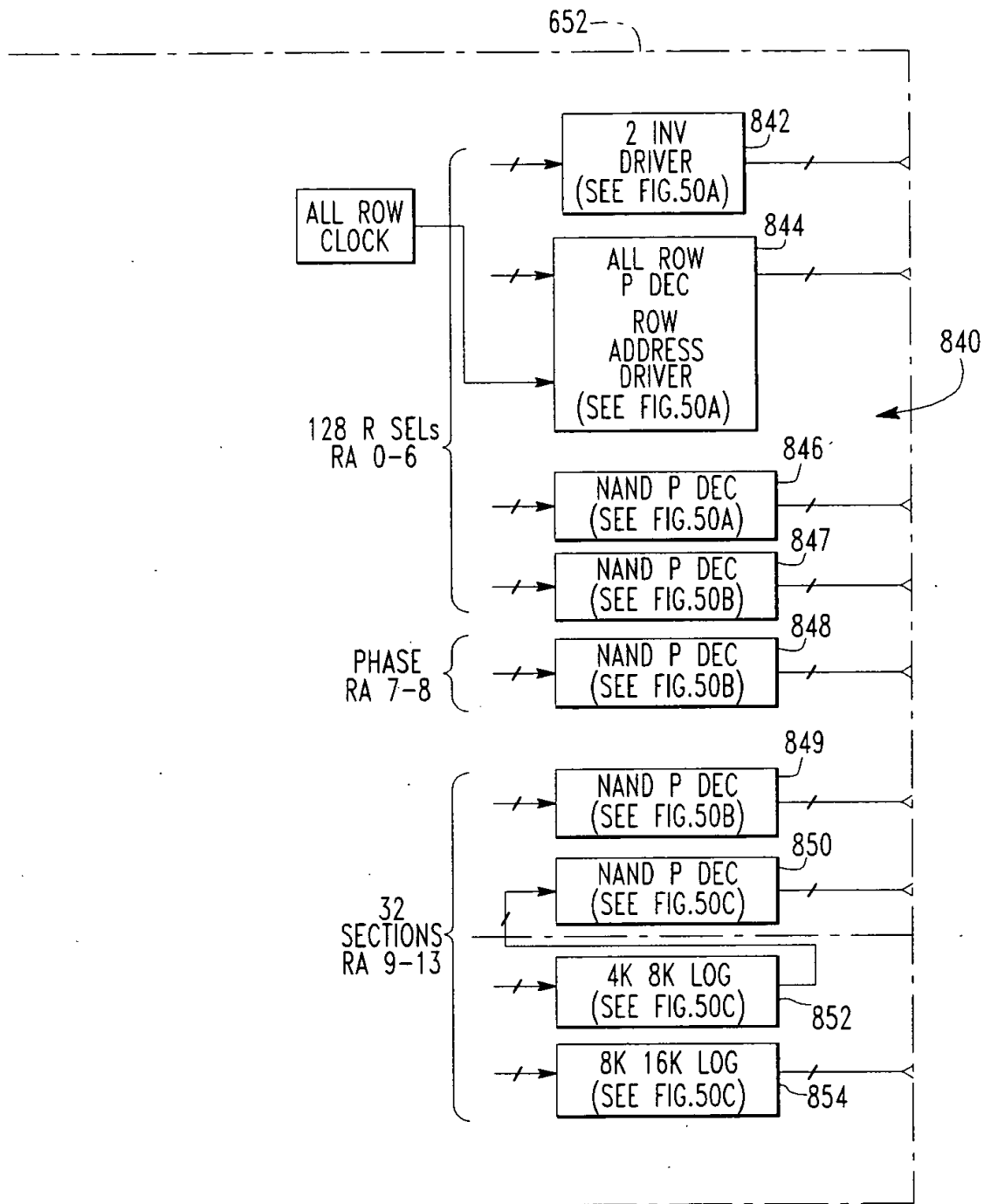


FIG. 48B

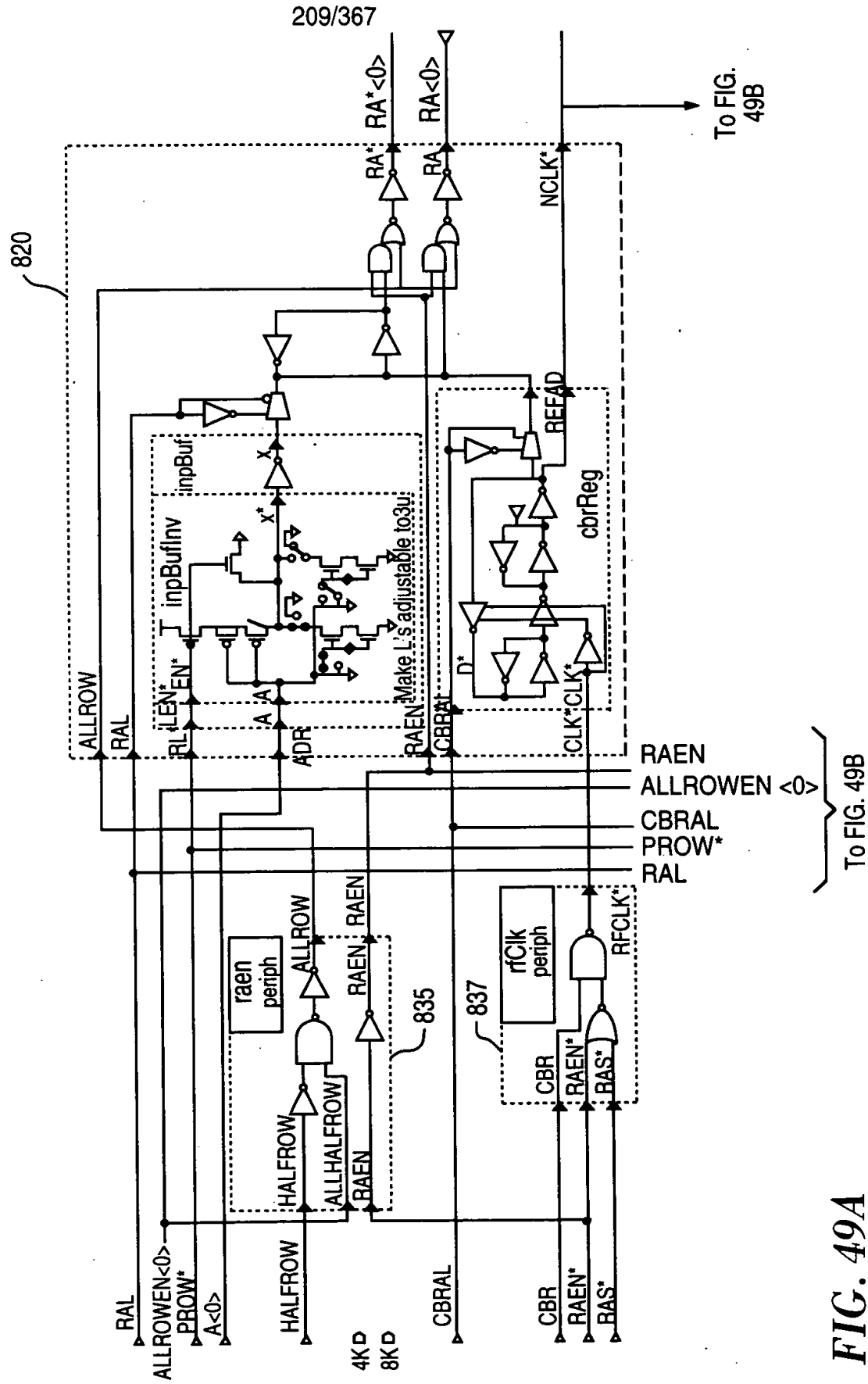
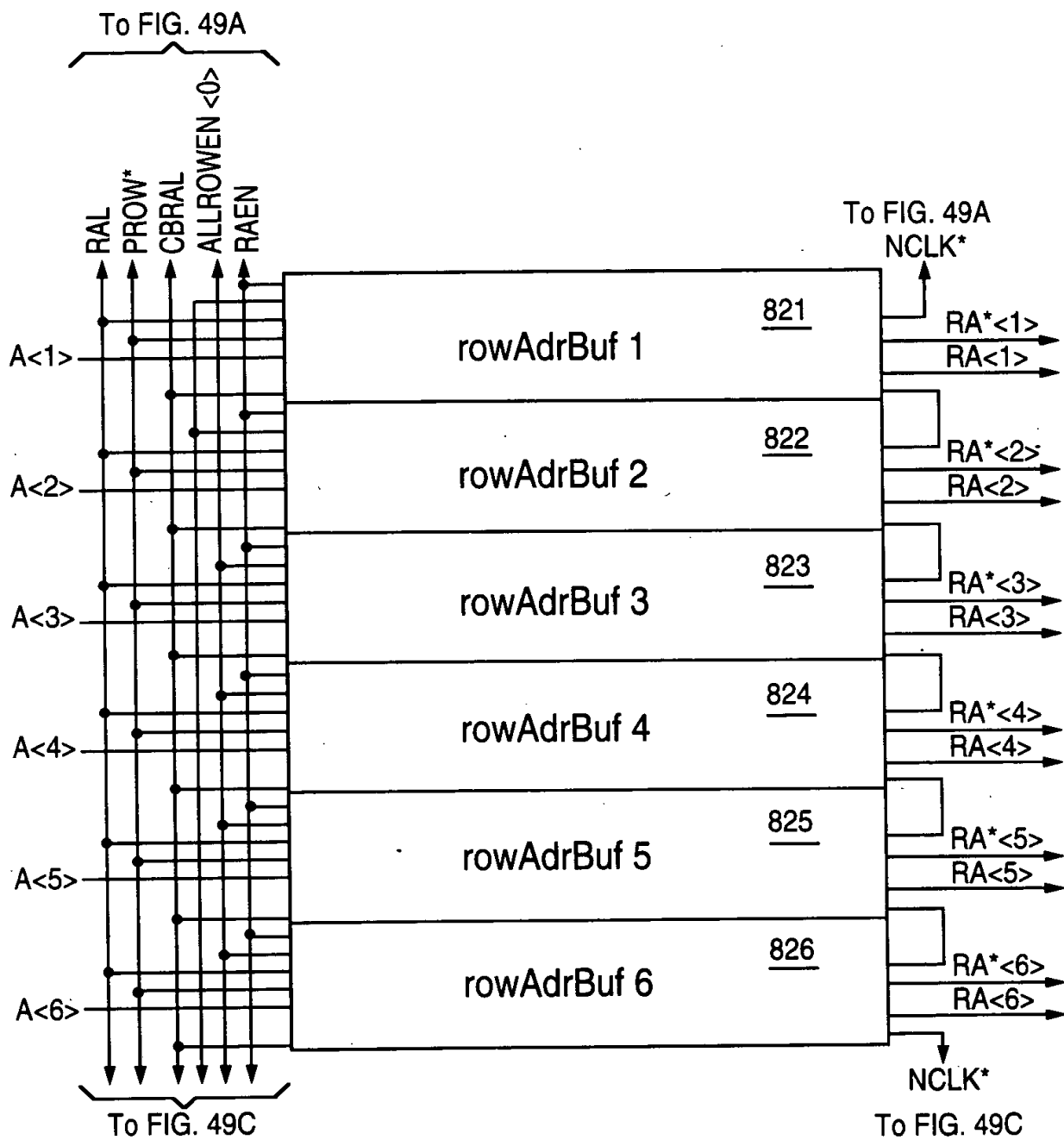
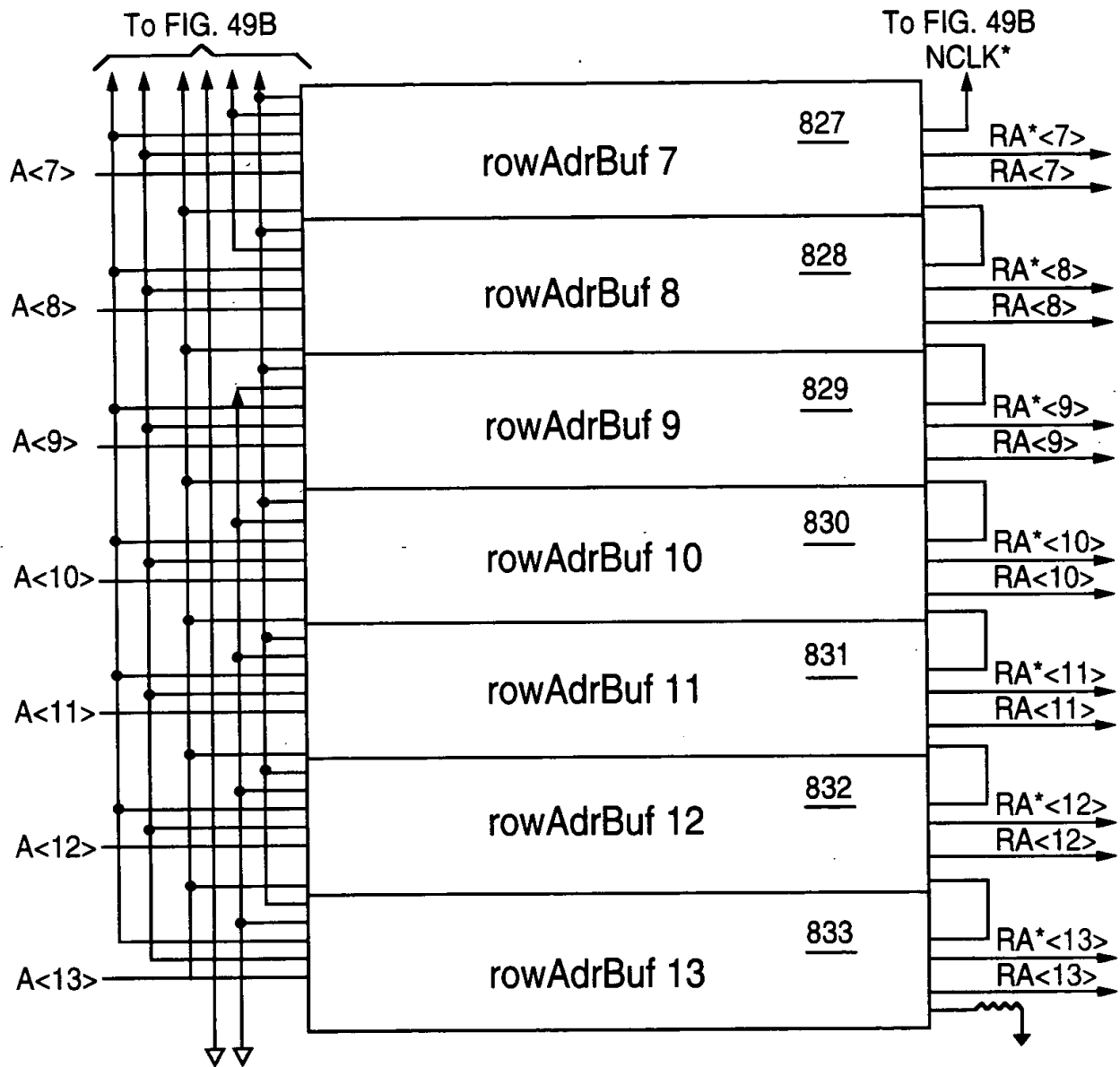


FIG. 49A

**FIG. 49B**

**FIG. 49C**

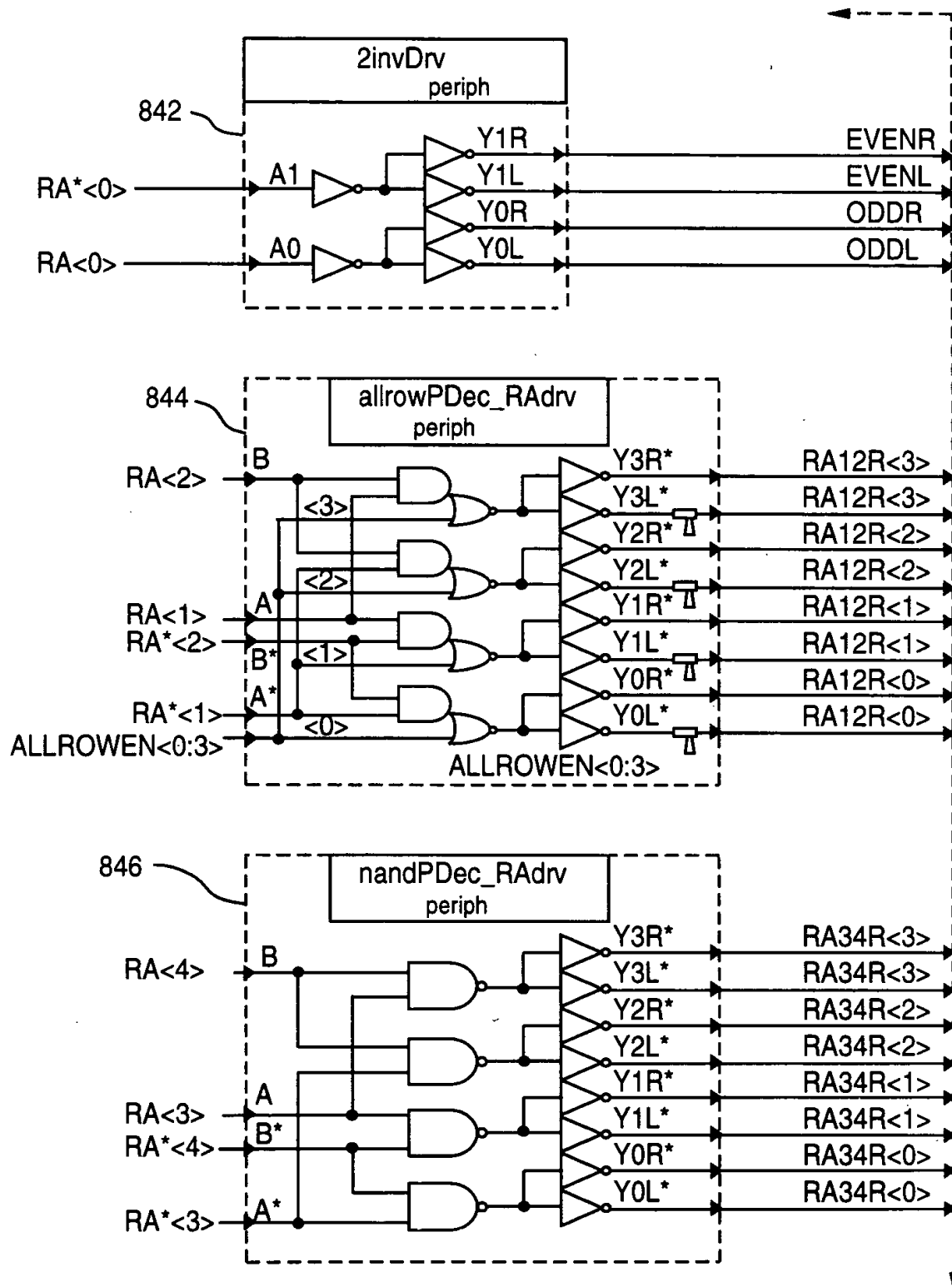
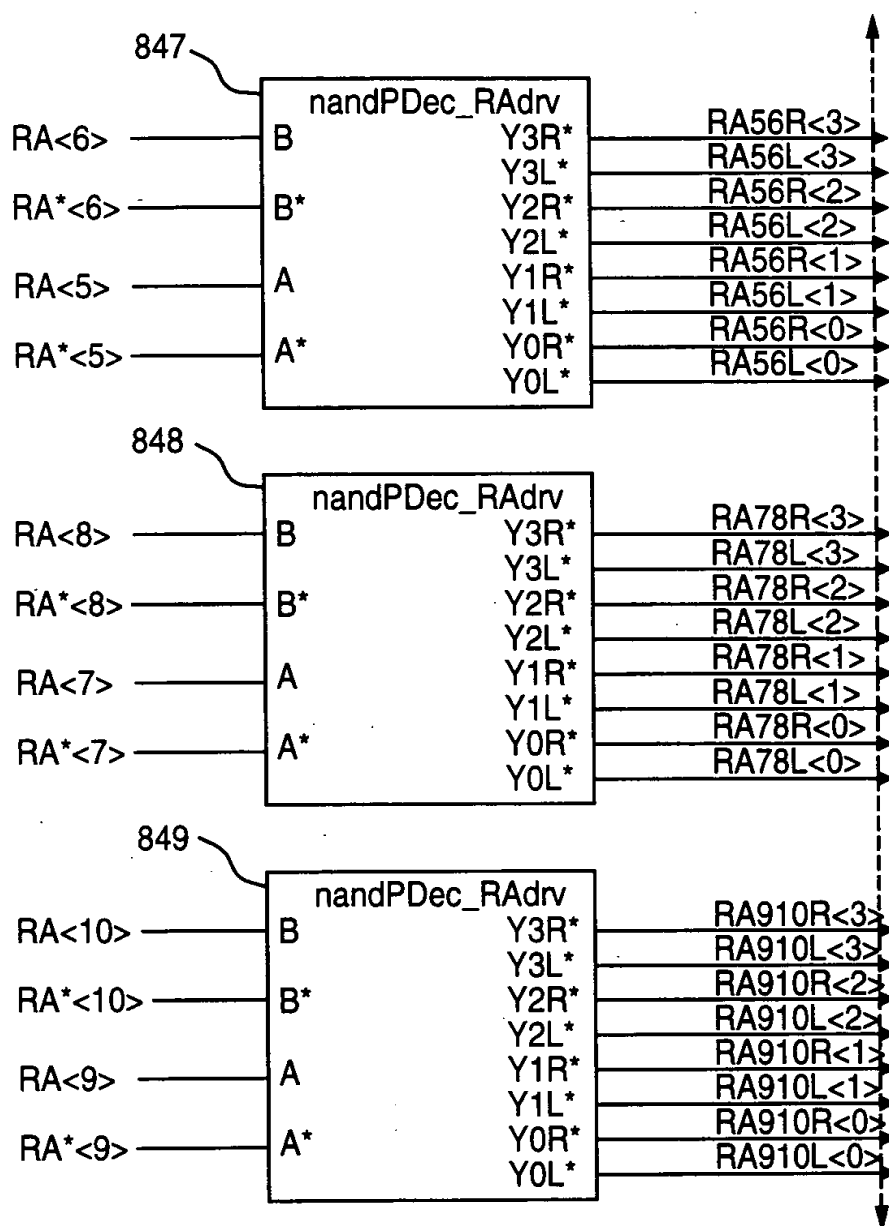


FIG. 50A

**FIG. 50B**

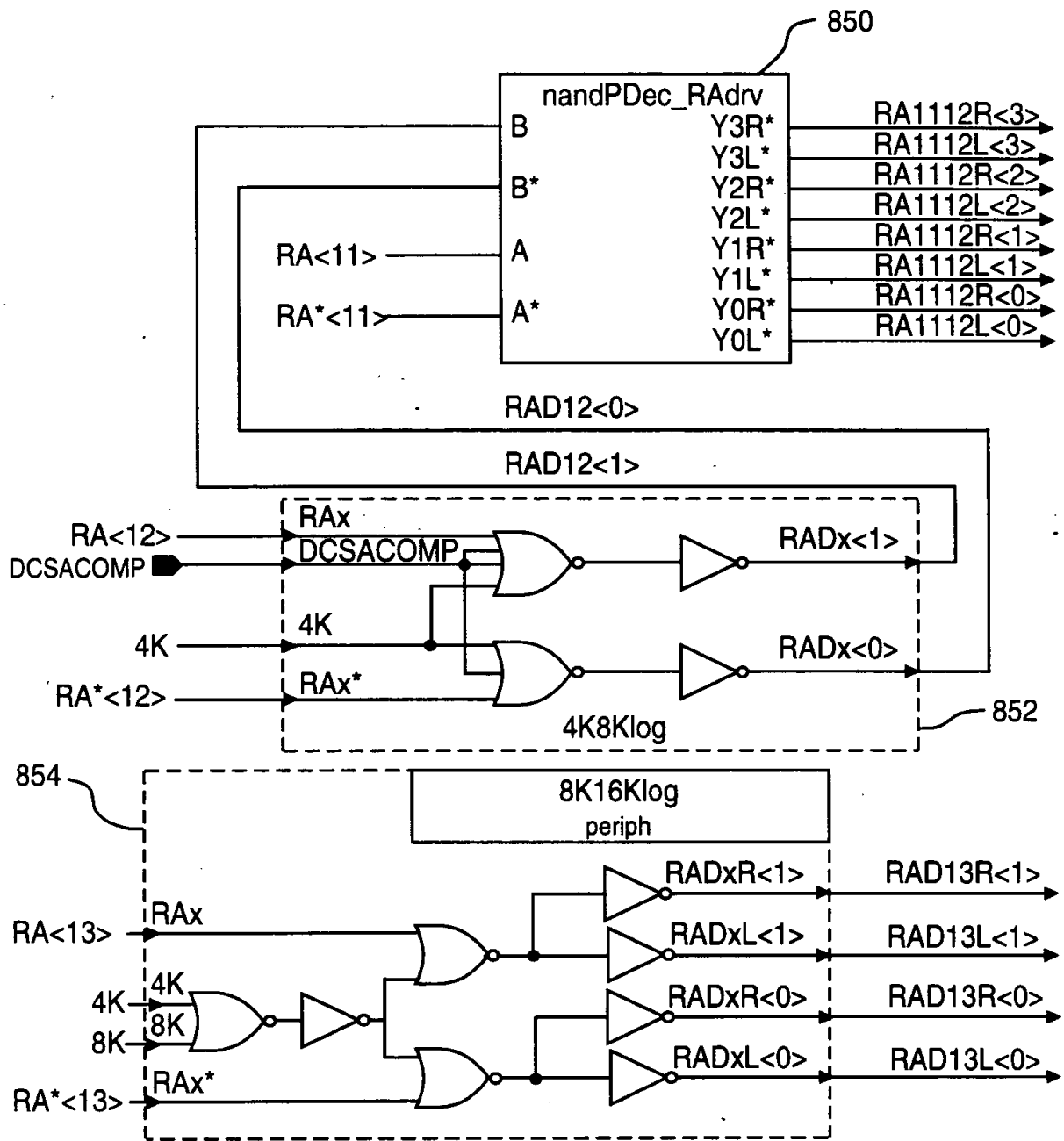


FIG. 50C

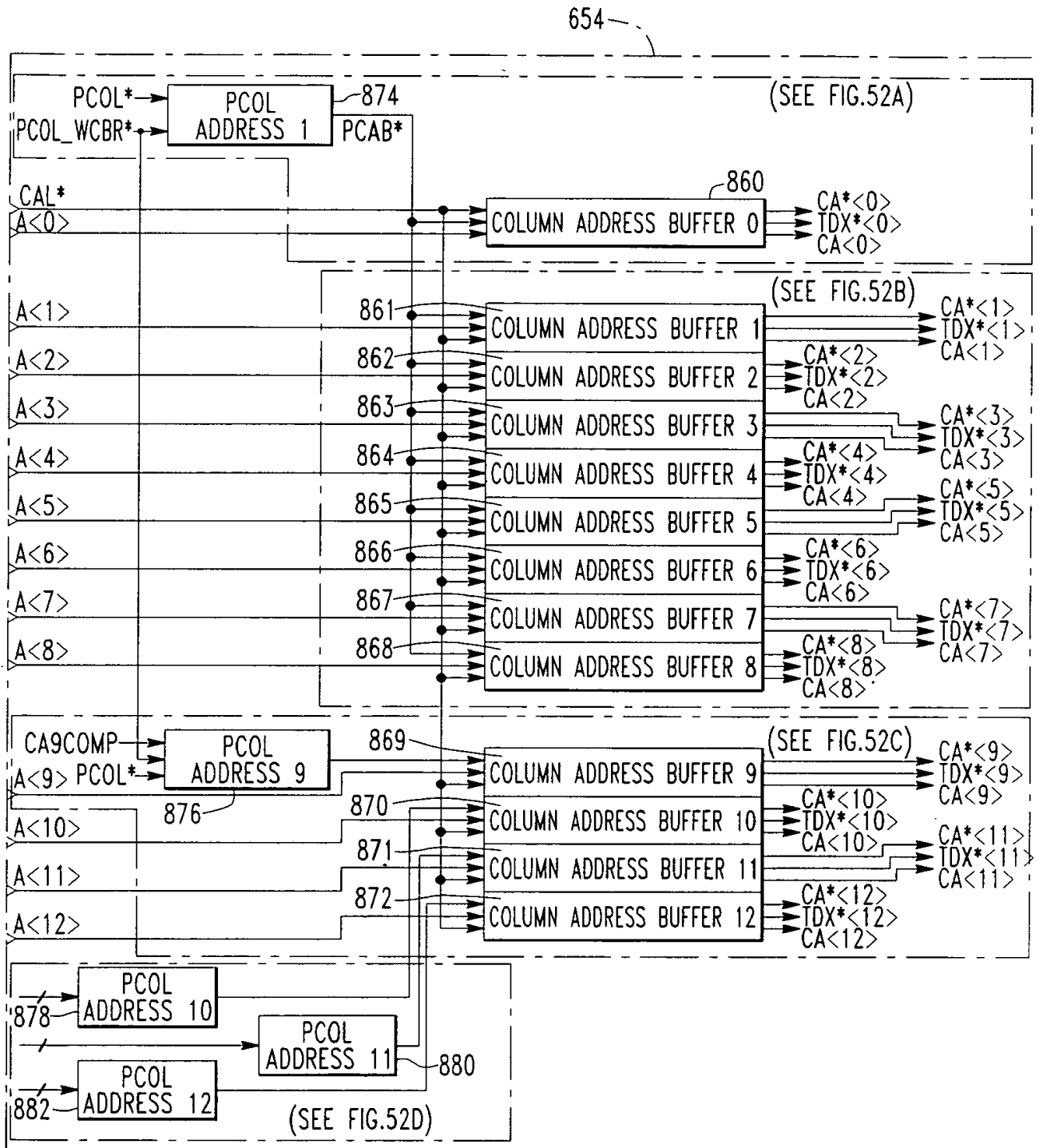


FIG. 51A

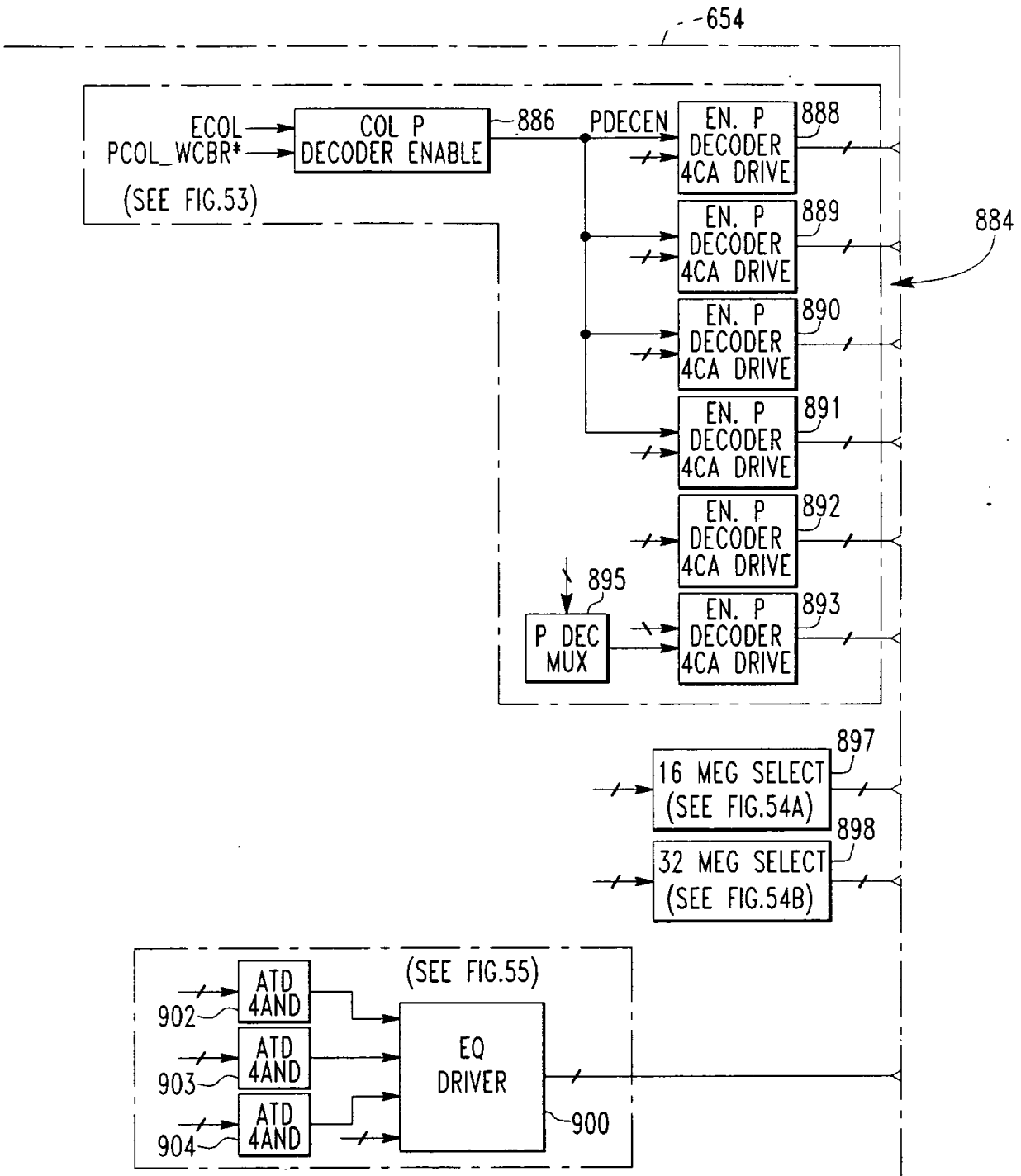
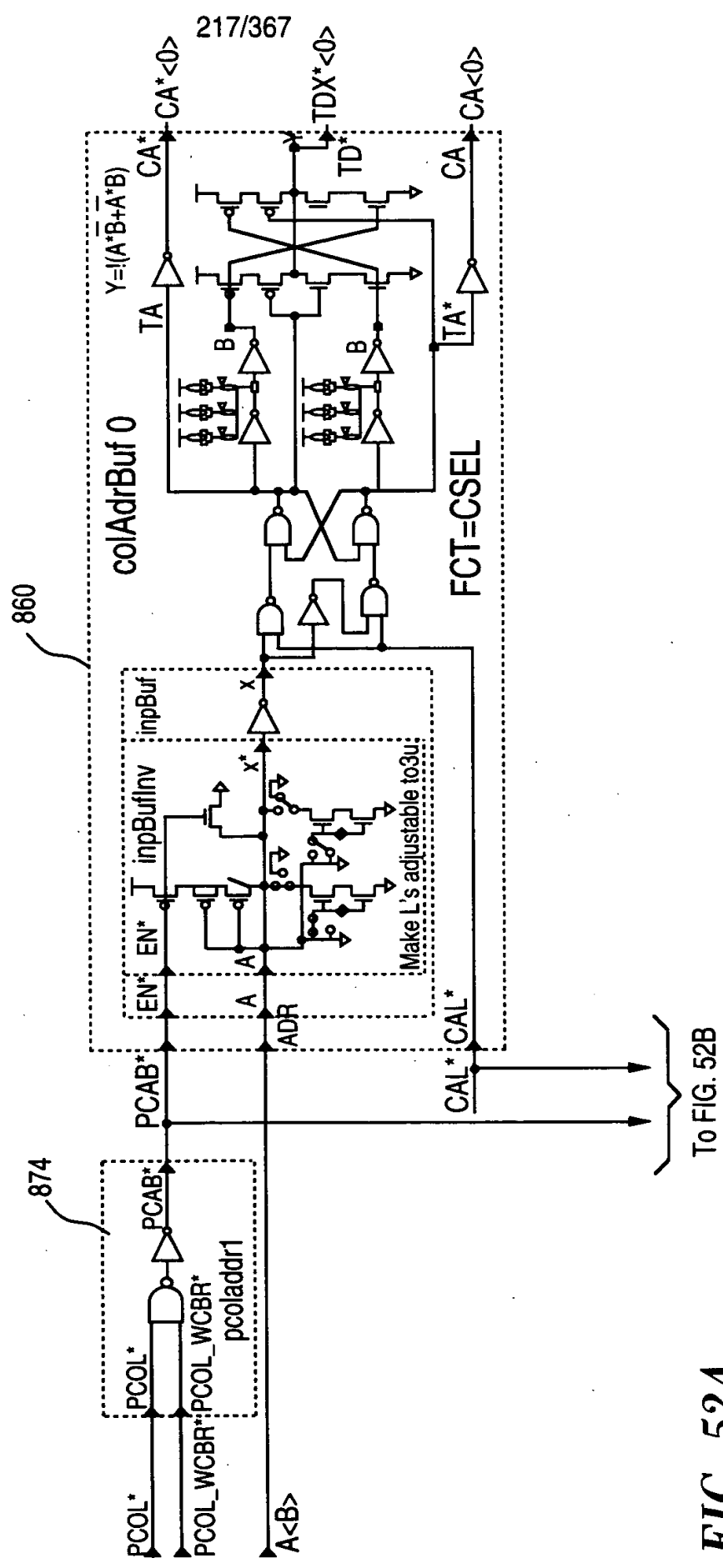


FIG. 51B



To FIG. 52B

FIG. 52A

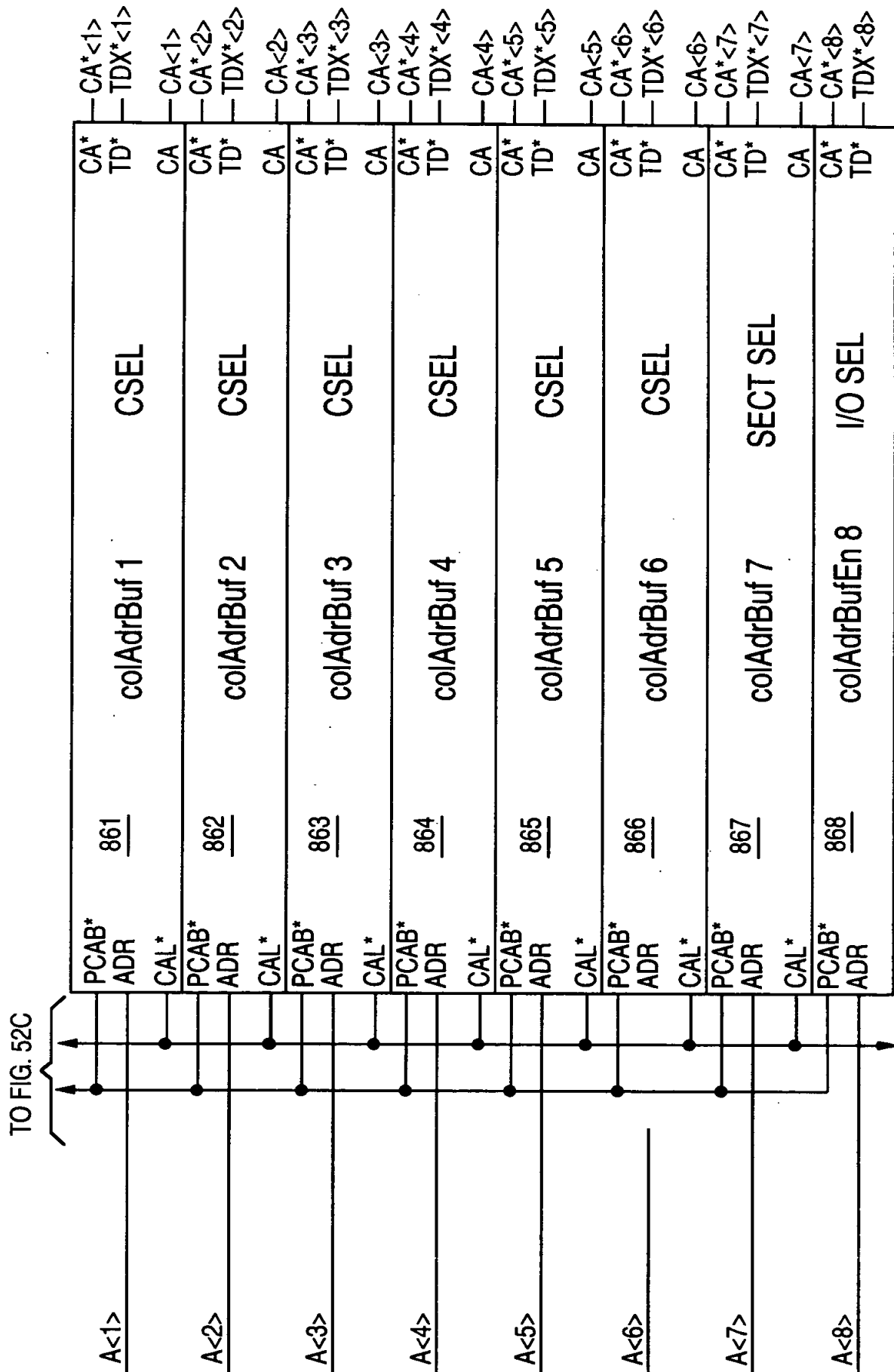
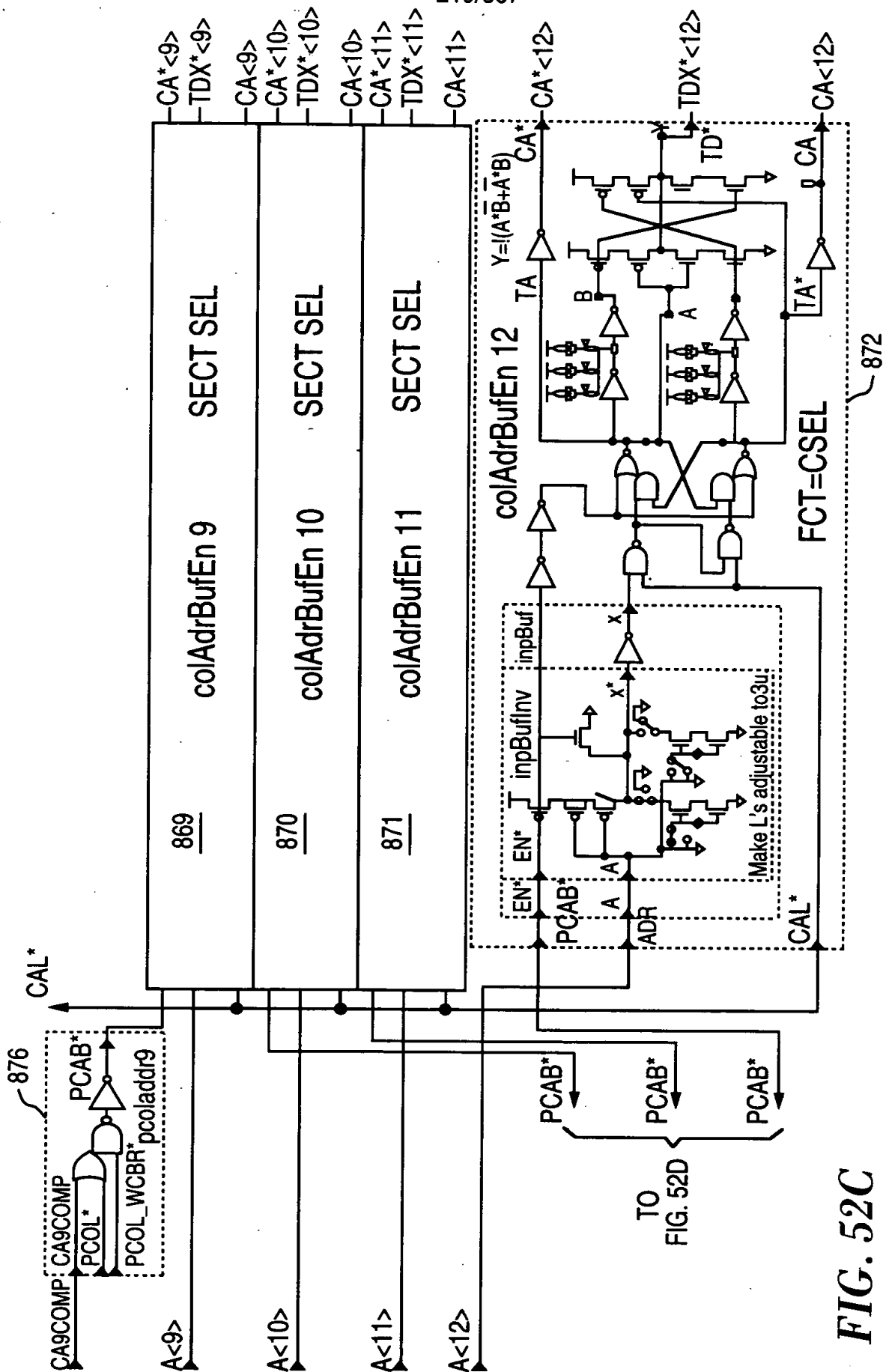
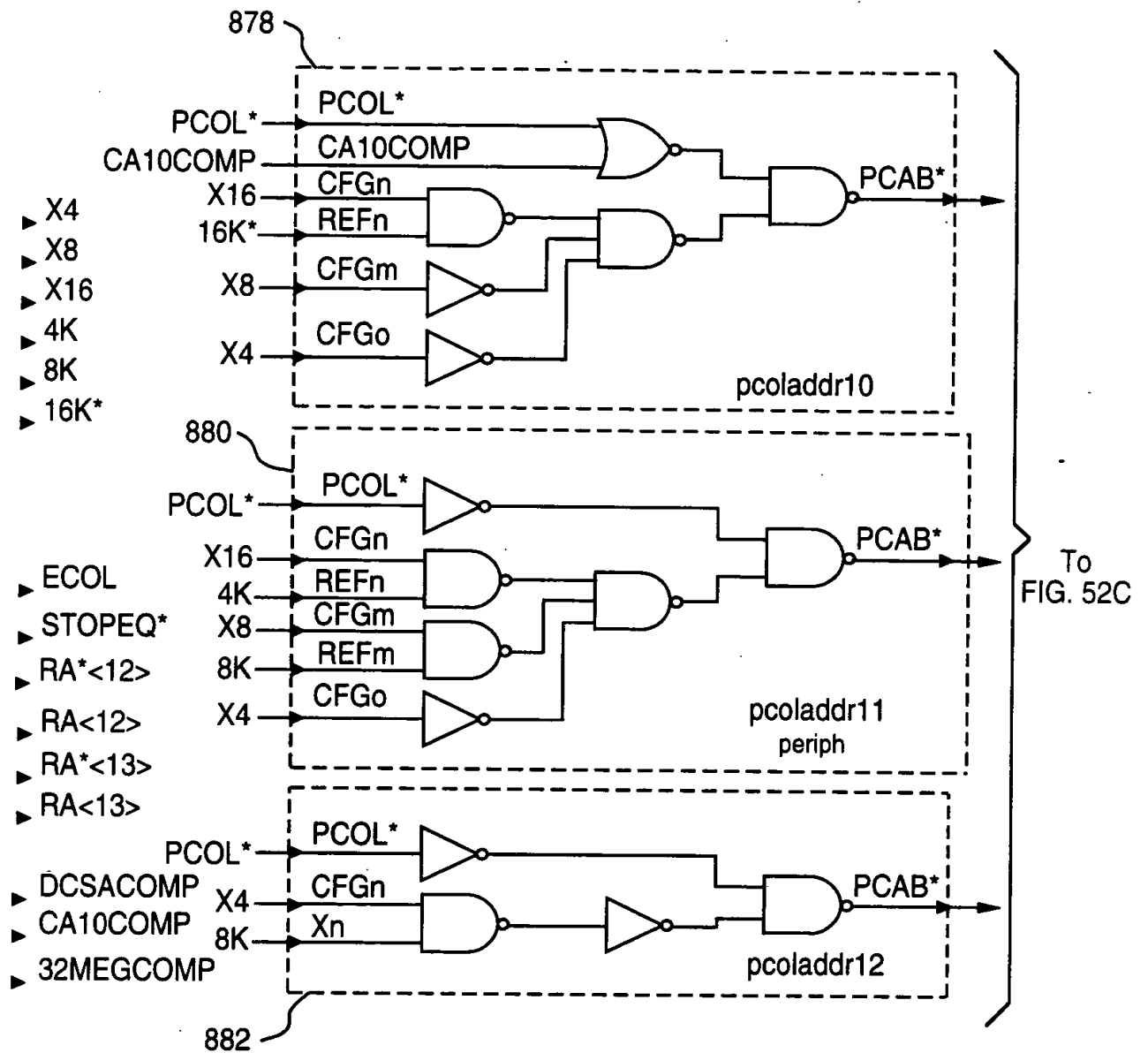


FIG. 52B



**FIG. 52D**

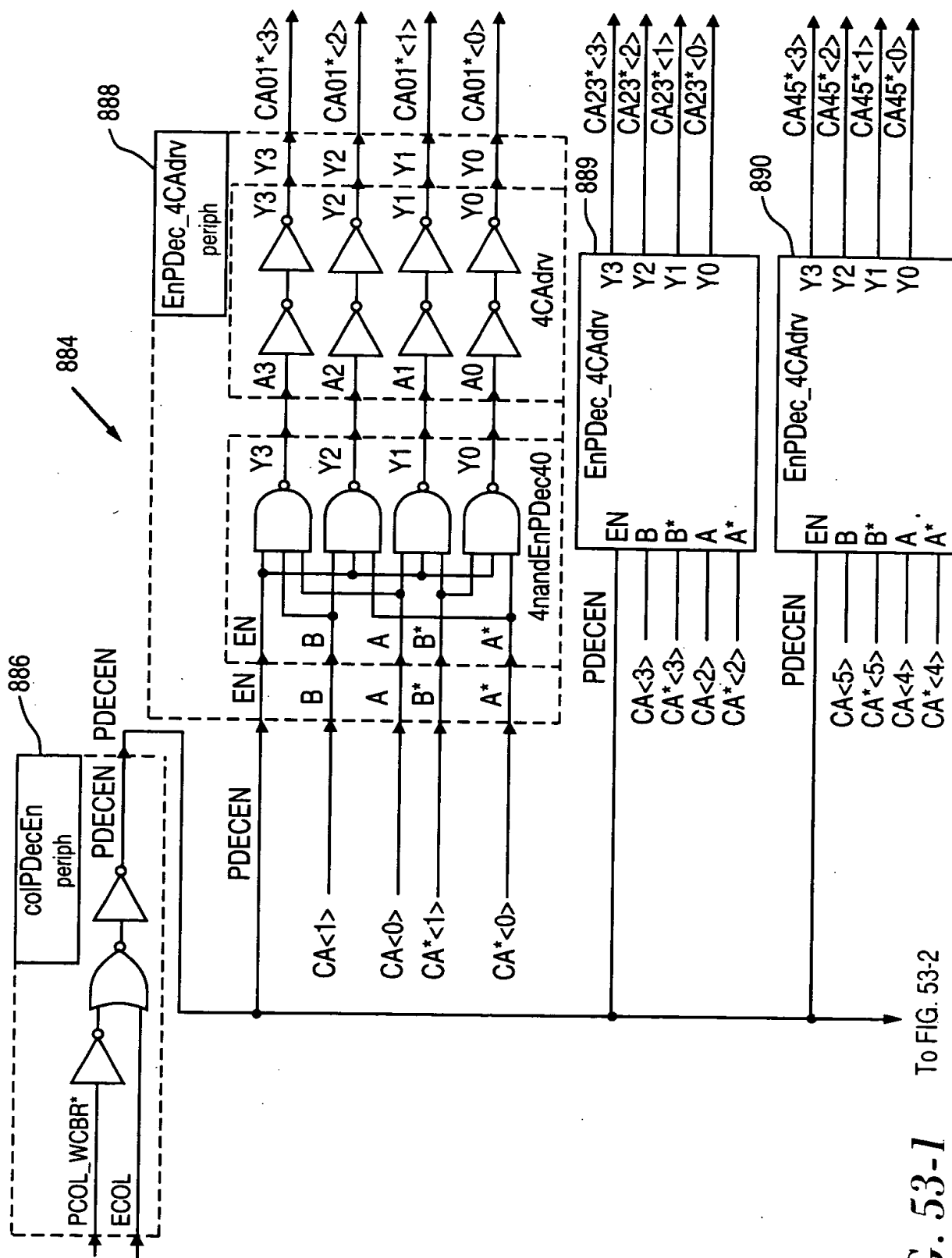


FIG. 53-1 To FIG. 53-2

To FIG. 53-1

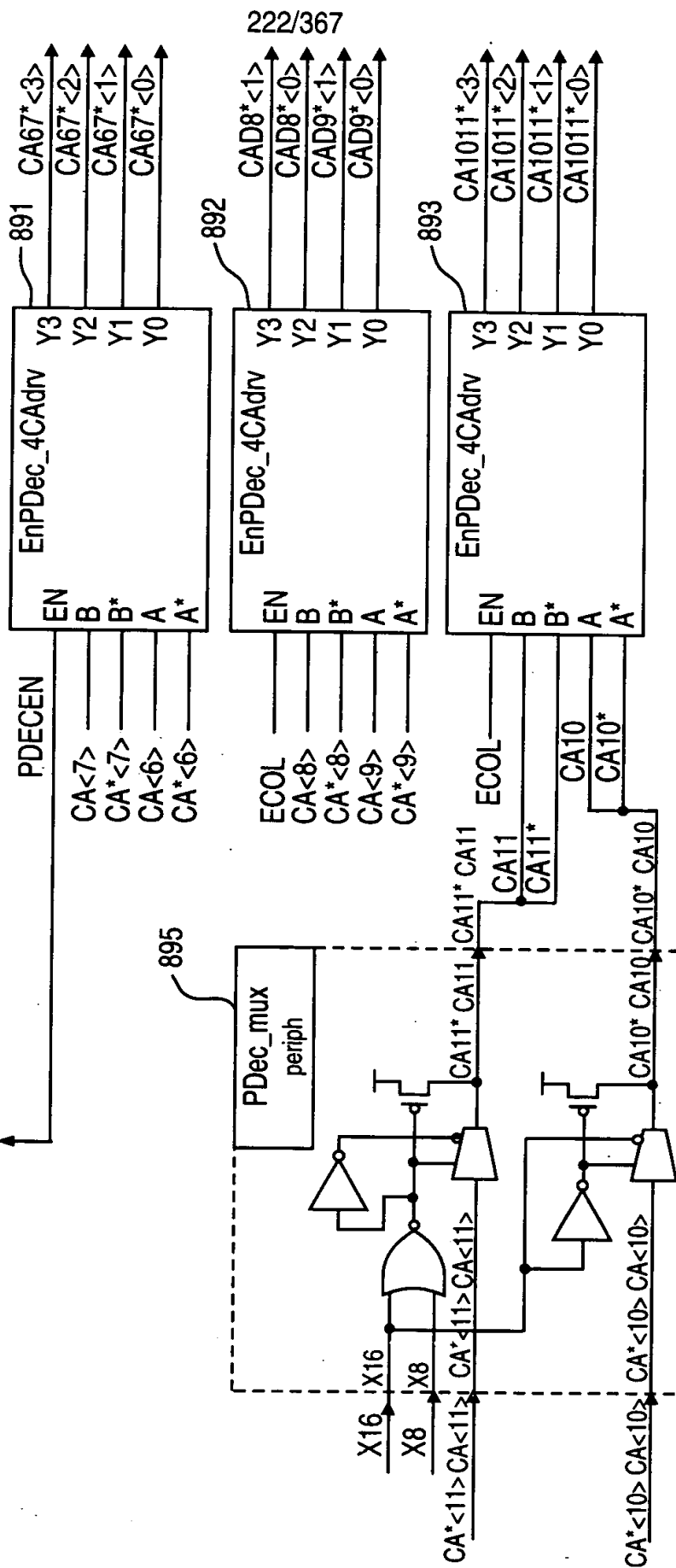


FIG. 53-2

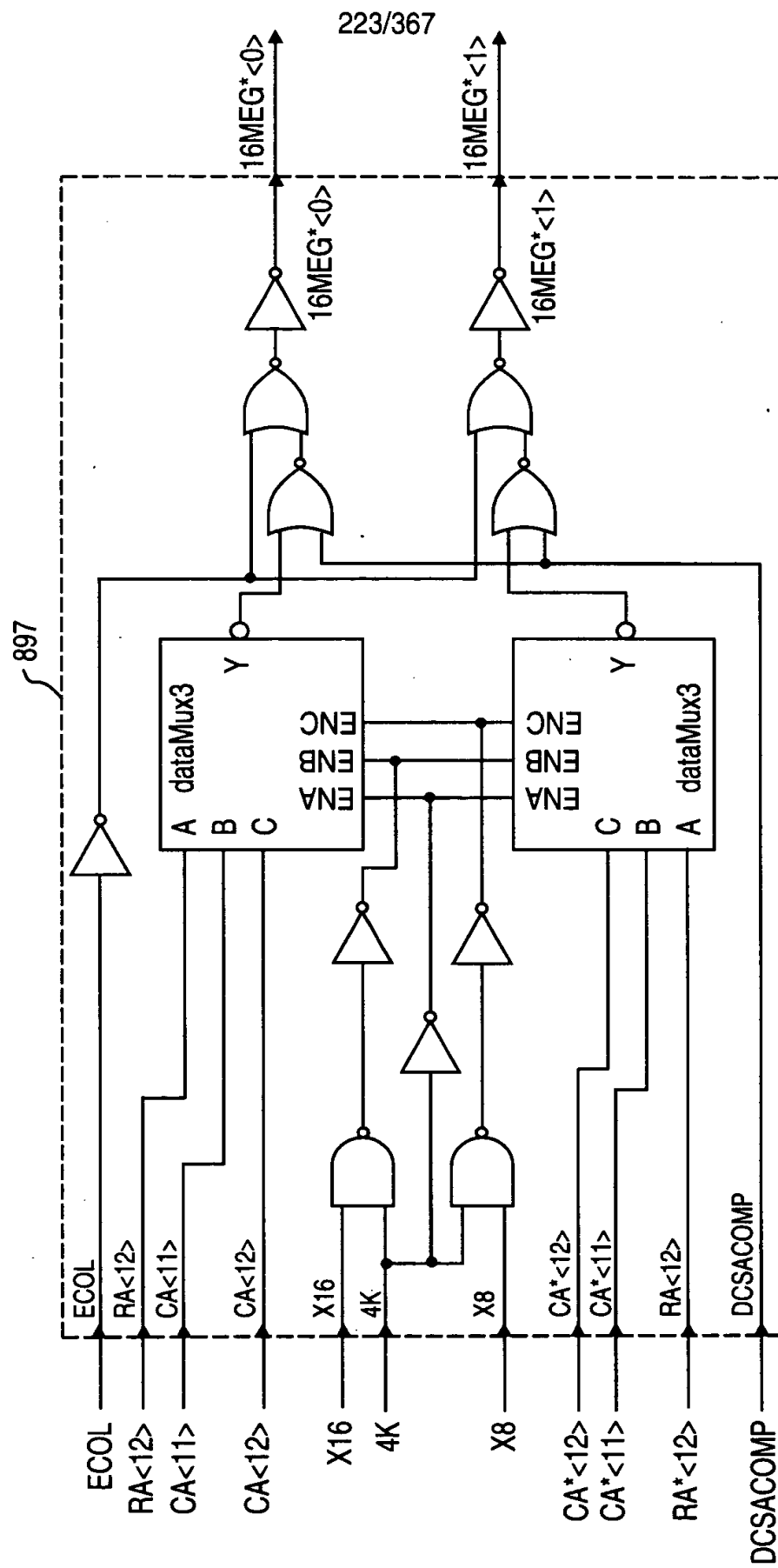


FIG. 54A

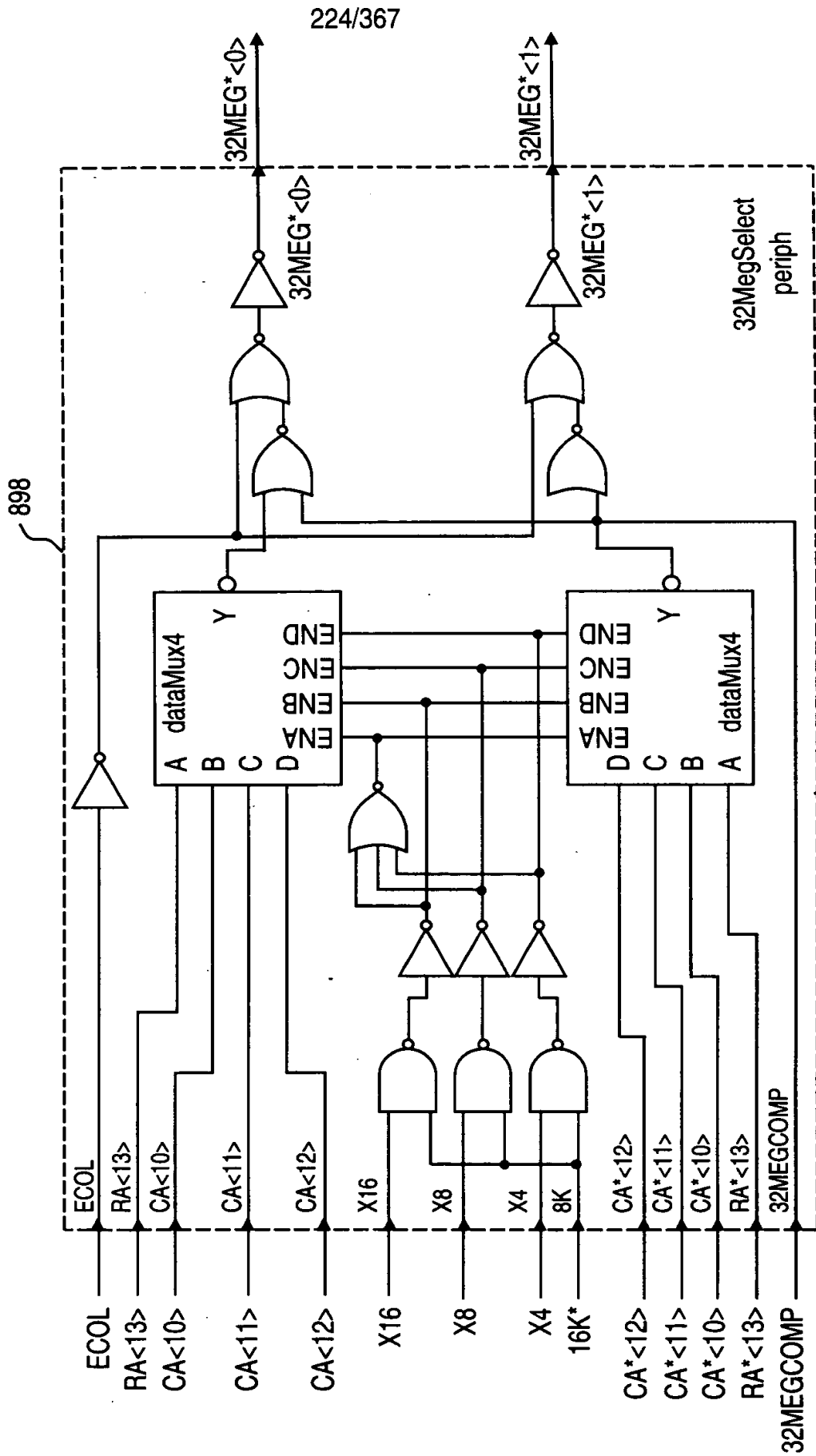


FIG. 54B

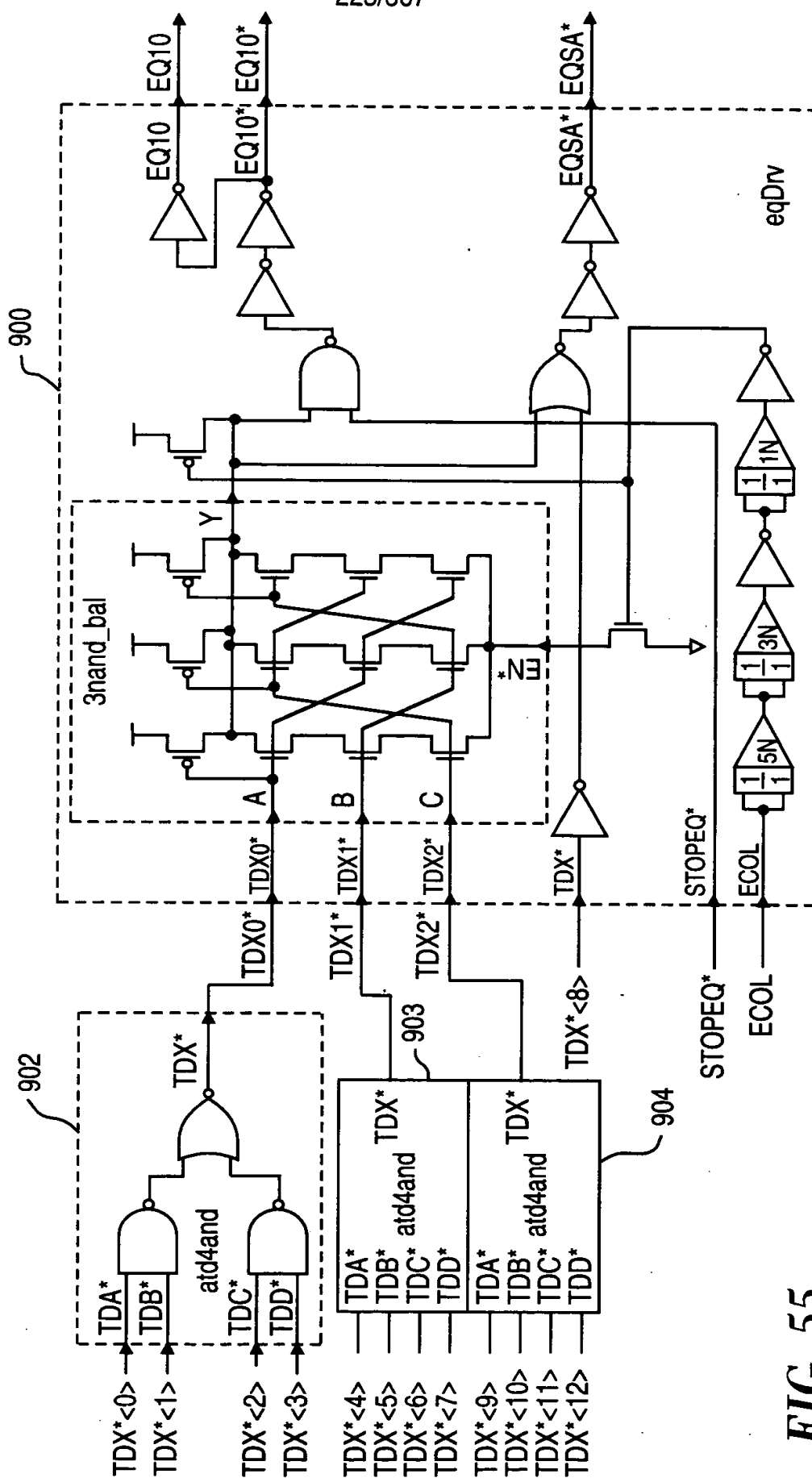


FIG. 55

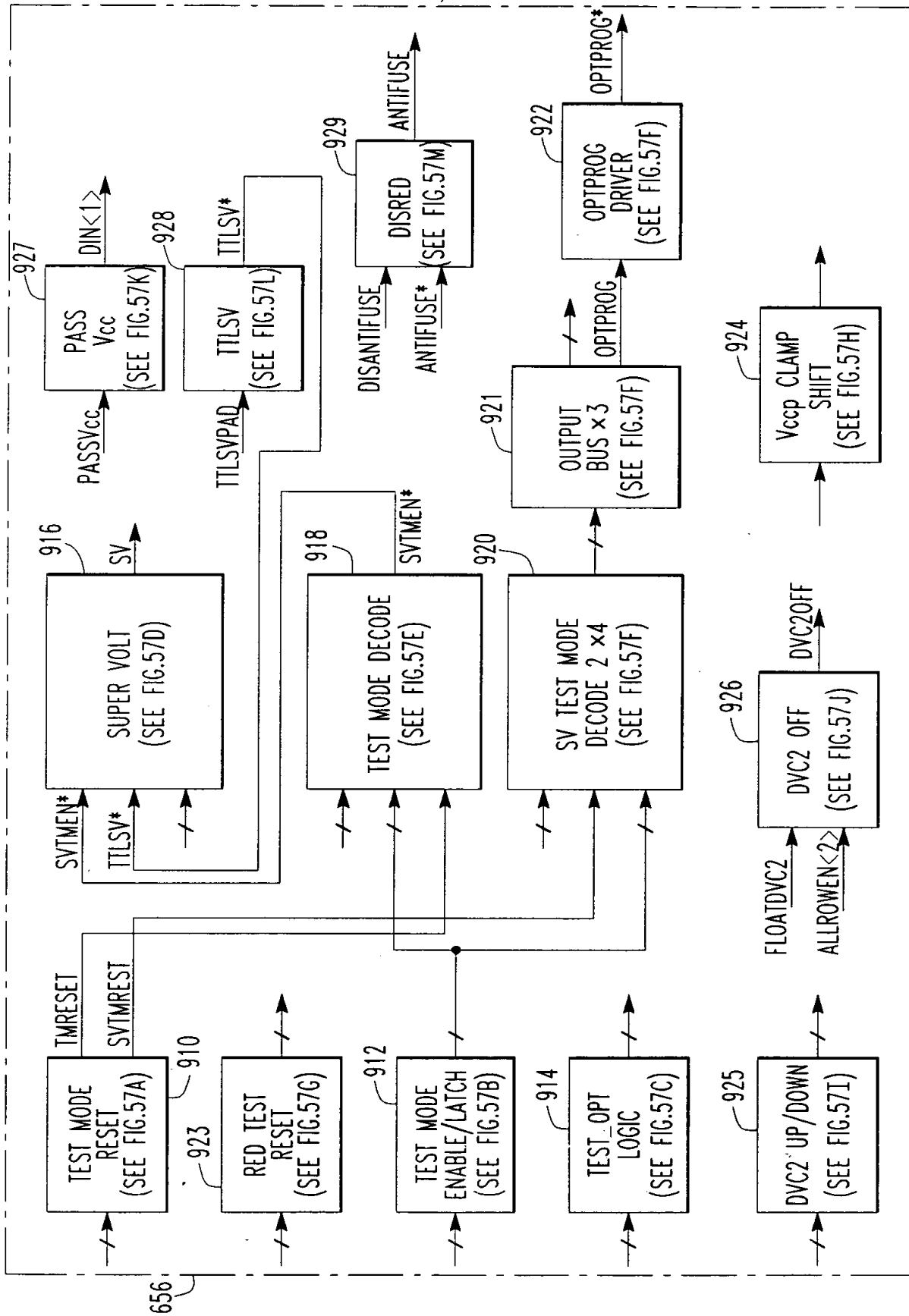


FIG. 56

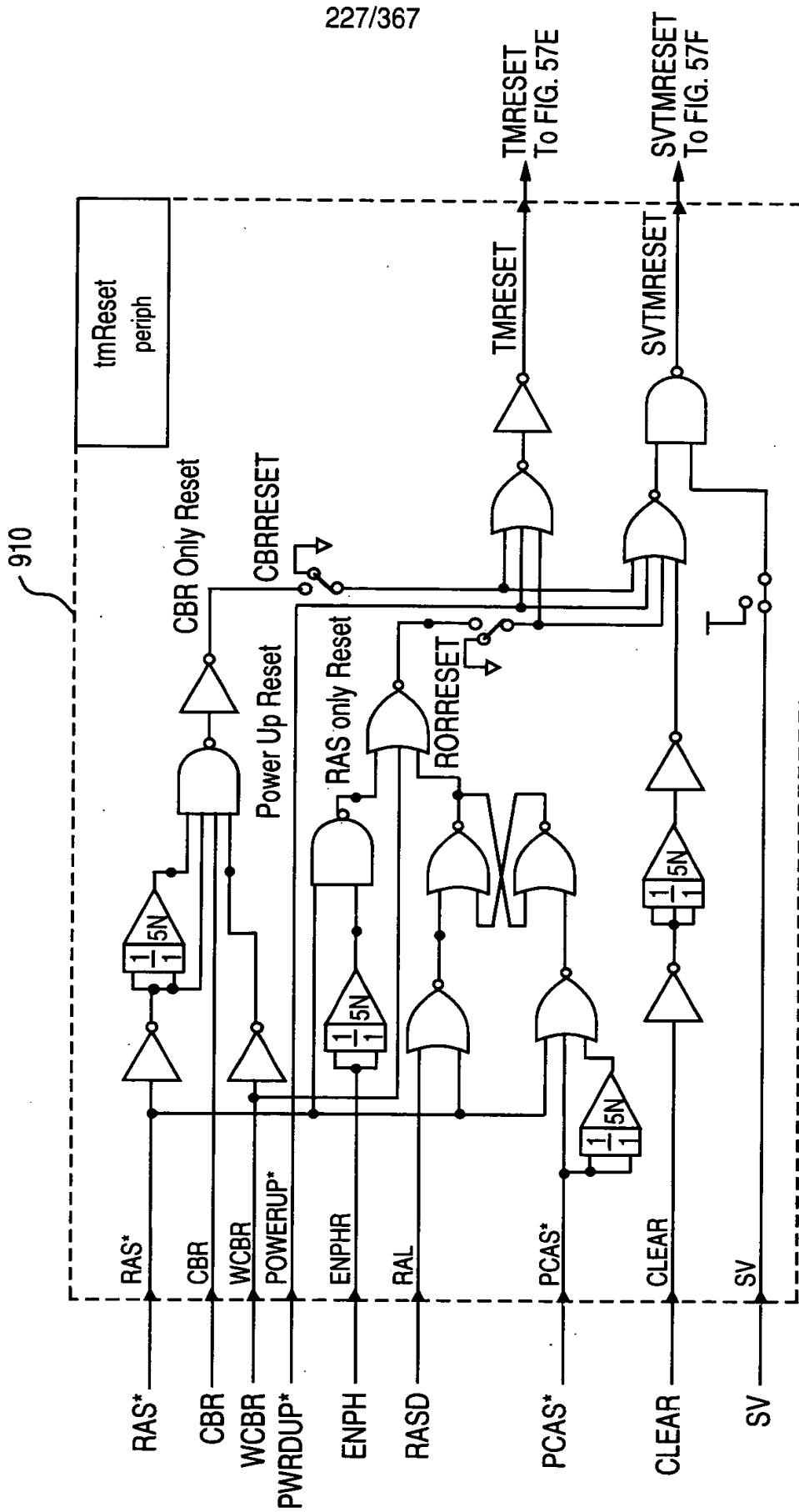


FIG. 57A

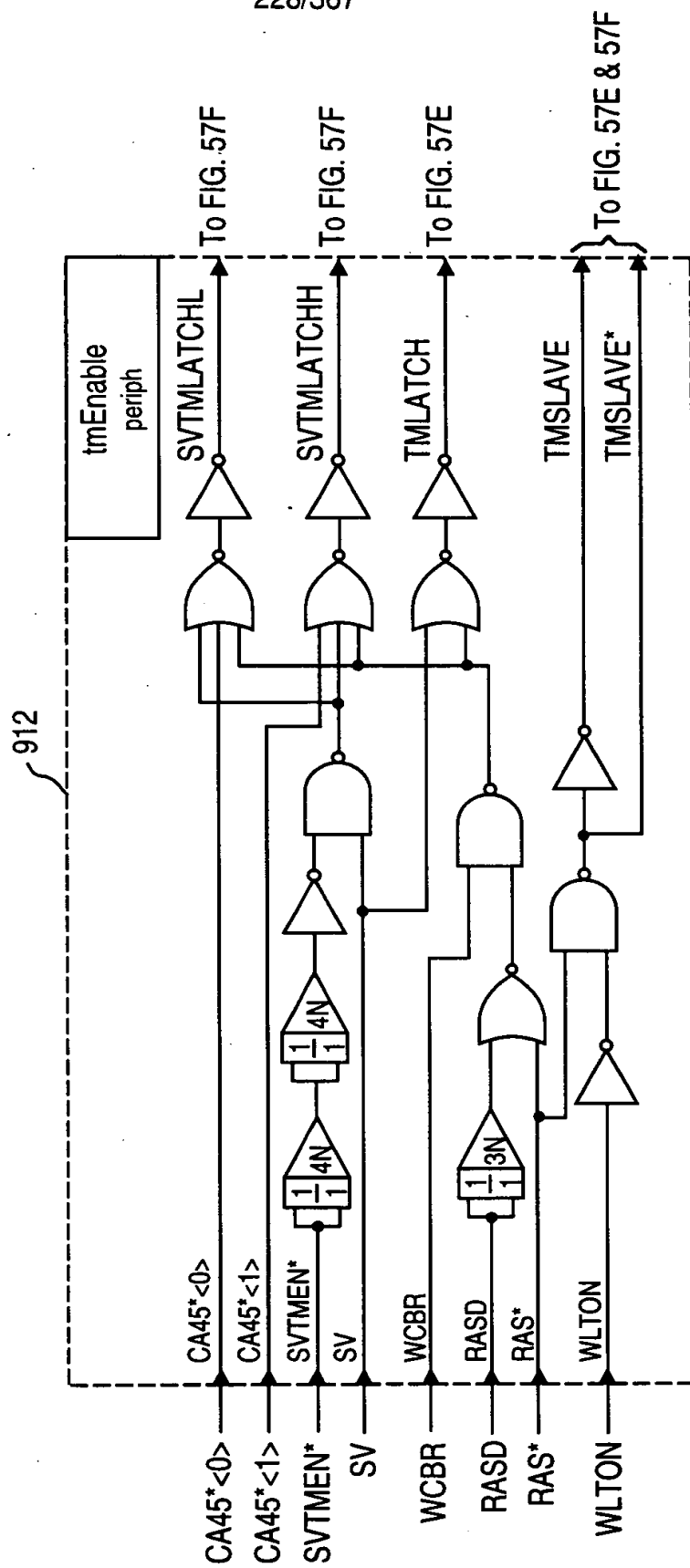


FIG. 57B

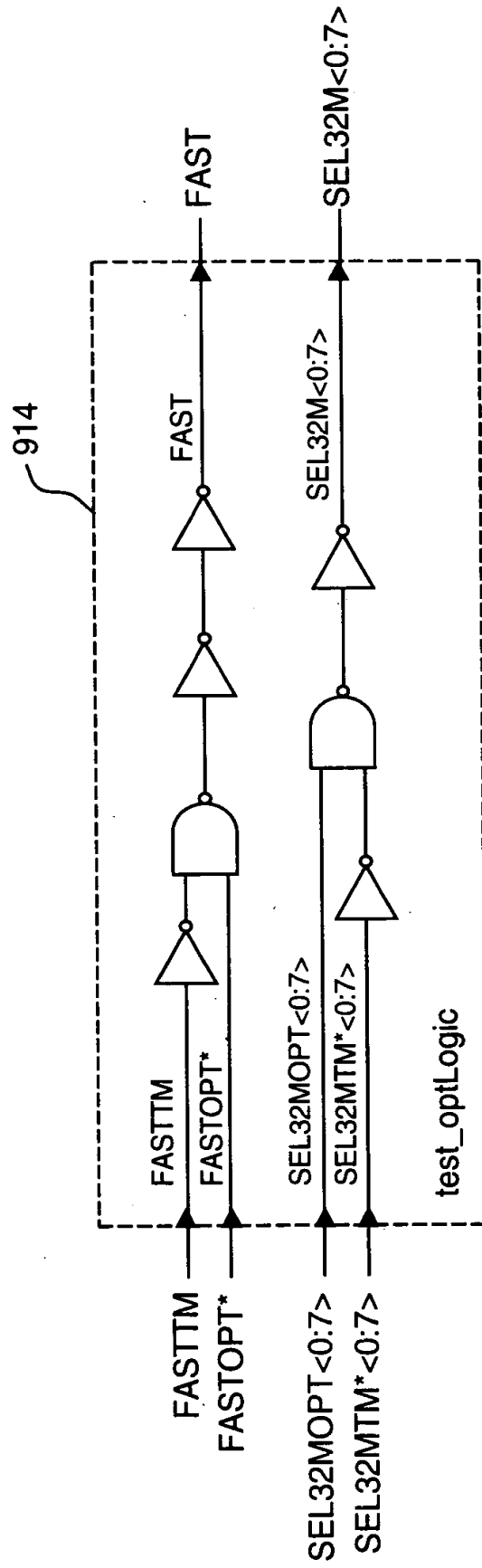
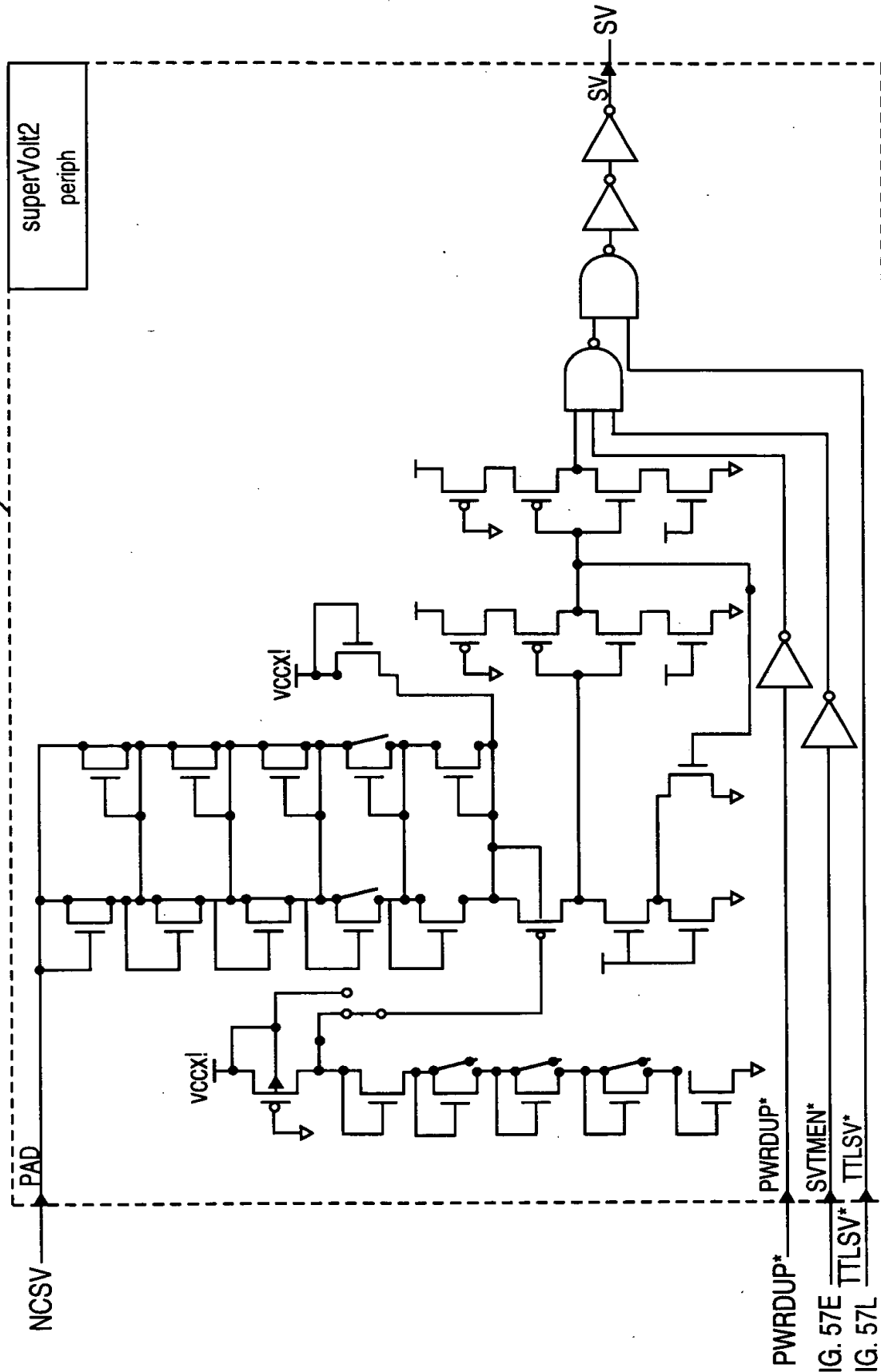


FIG. 57C

916



From FIG. 57E
From FIG. 57L

FIG. 57D

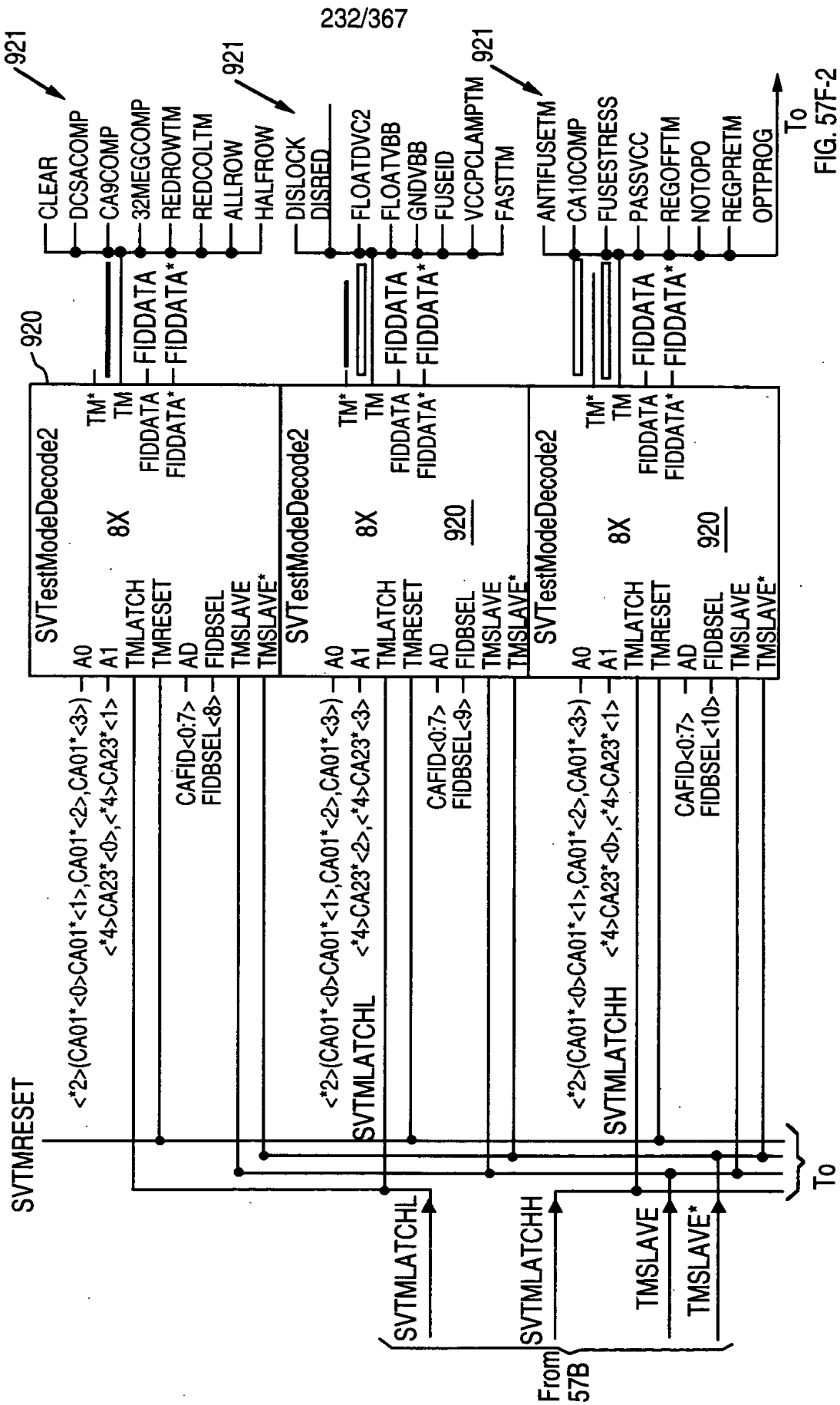


FIG. 57F-3

FIG. 57F-1

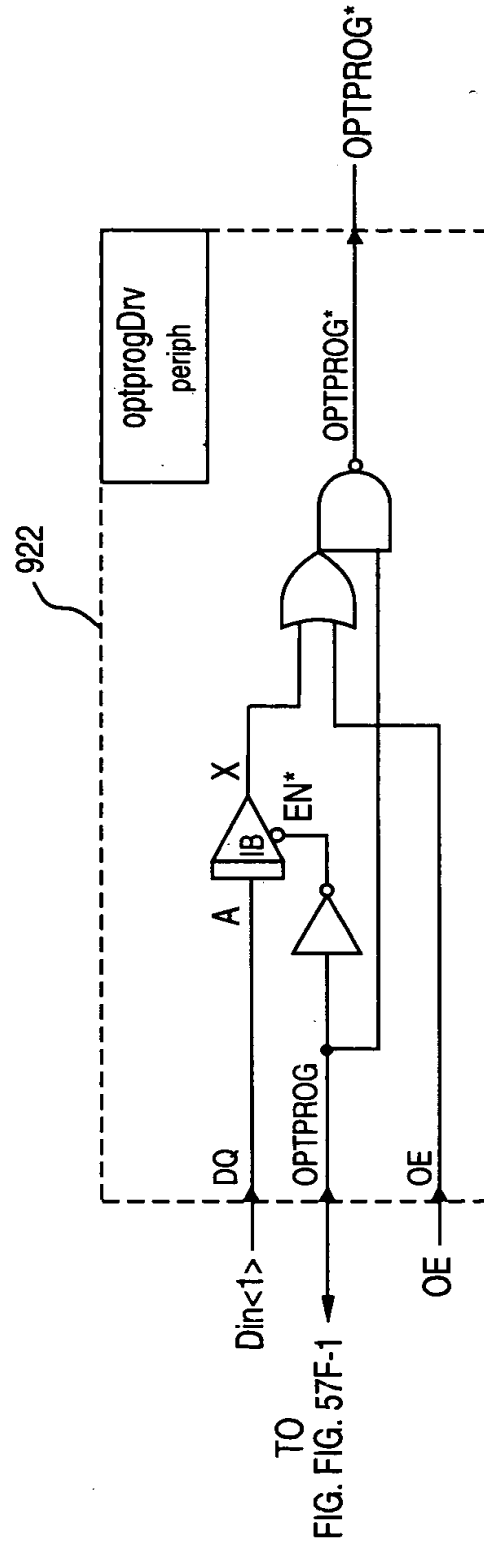


FIG. 57F-1

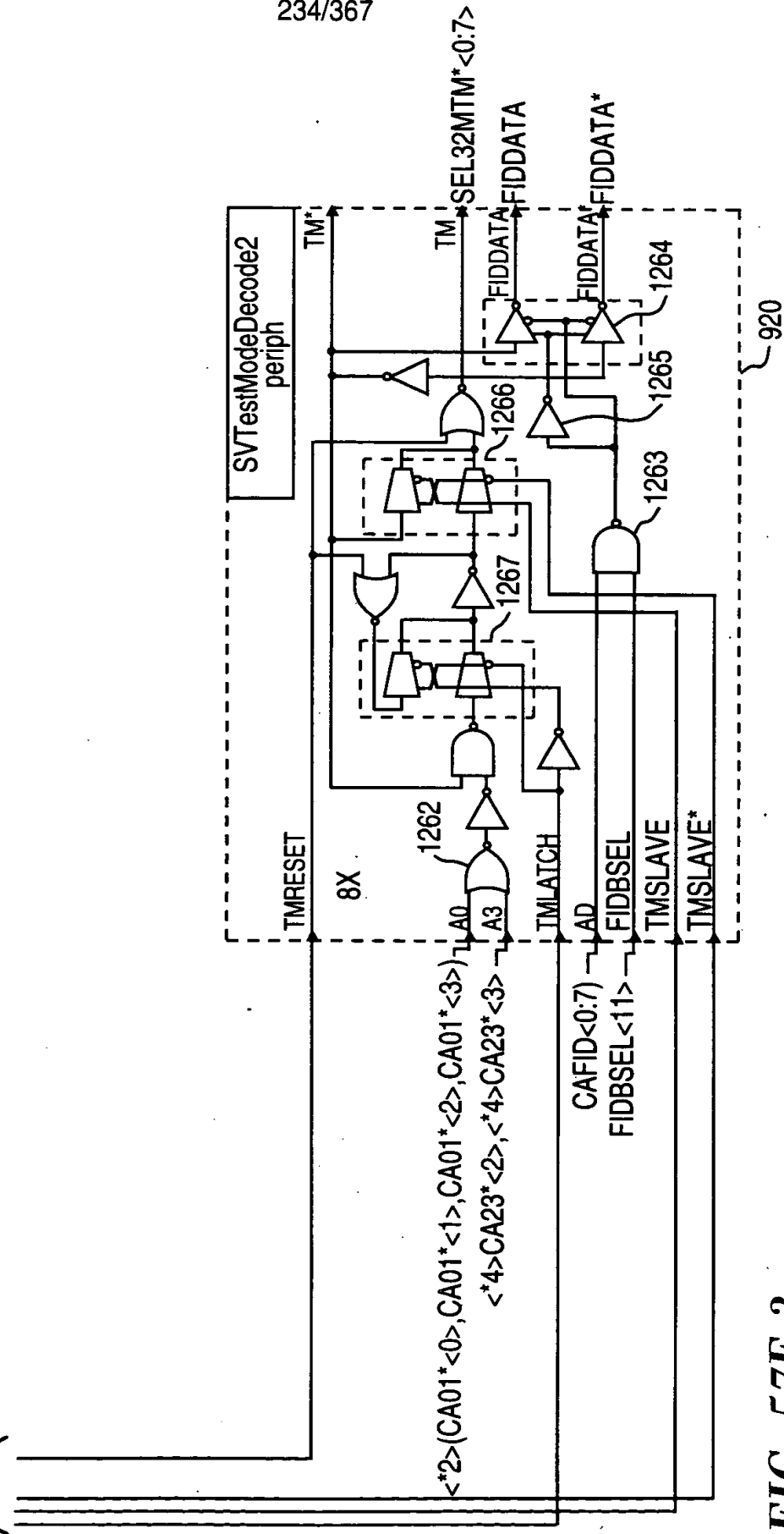


FIG. 57F-3

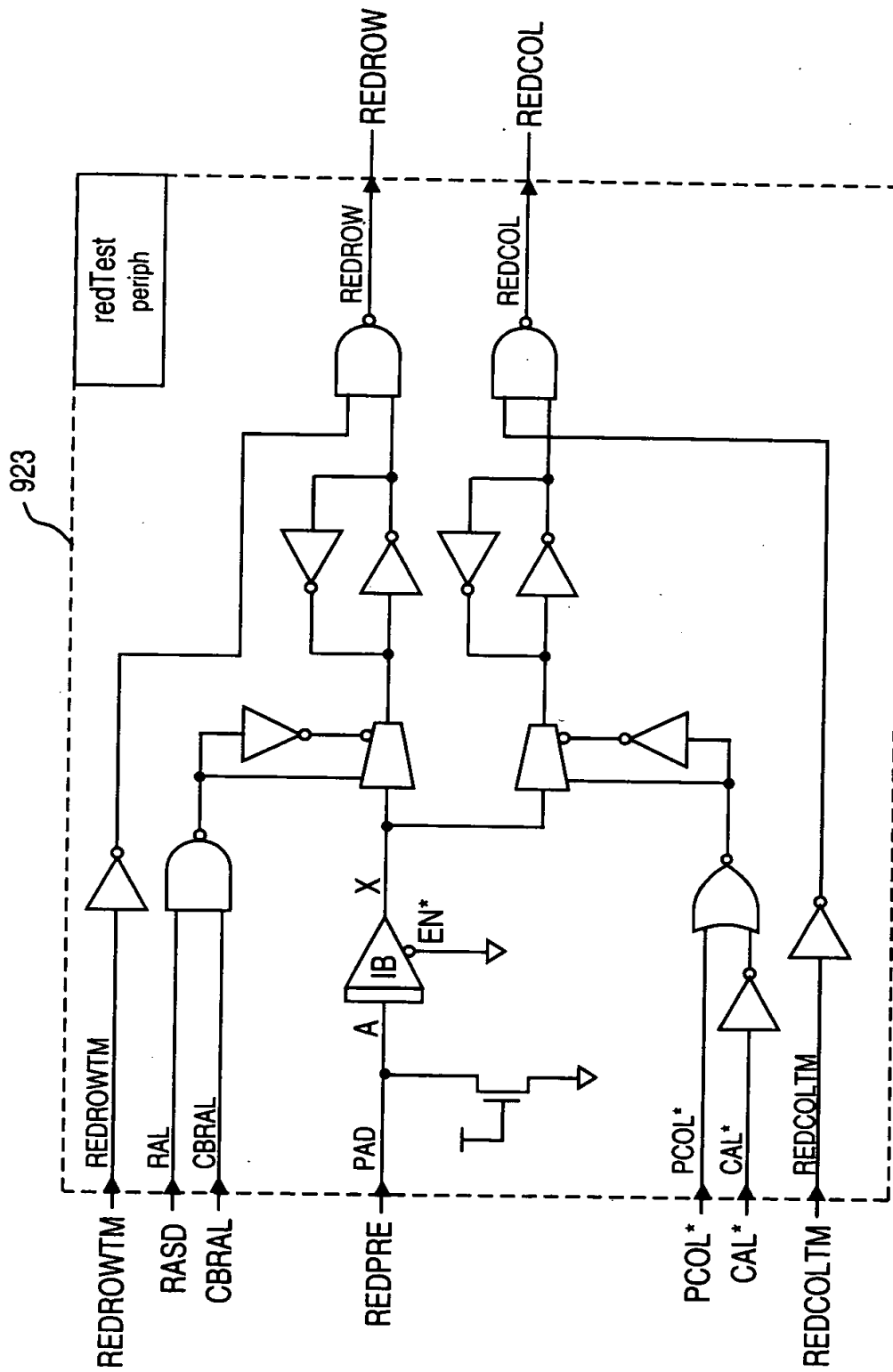
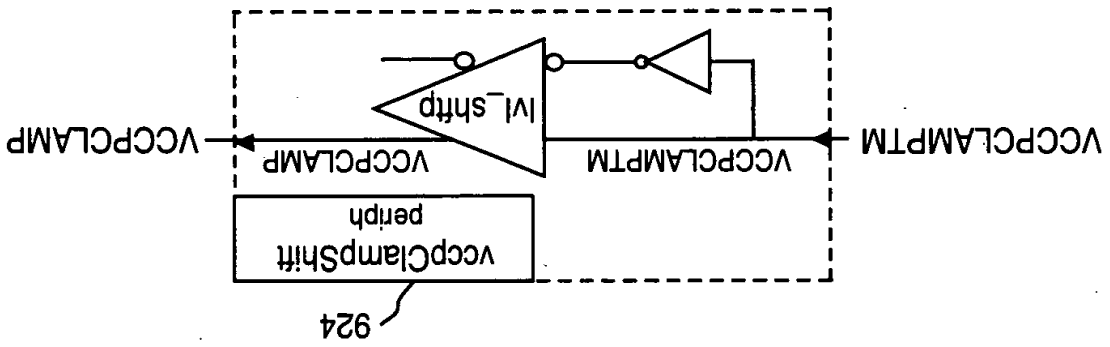
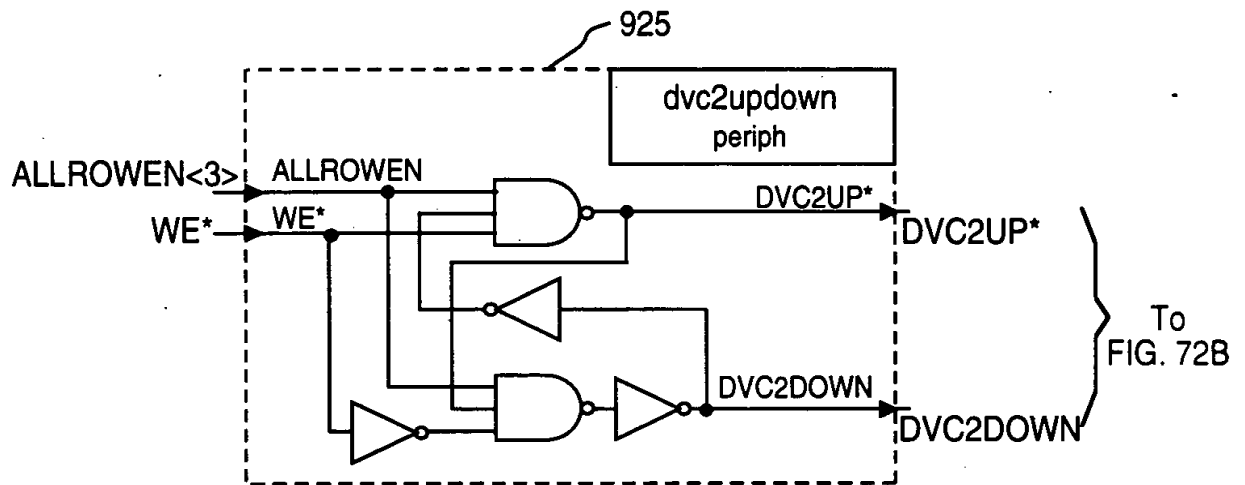
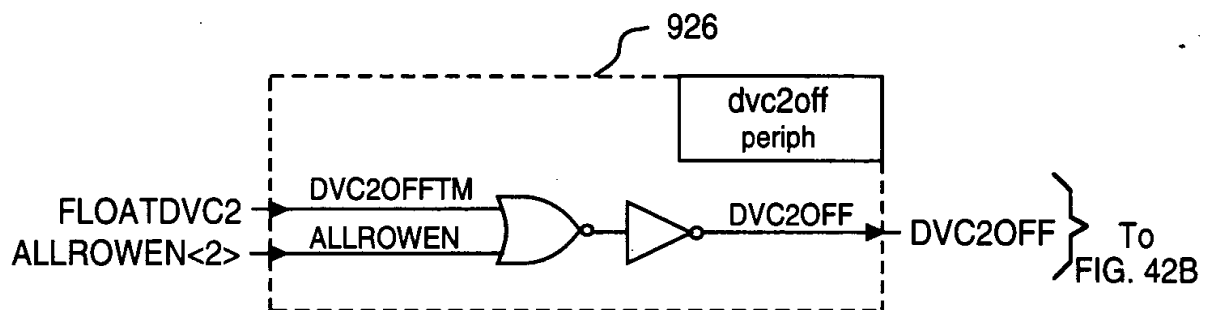


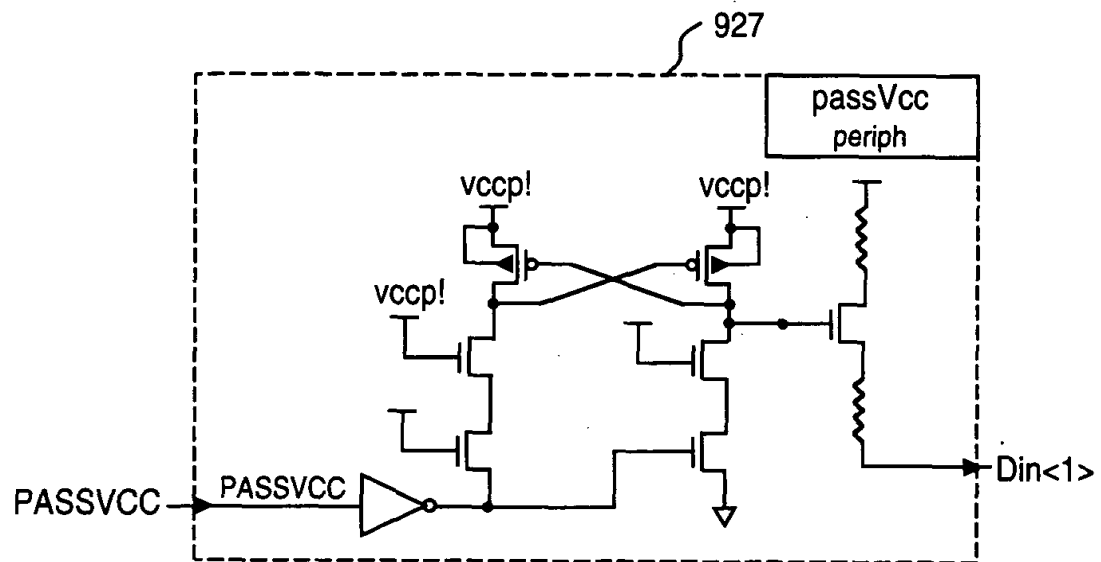
FIG. 57C

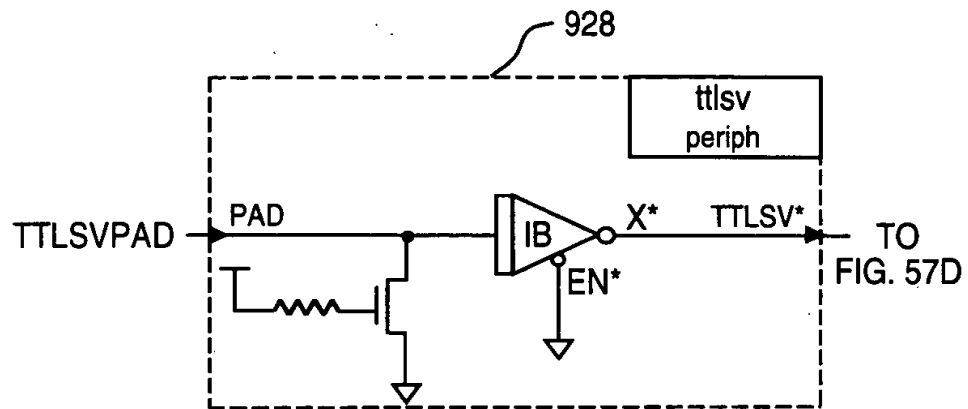
FIG. 57H

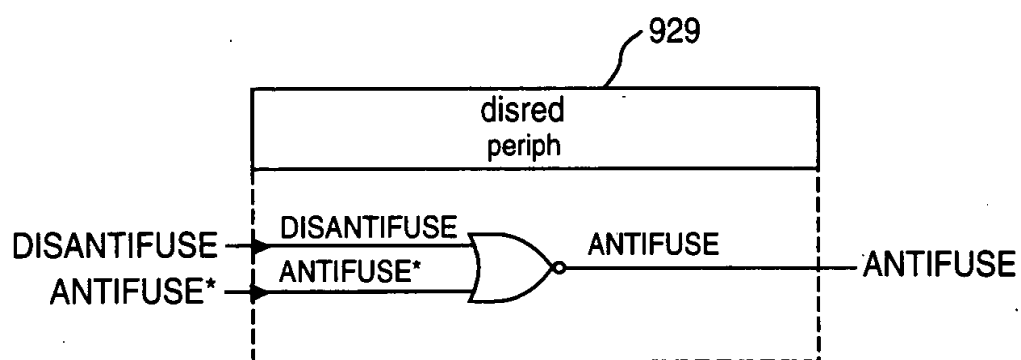


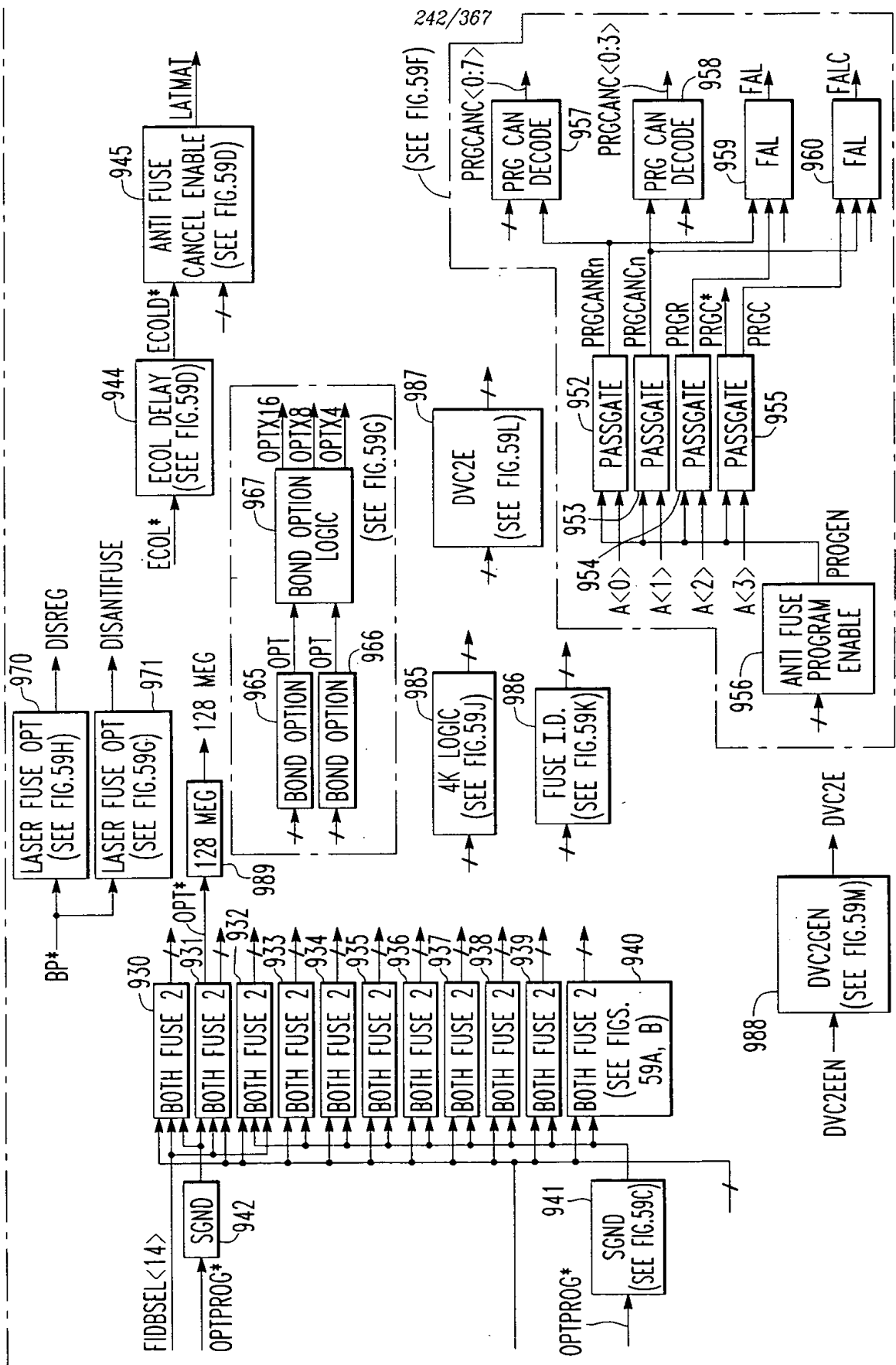
**FIG. 57I**

**FIG. 57J**

**FIG. 57K**

**FIG. 57L**

**FIG. 57M**



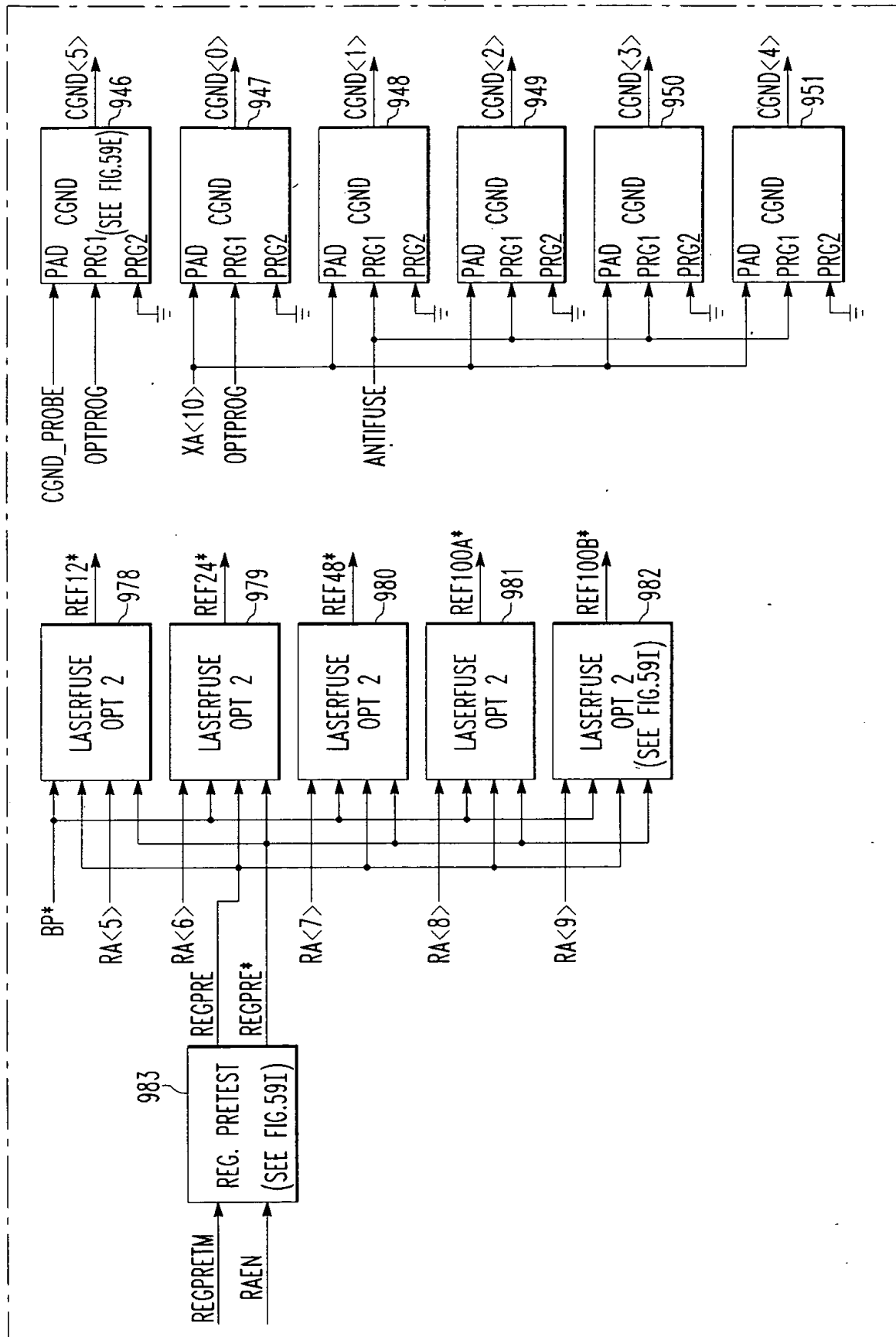
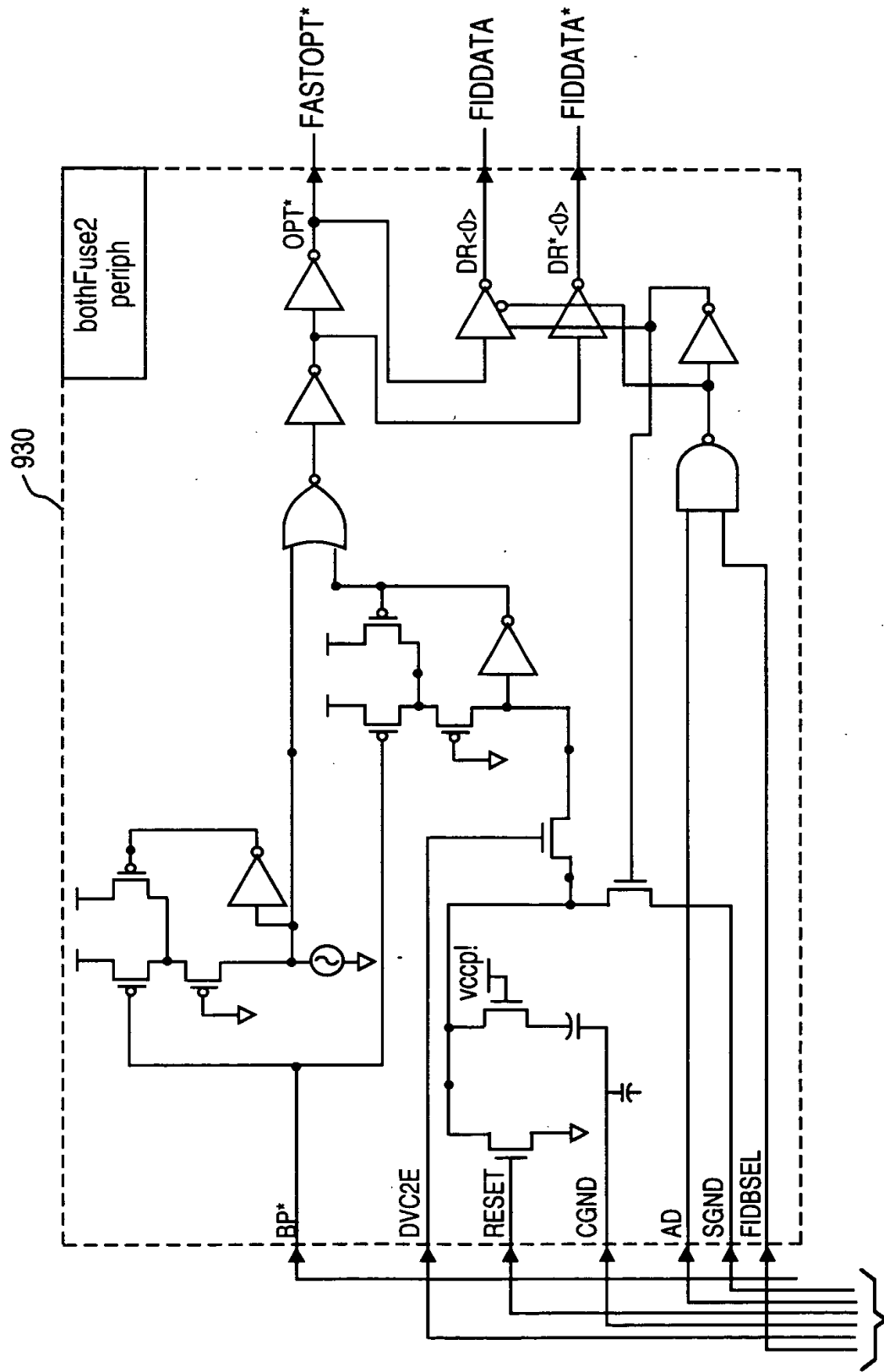


FIG. 59A



To

FIG. 59B

FIG. 59A

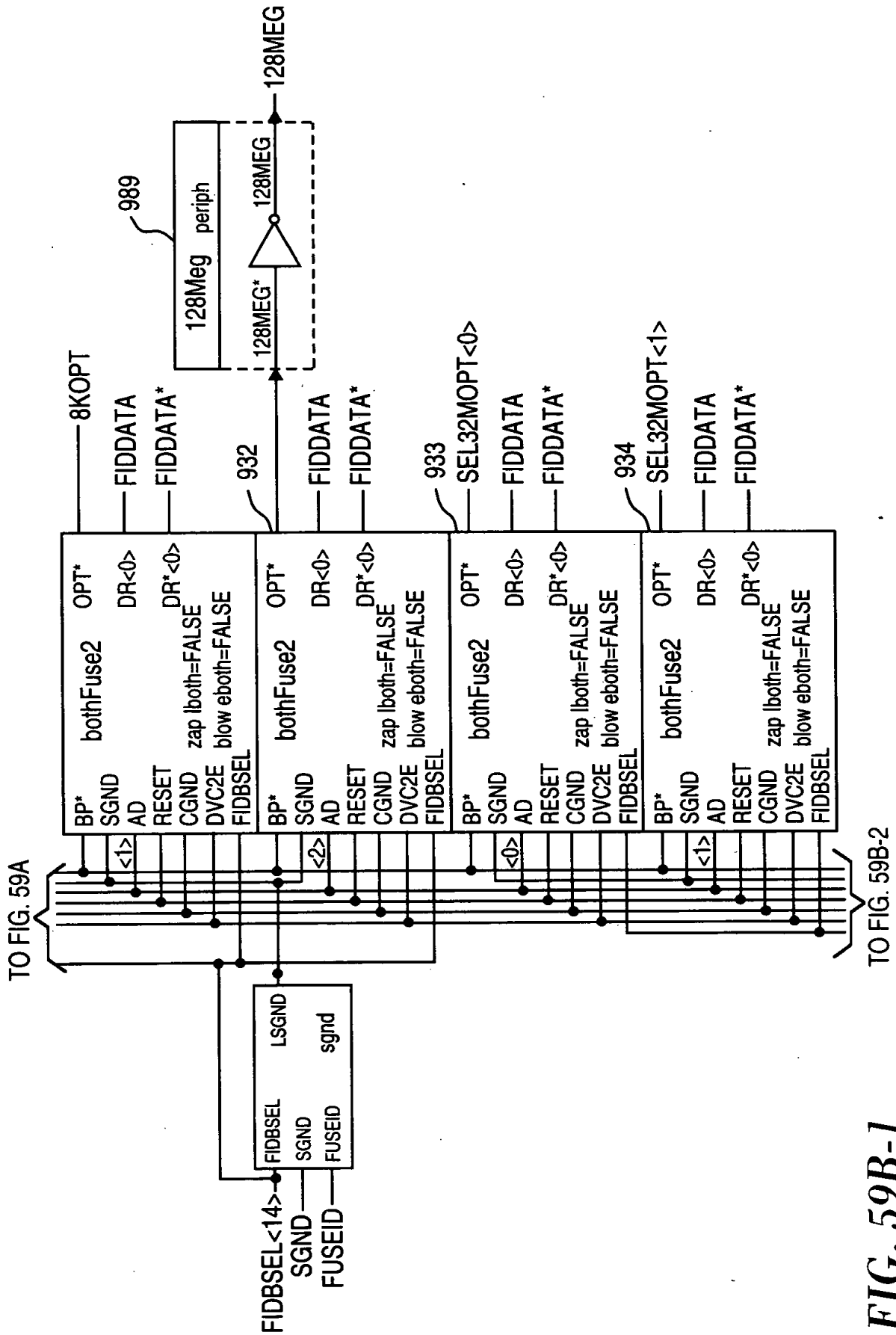


FIG. 59B-1

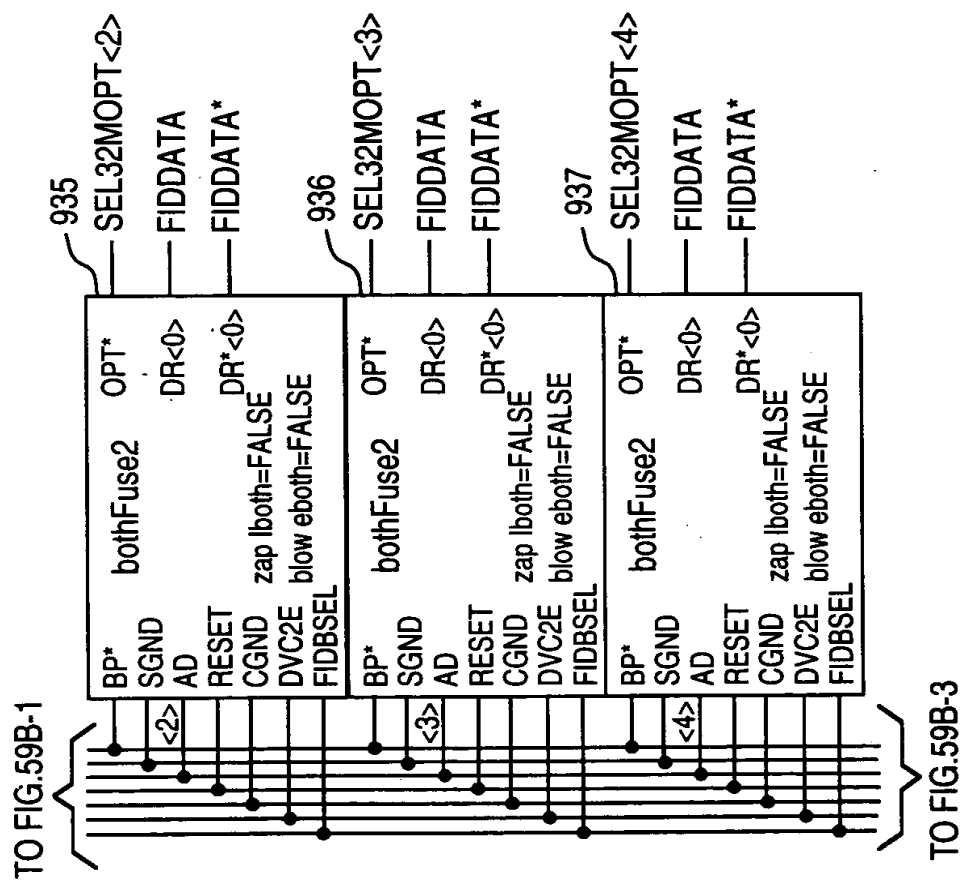


FIG. 59B-2

FIG. 59B-3

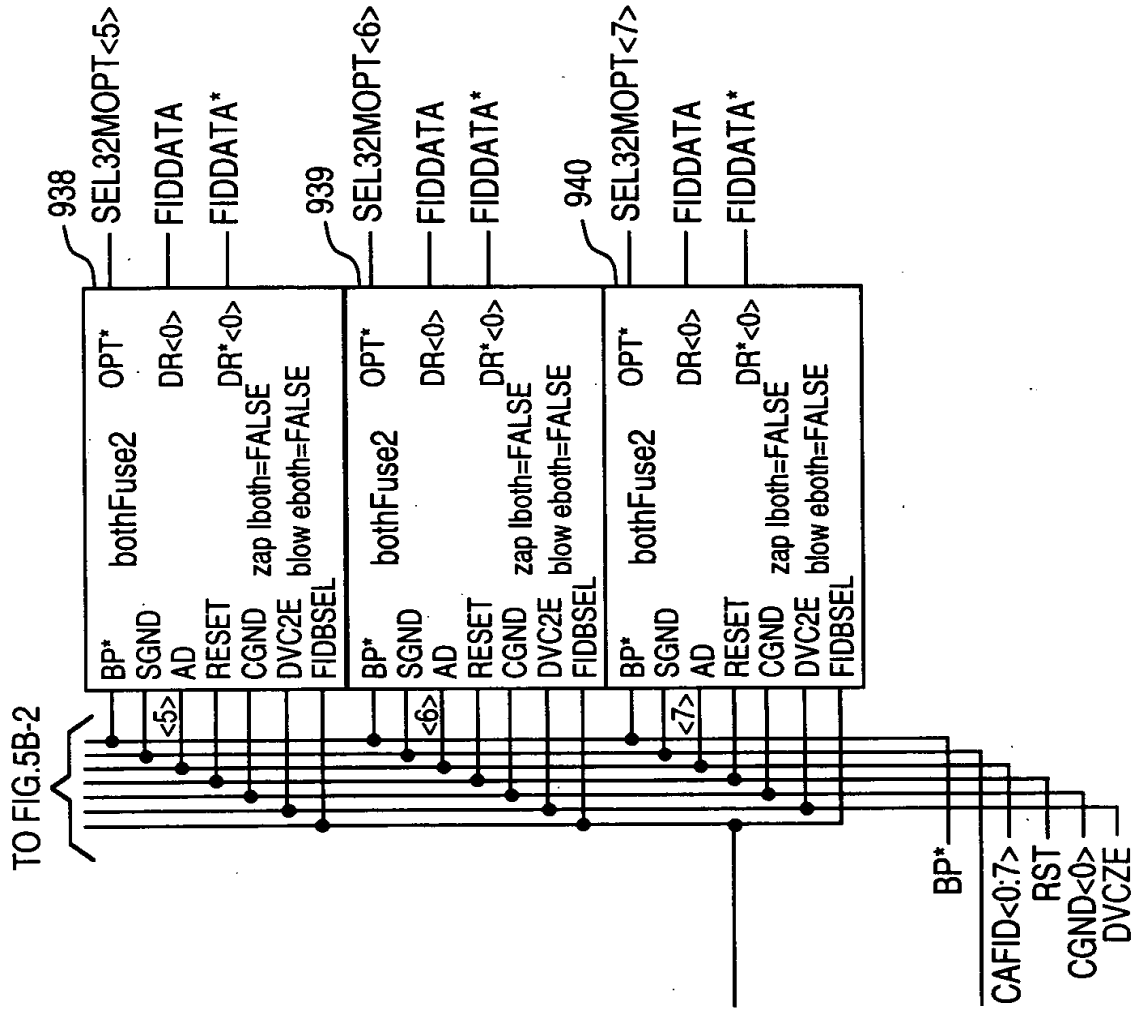
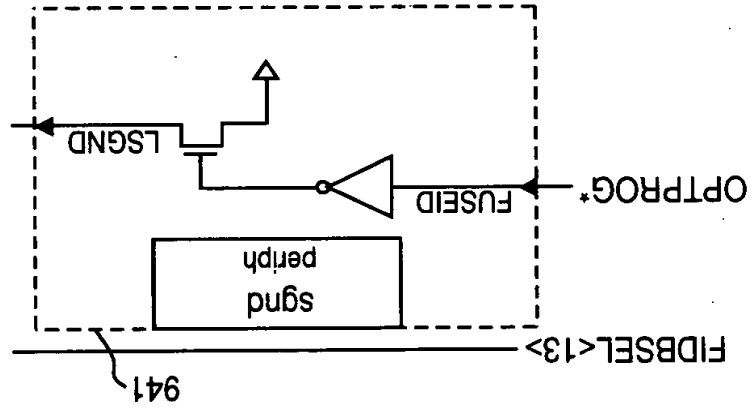


FIG. 59B-3

FIG. 59C



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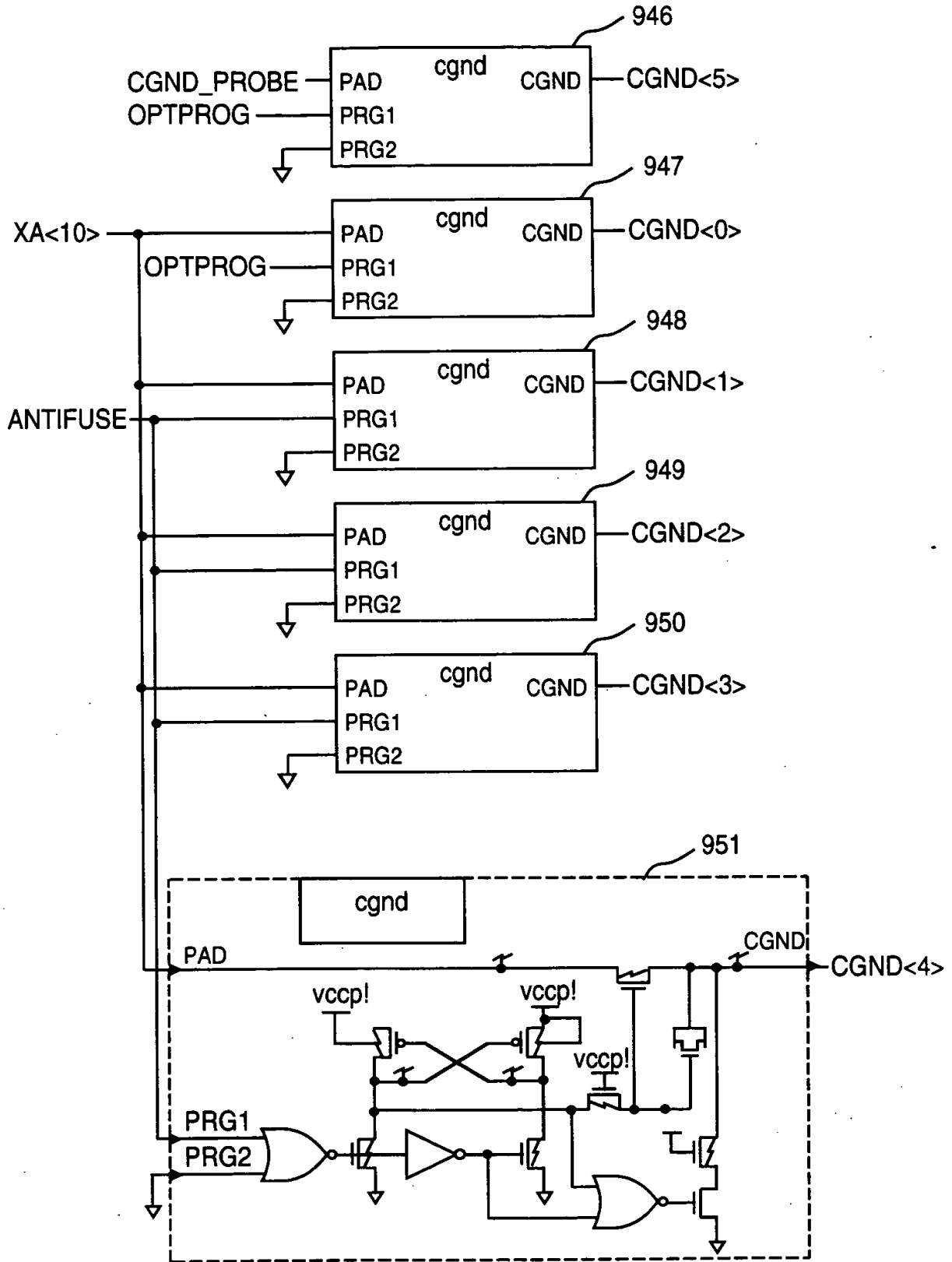


FIG. 59E

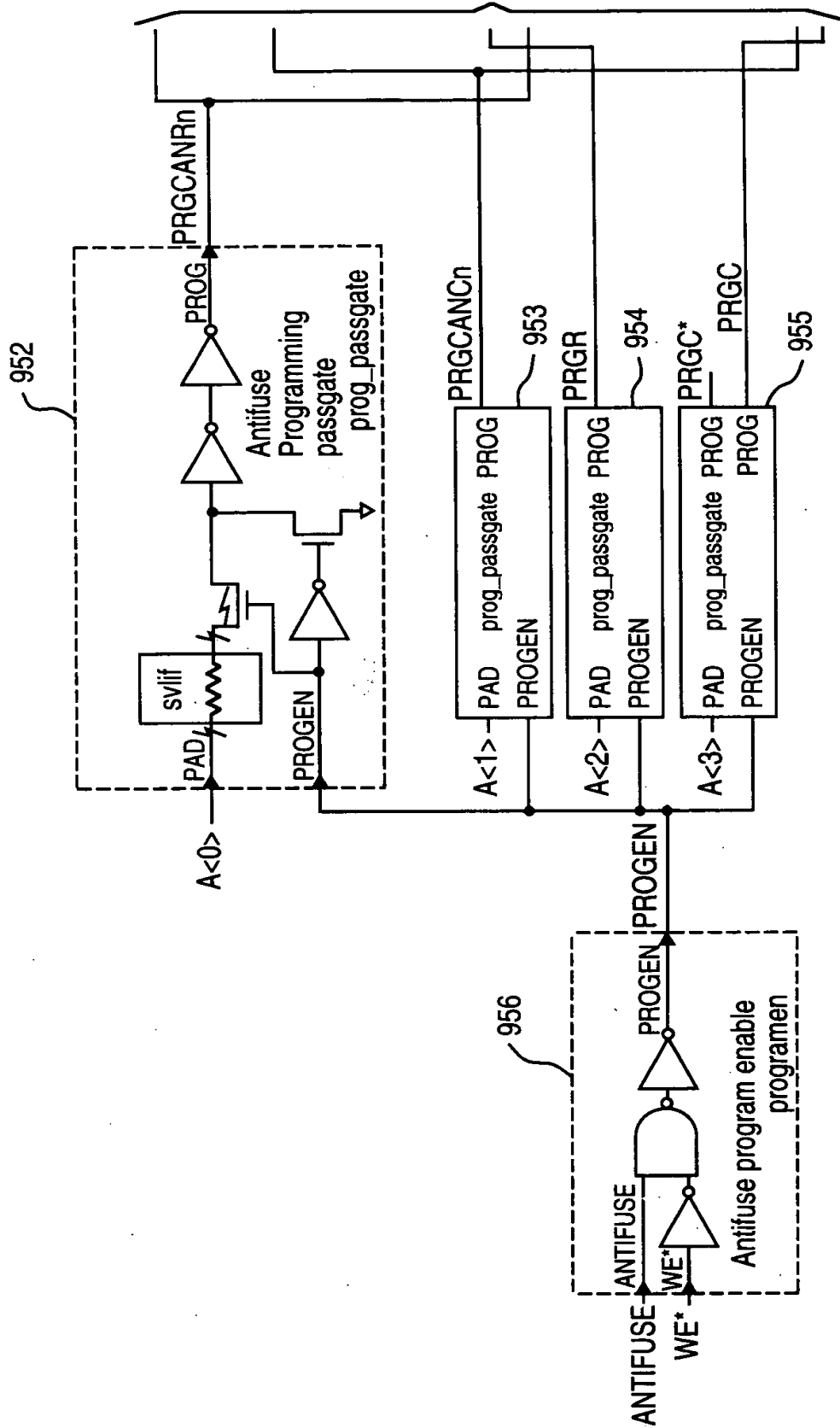


FIG. 59F-1

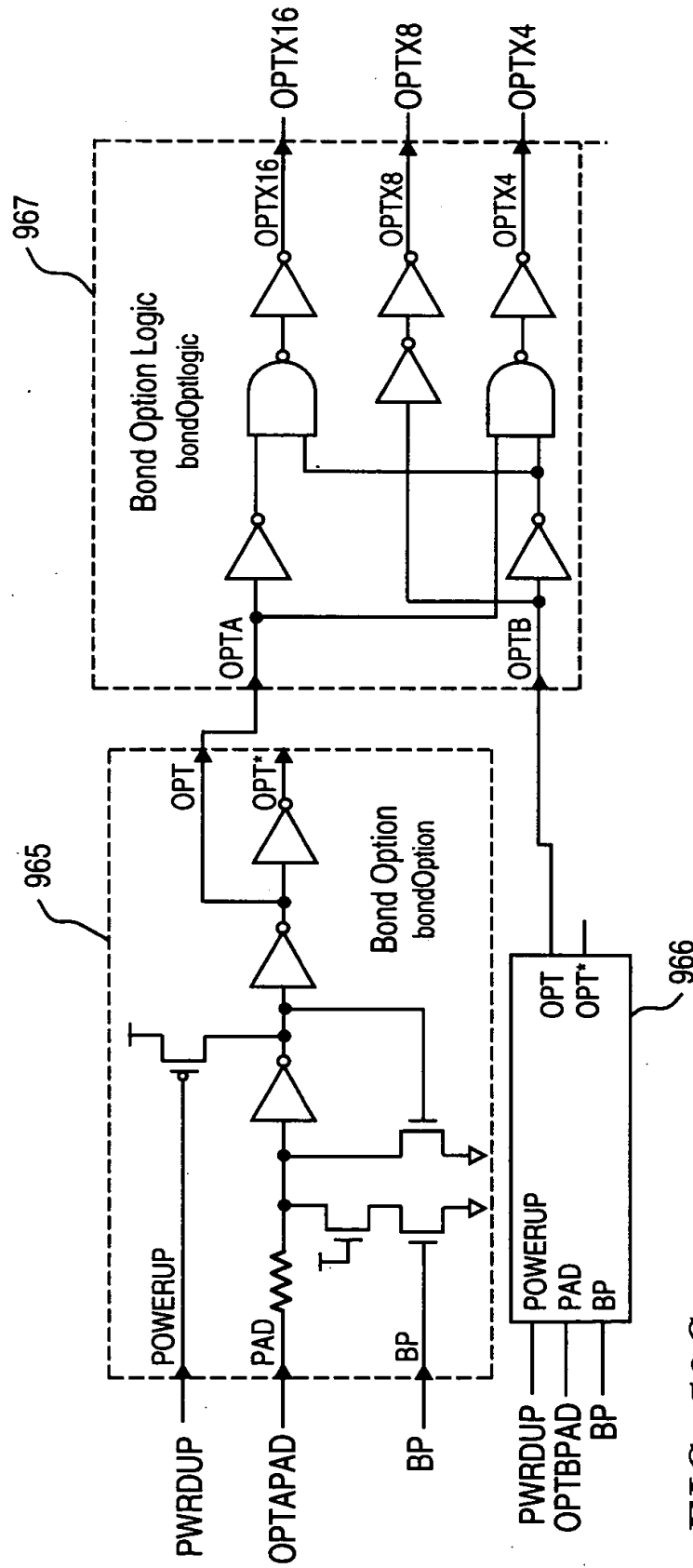
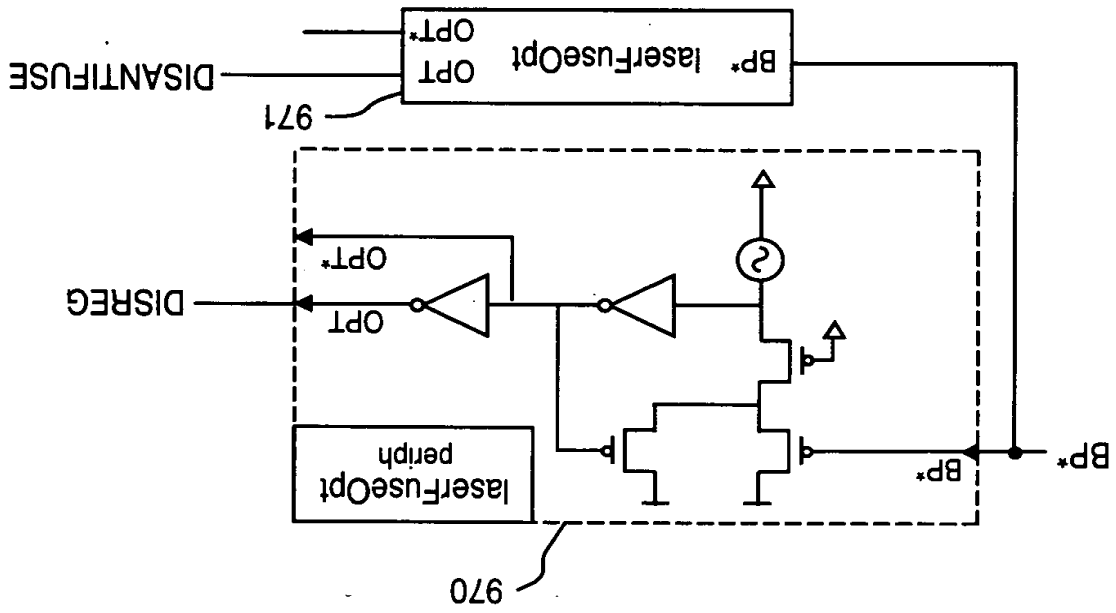


FIG. 59C

FIG. 59H



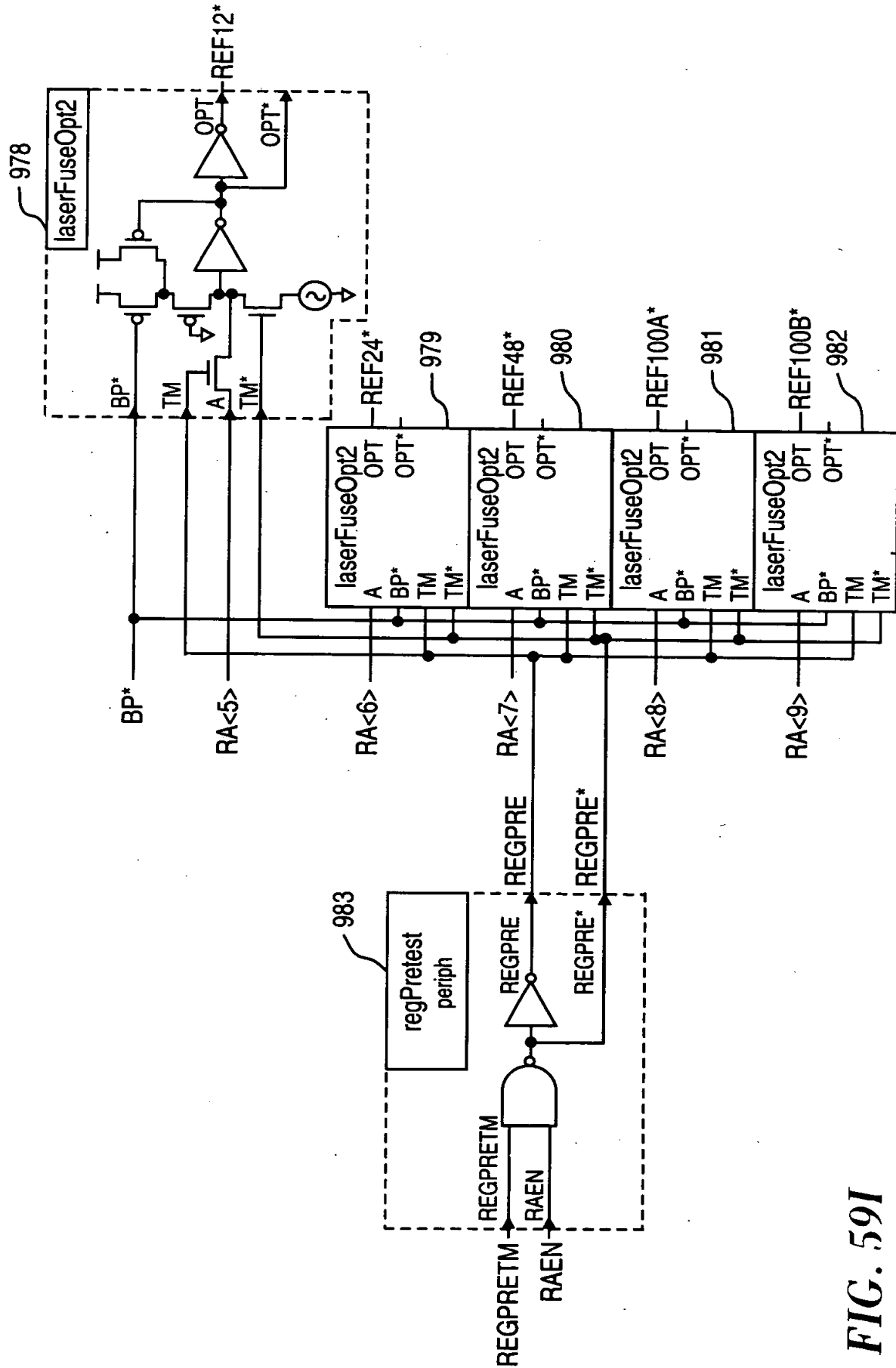
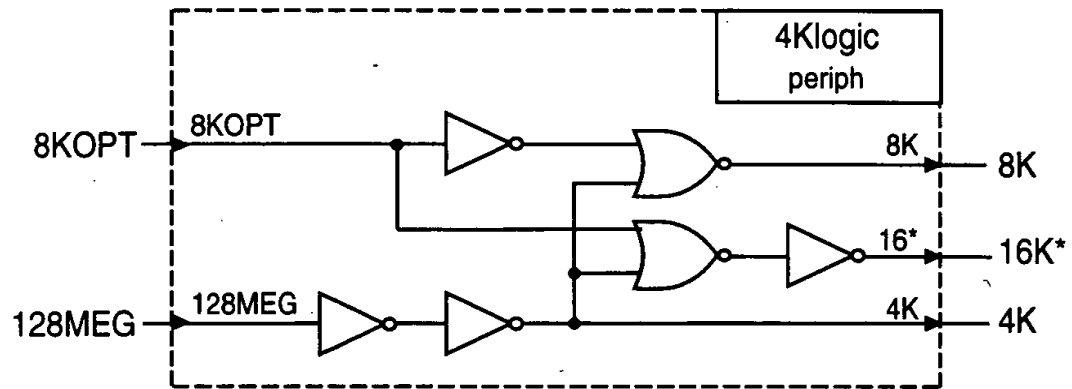
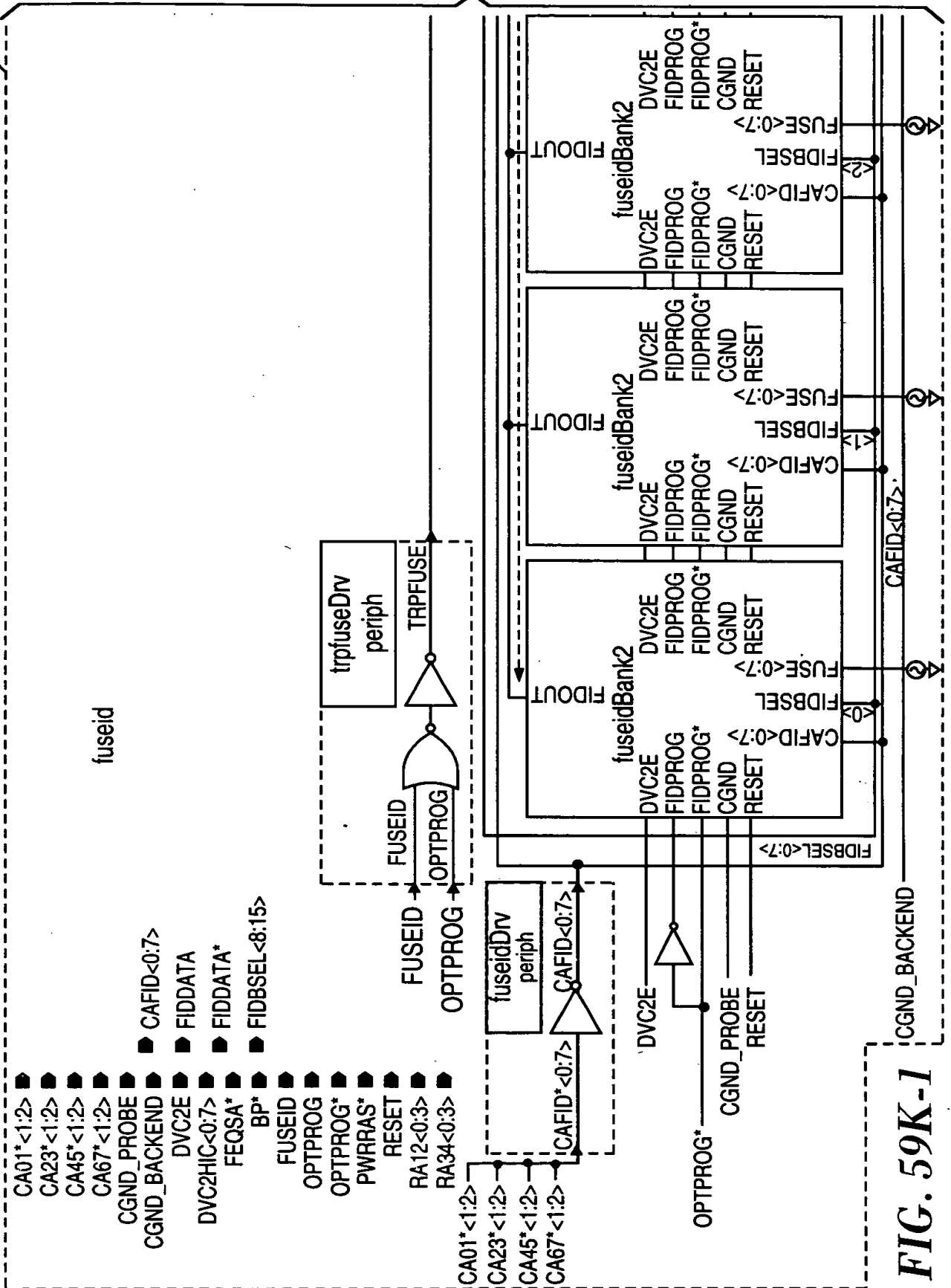


FIG. 59I

**FIG. 59J**



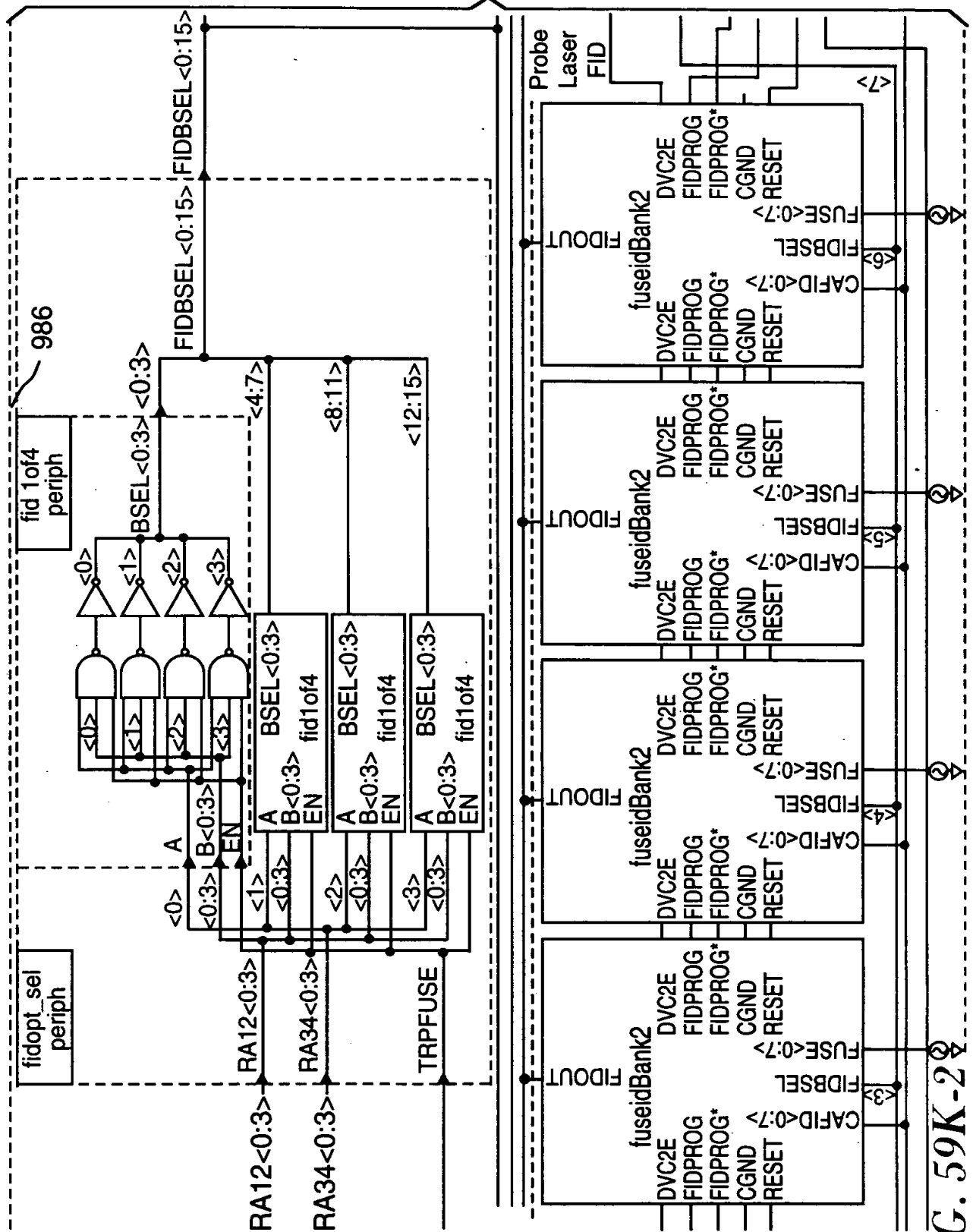
TO
FIG.
59L-1

FIG. 59K-2

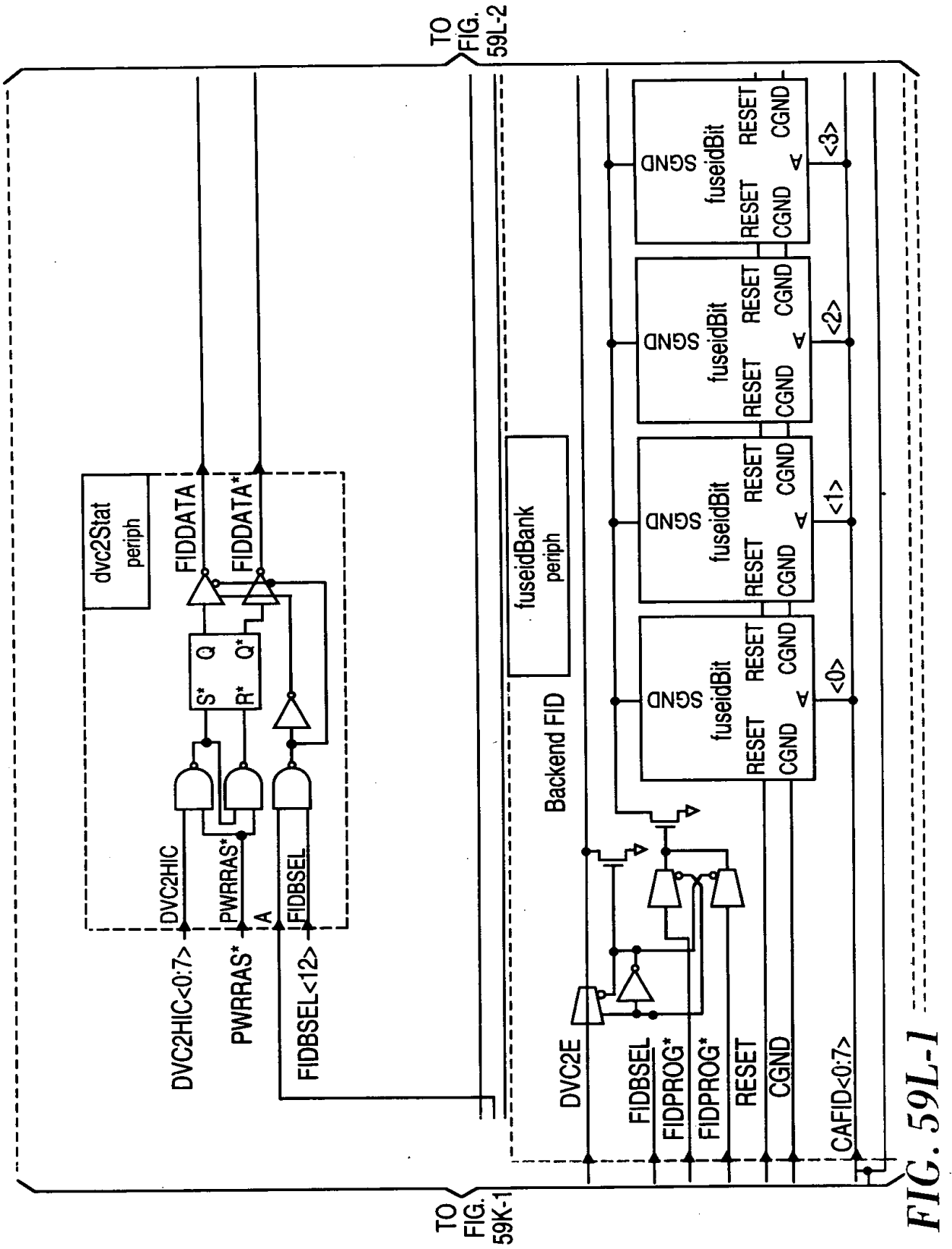


FIG. 59L-1

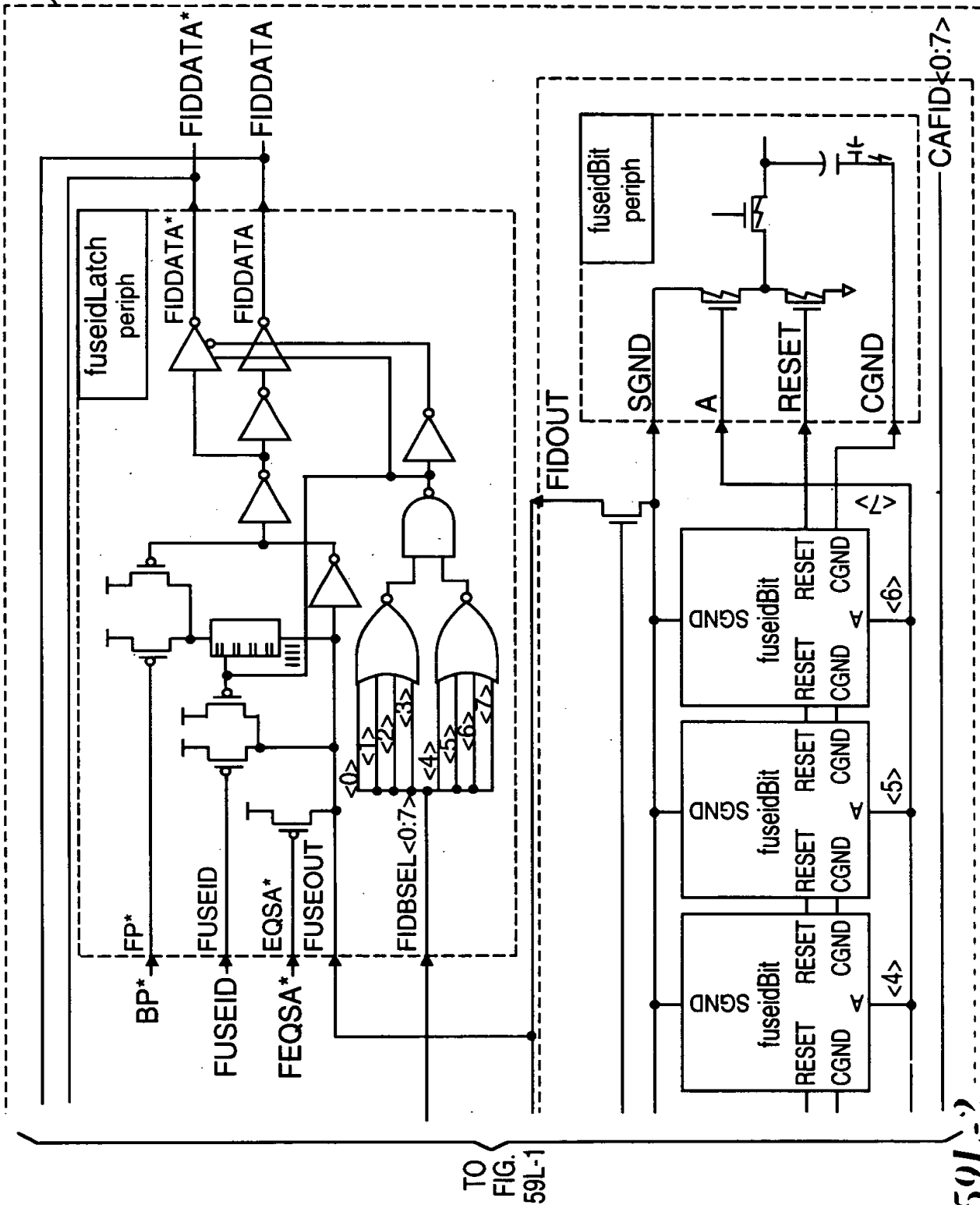


FIG. 59L-2

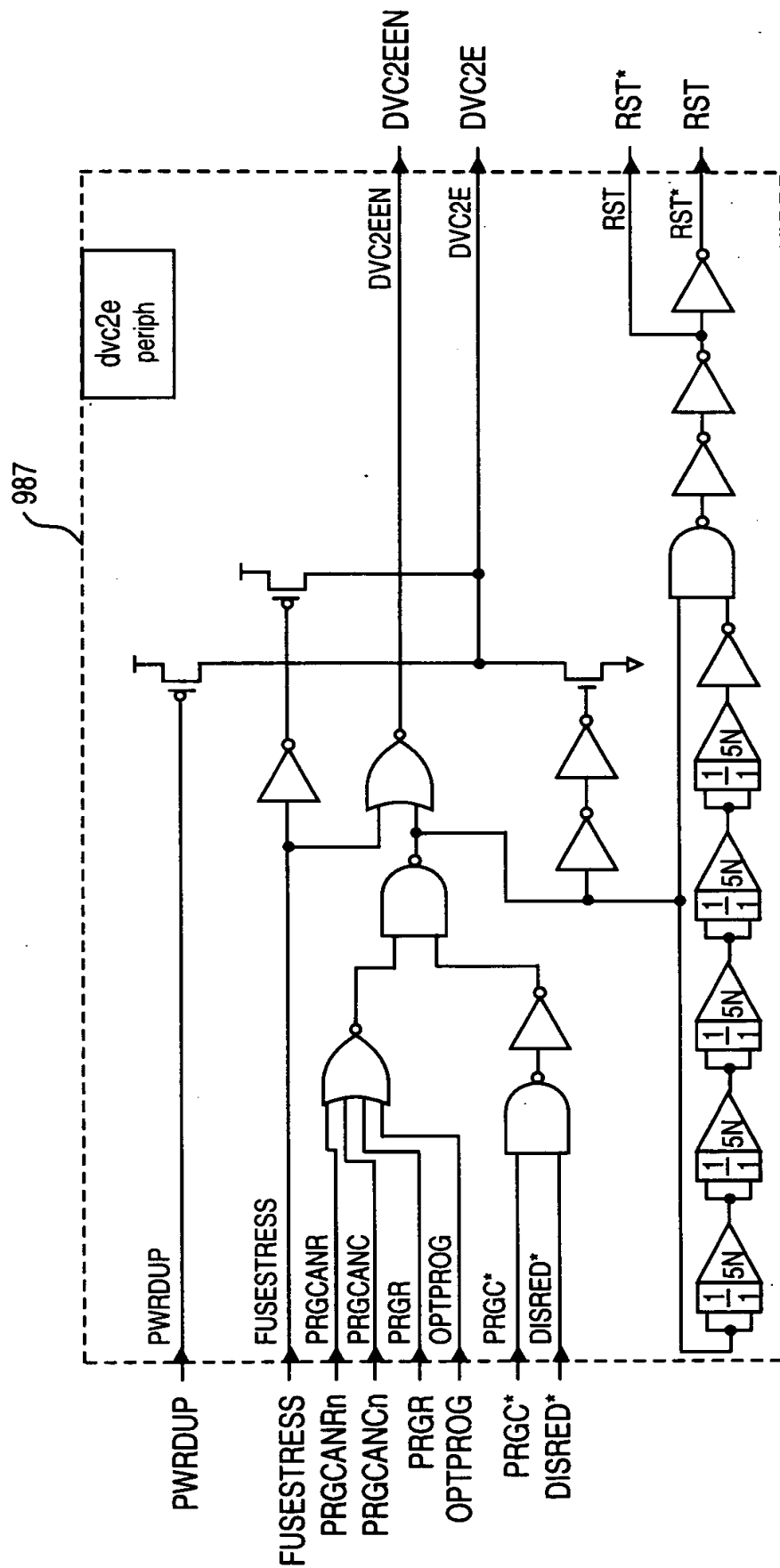


FIG. 59M

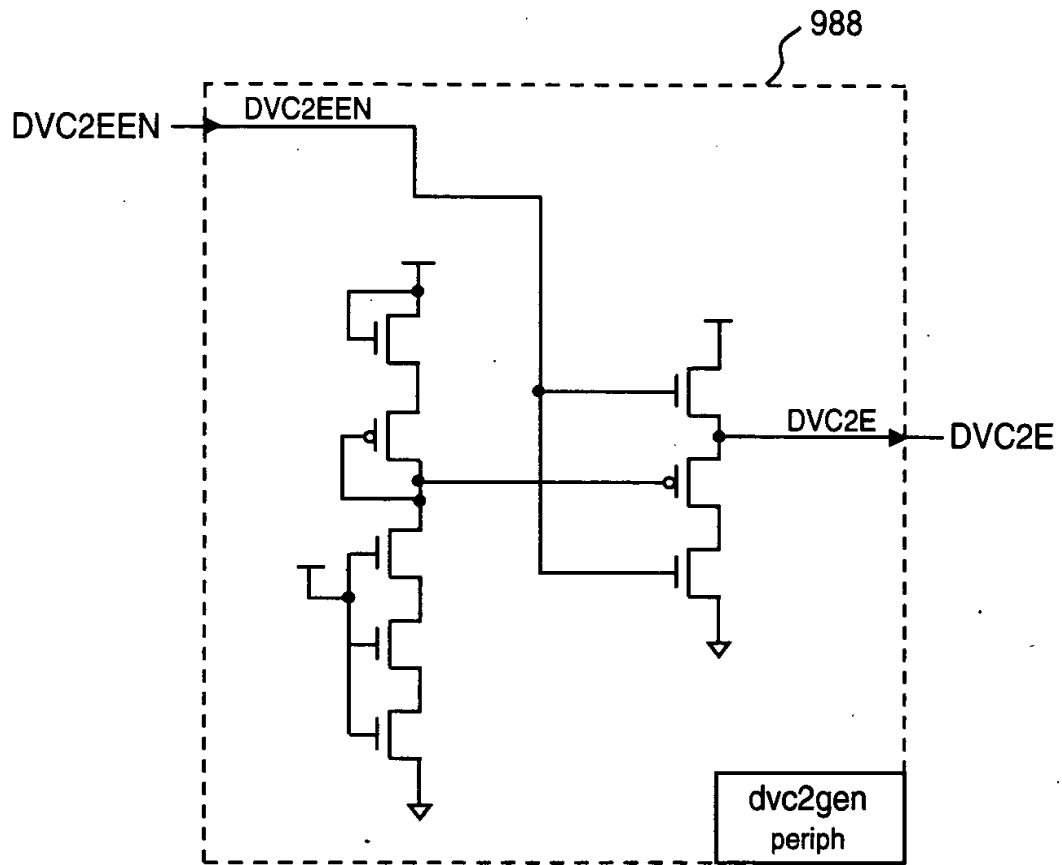
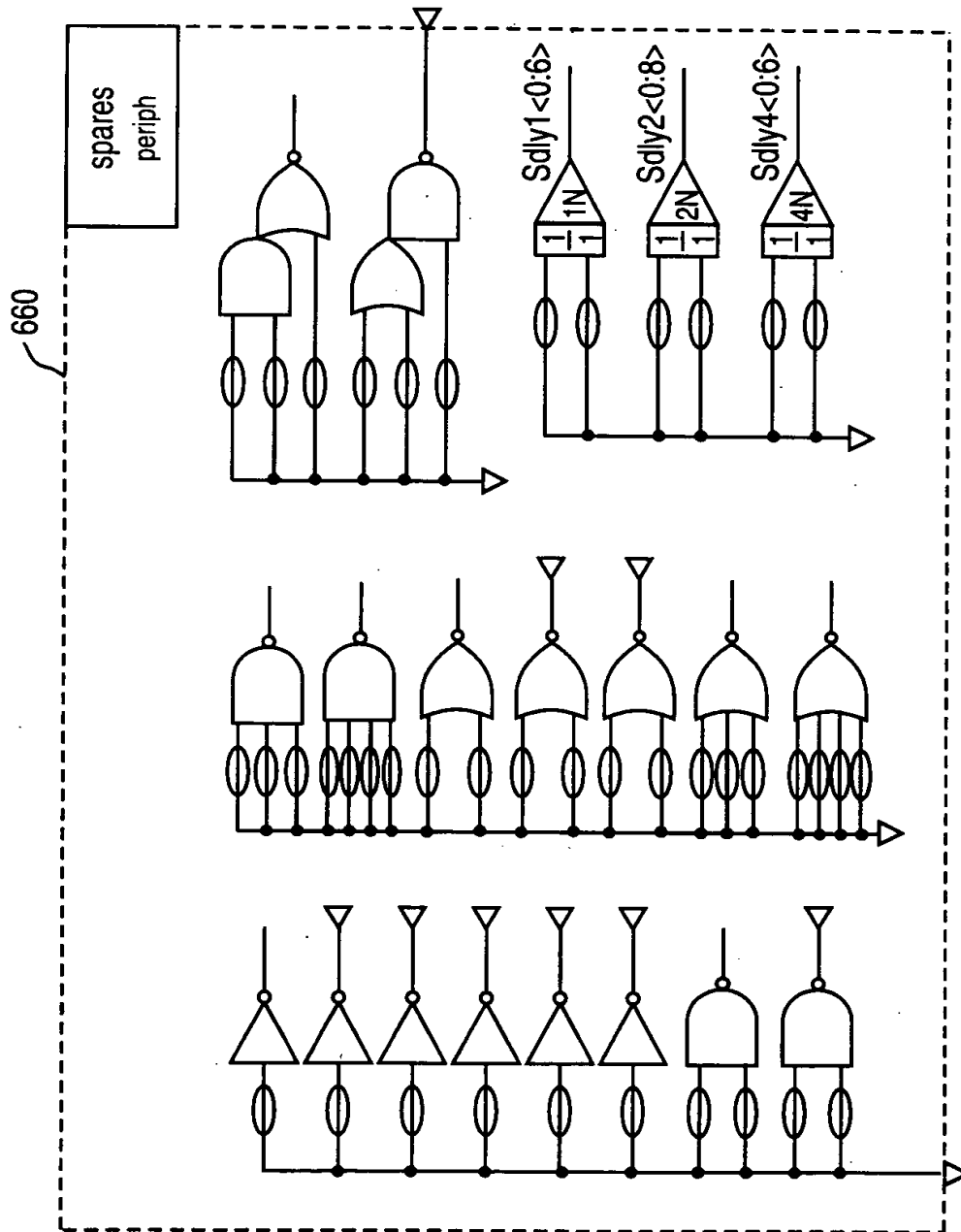


FIG. 59N



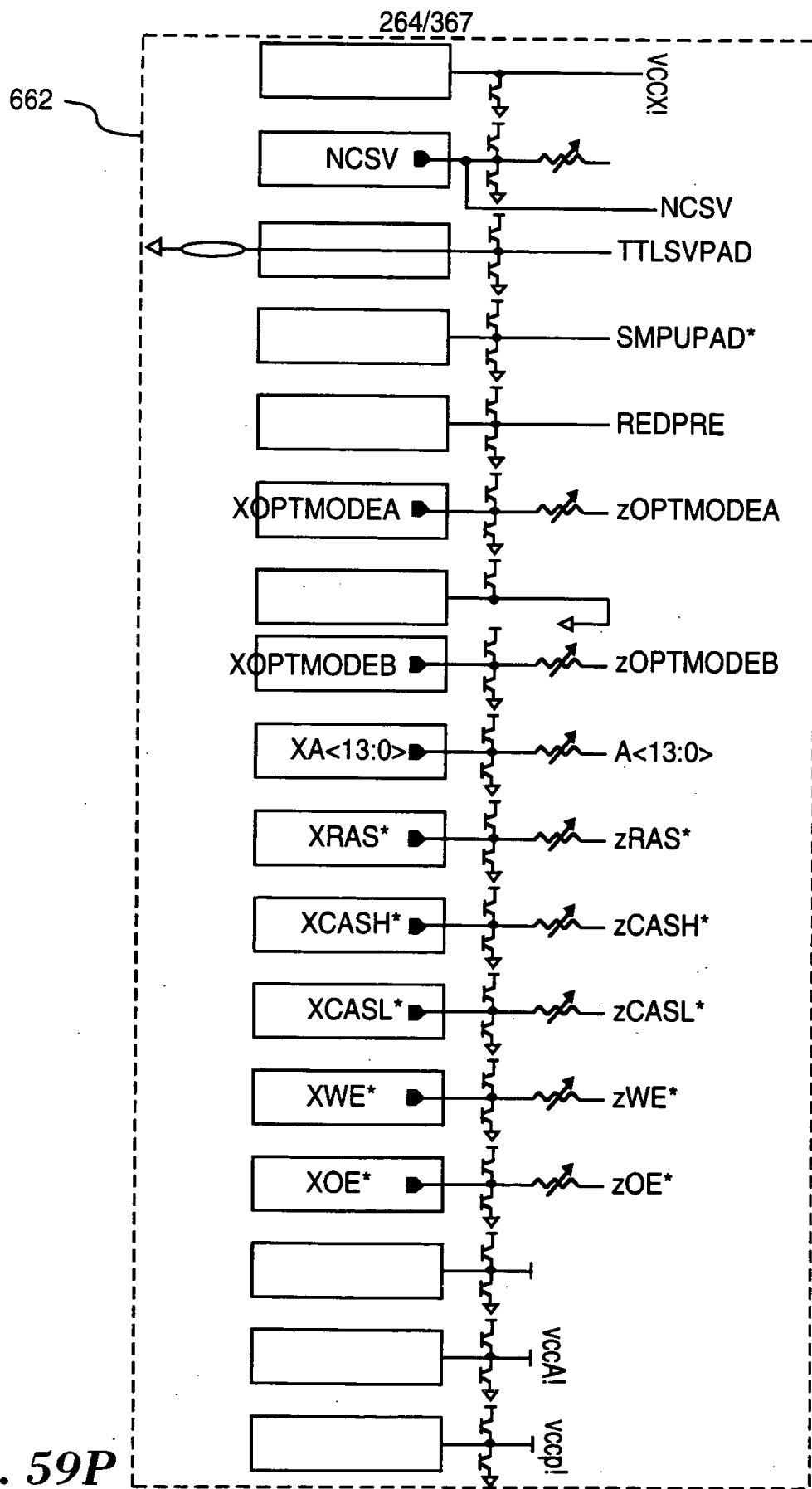


FIG. 59P

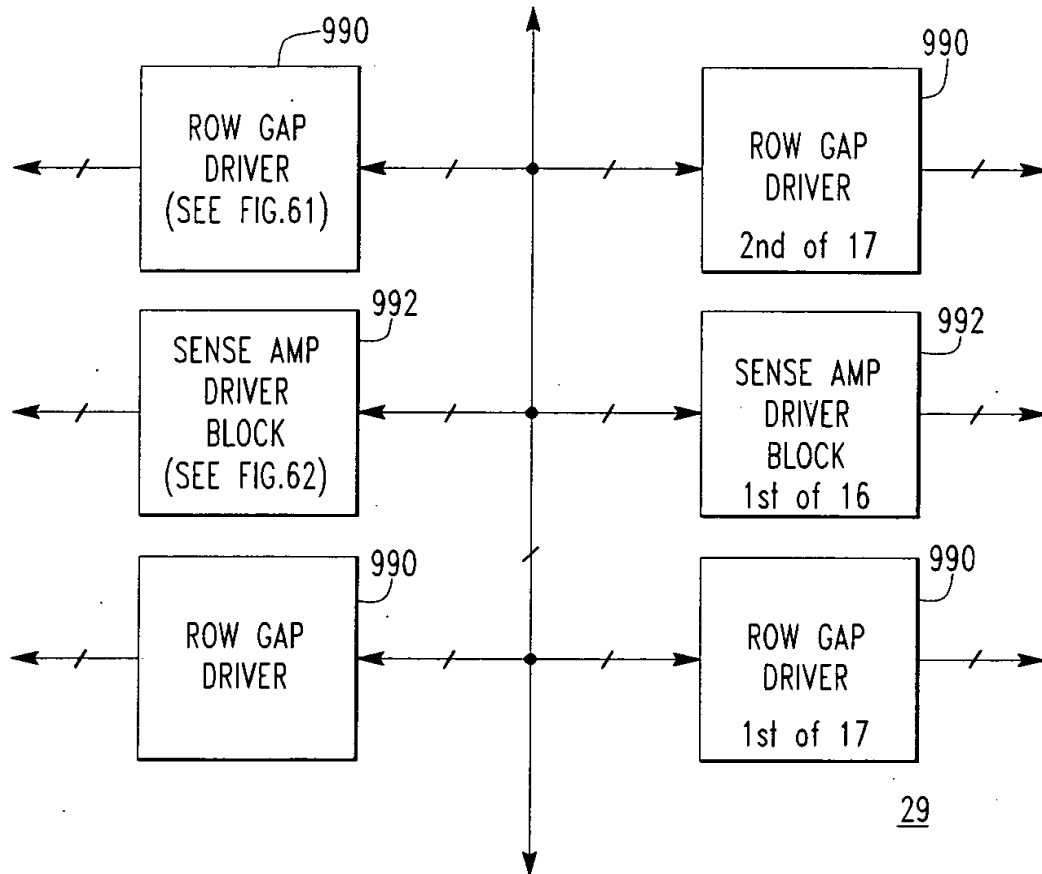


FIG. 60



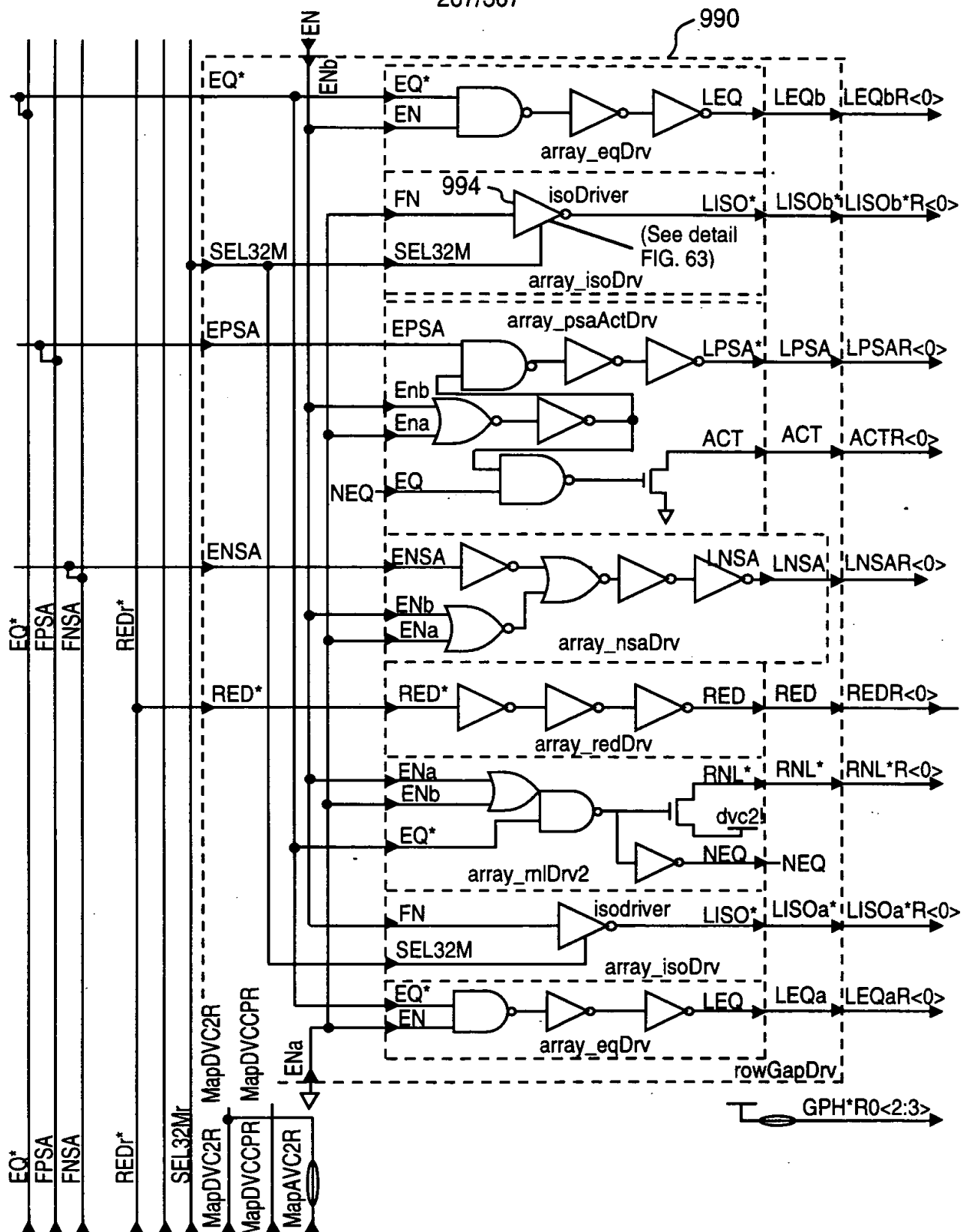


FIG. 62

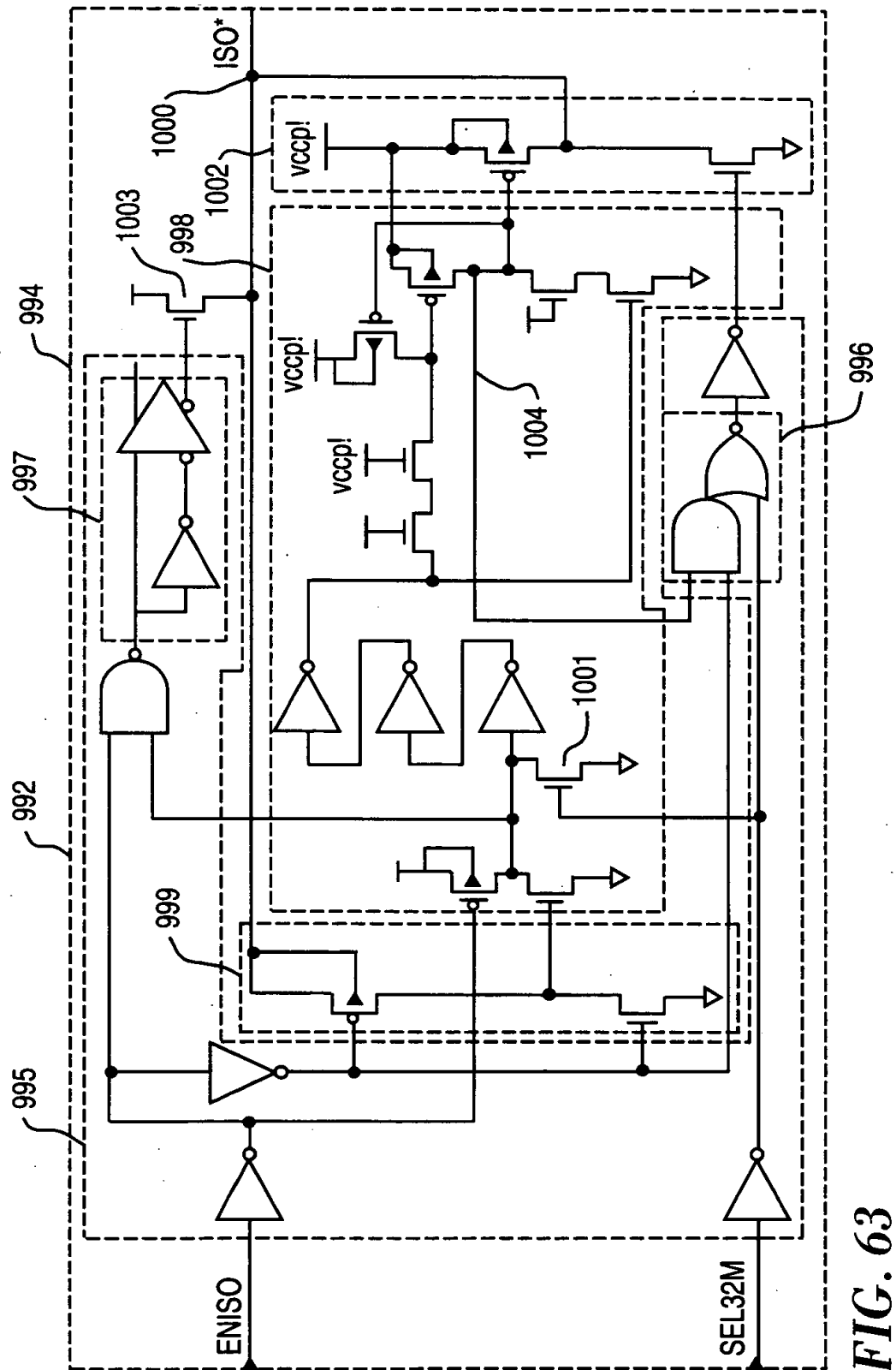


FIG. 63

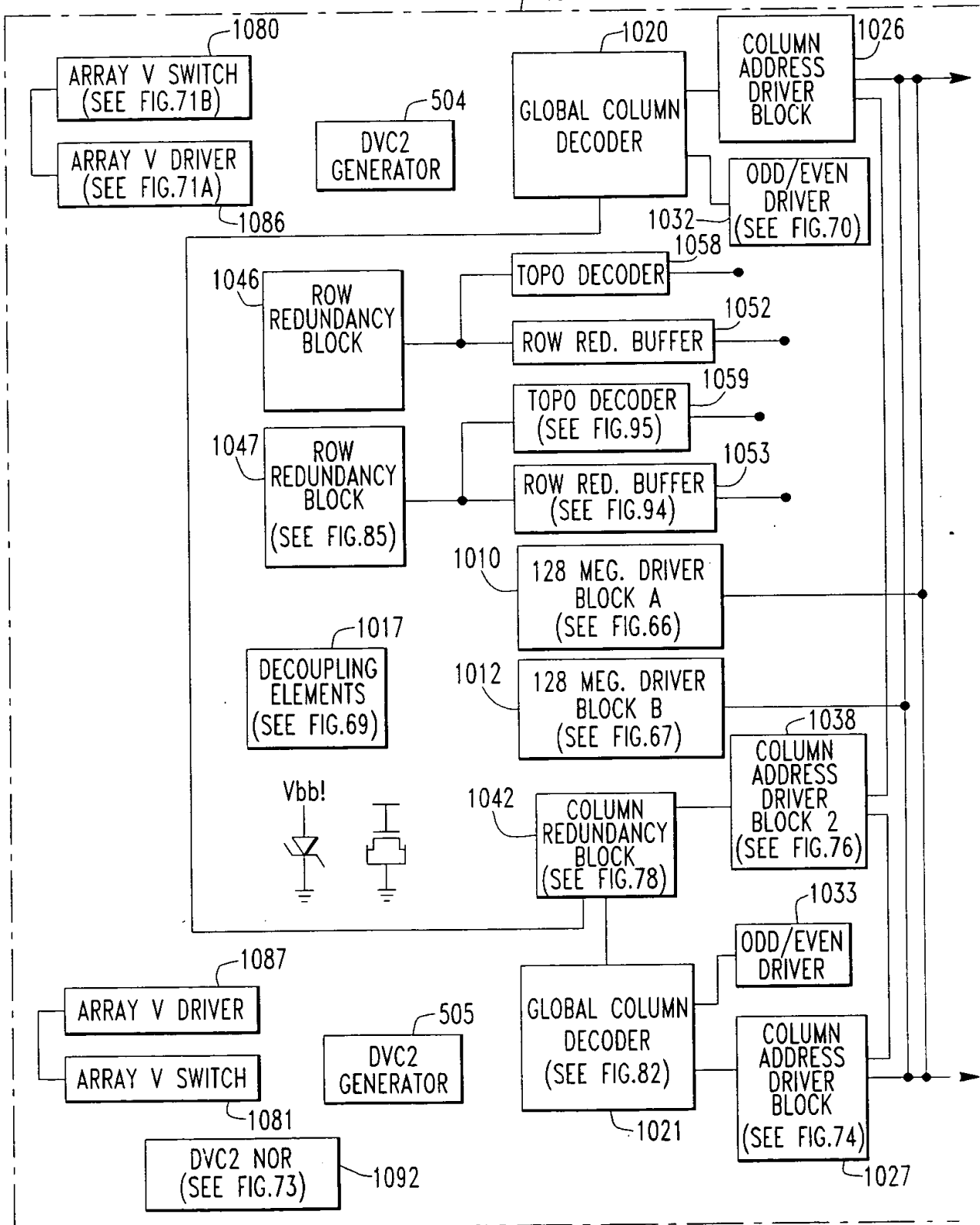


FIG. 64A

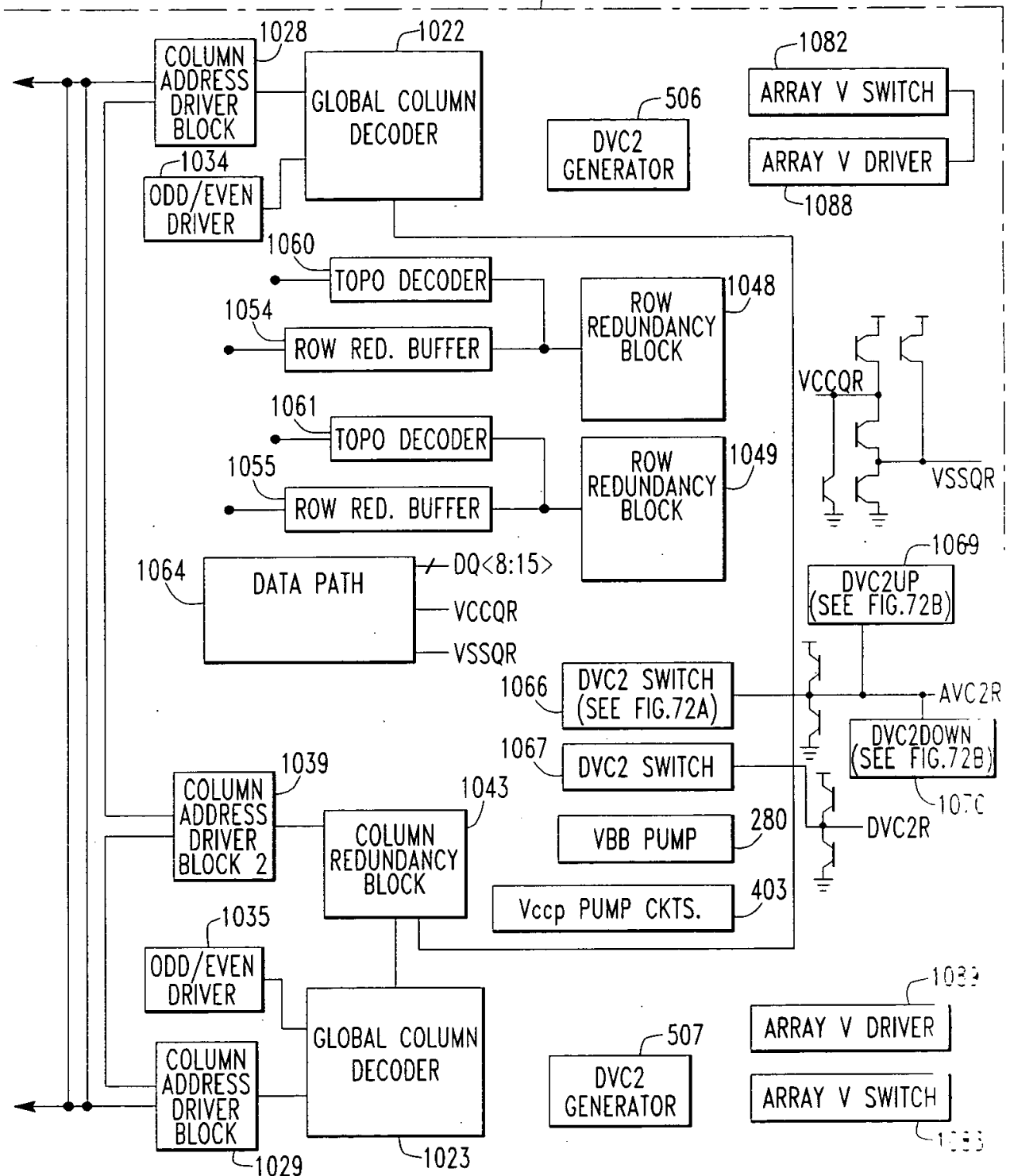


FIG. 64B

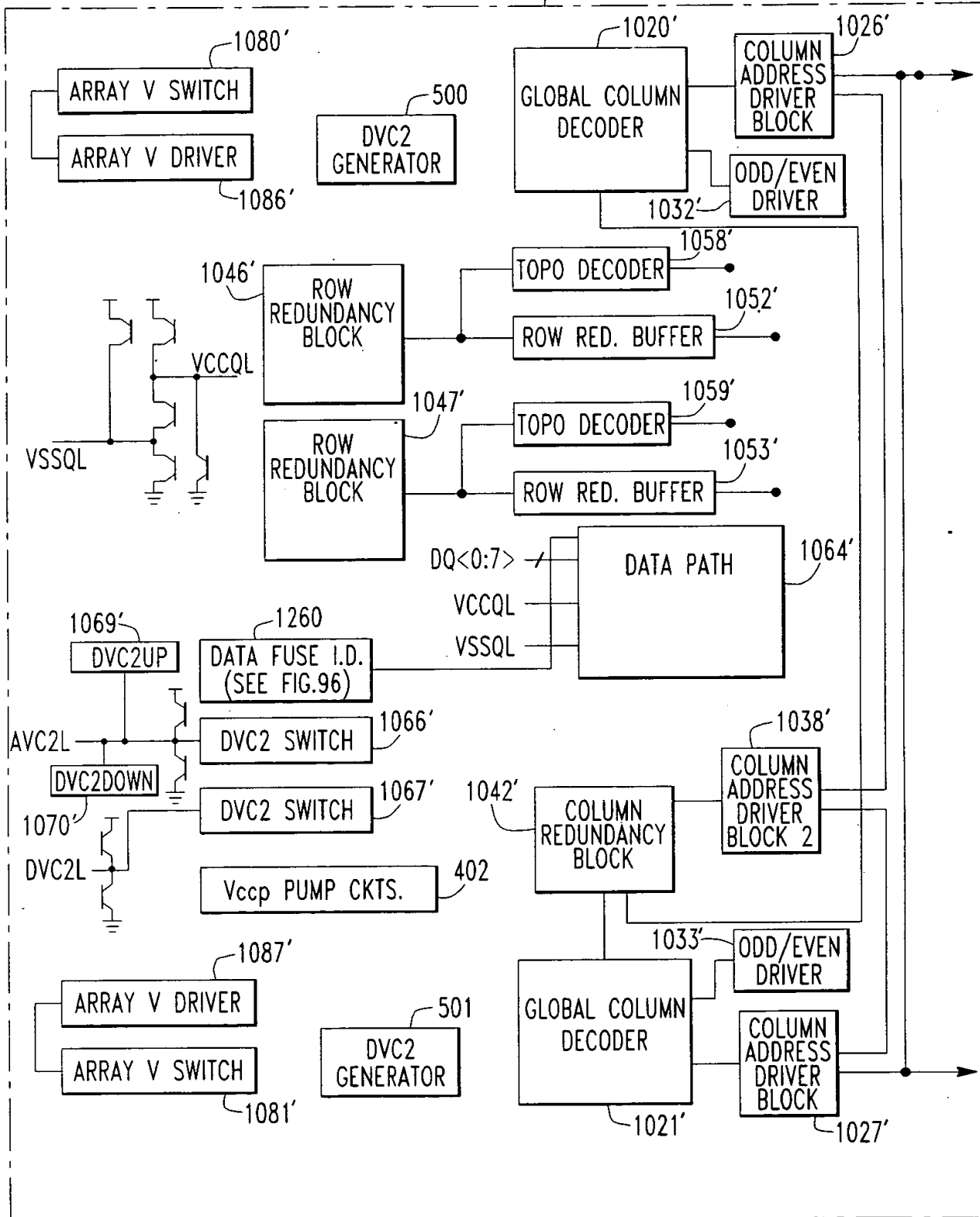


FIG. 65A

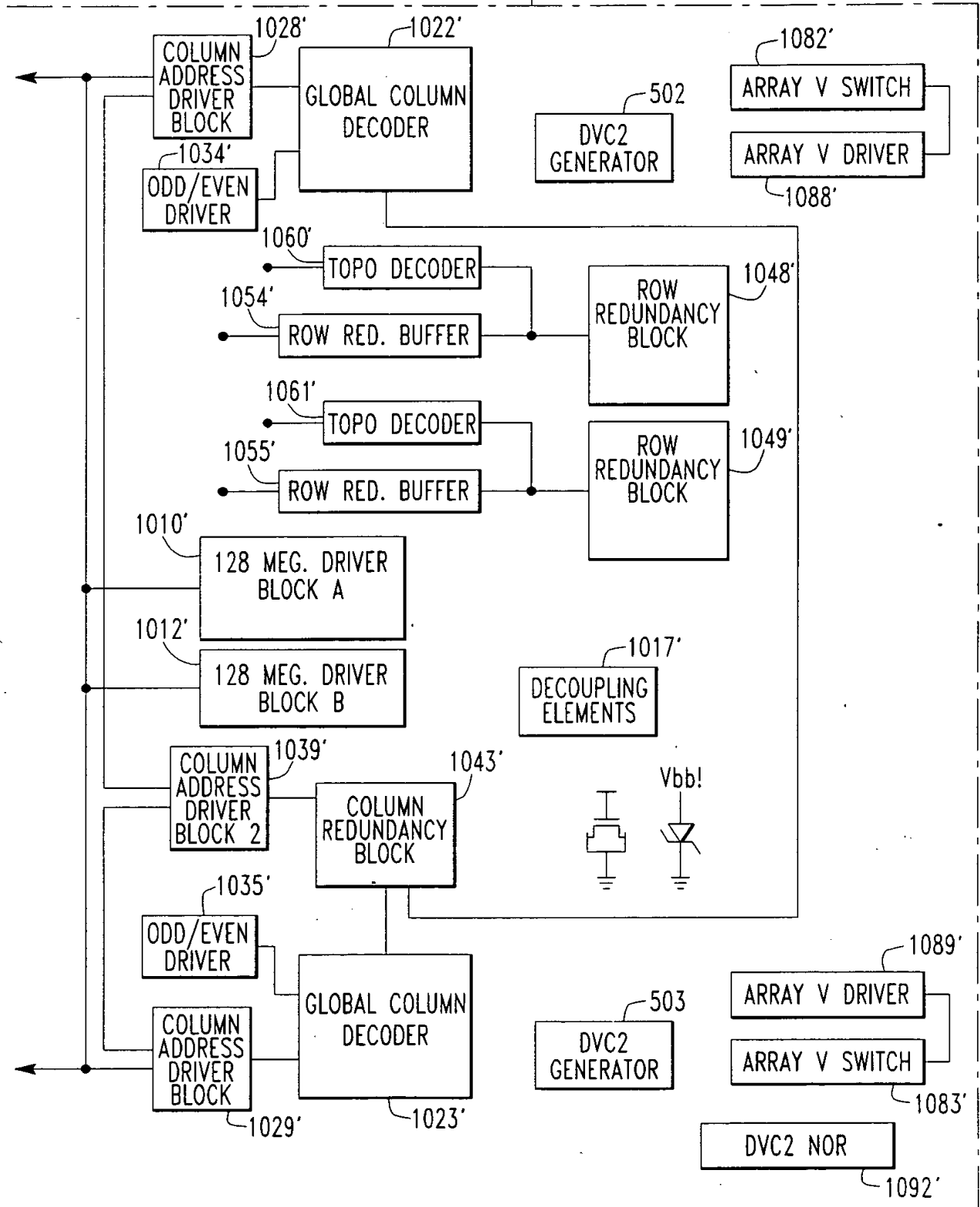
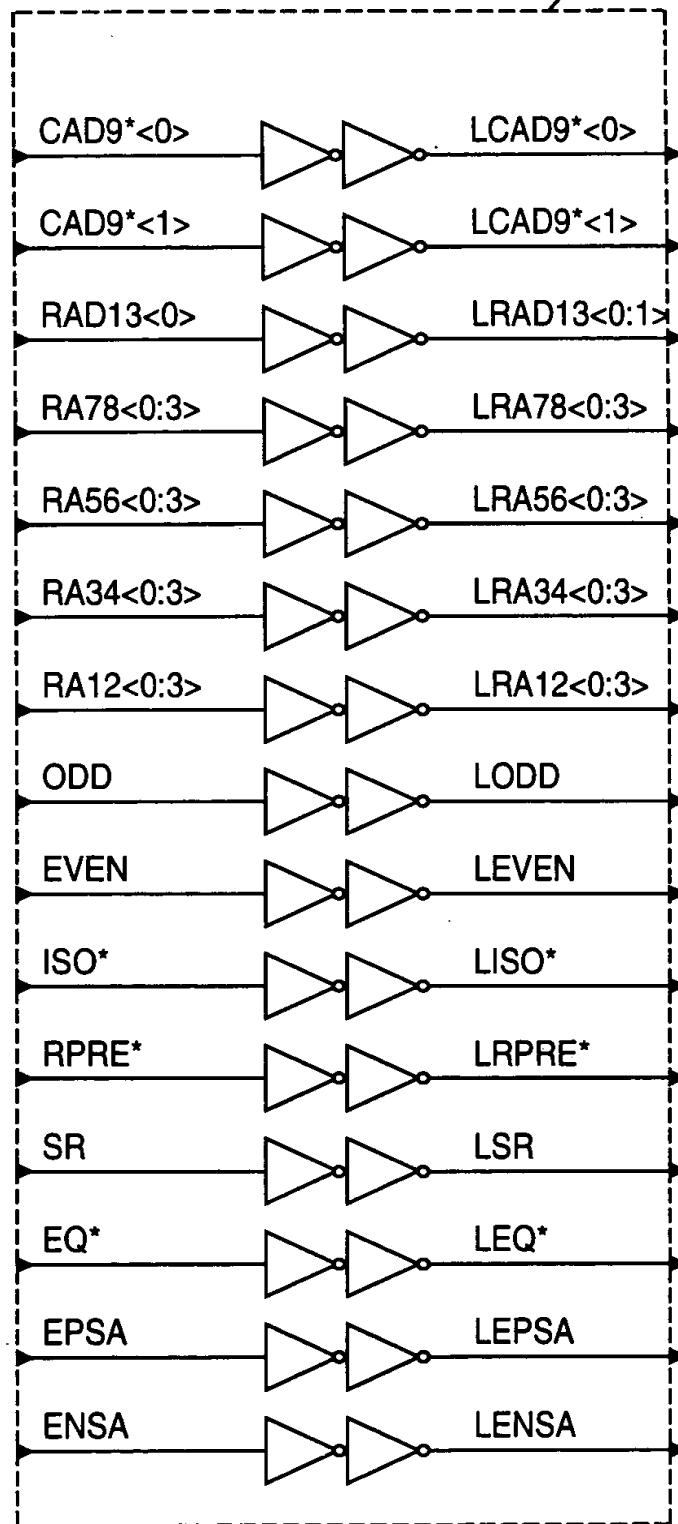


FIG. 65B

**FIG. 66**

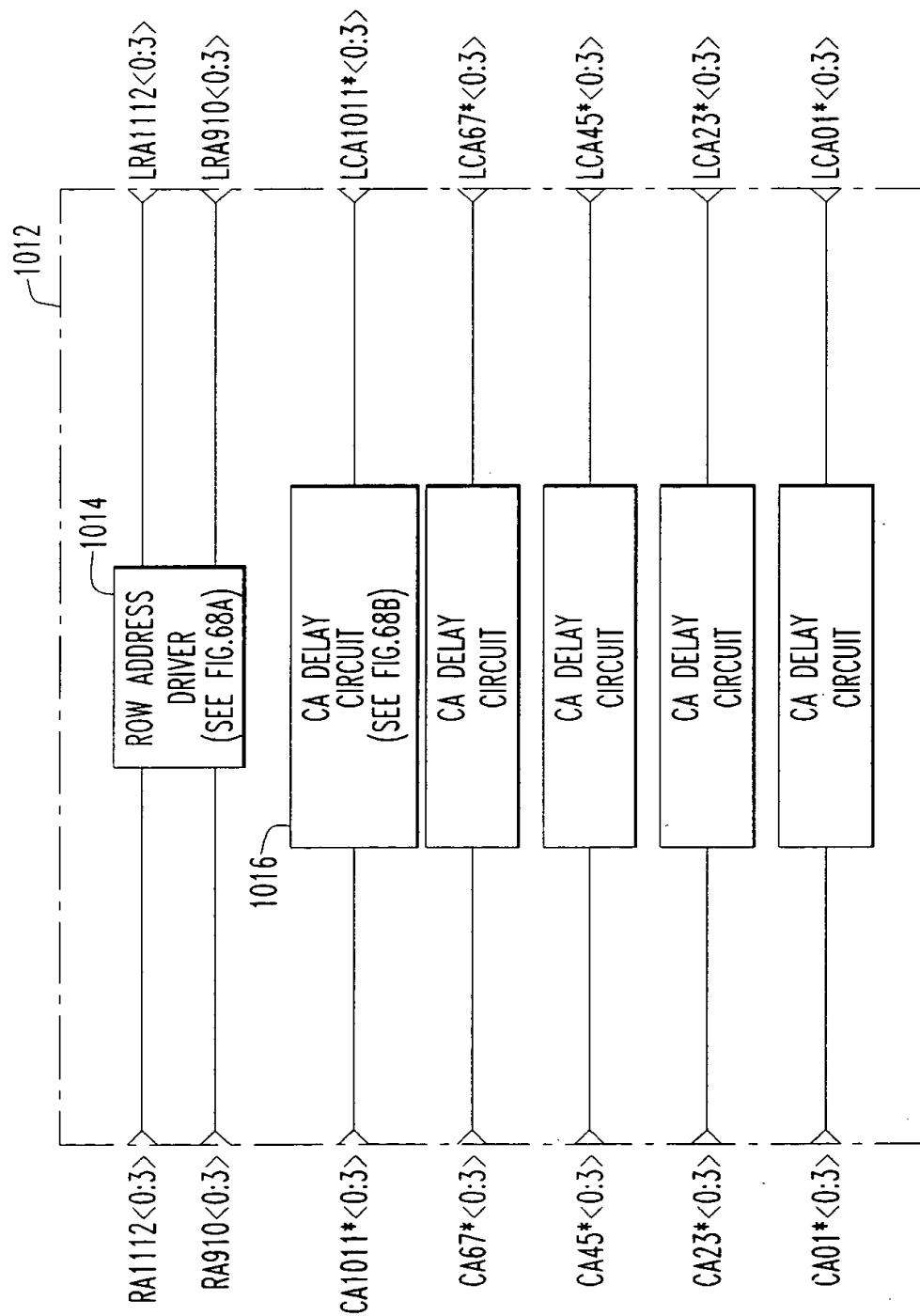
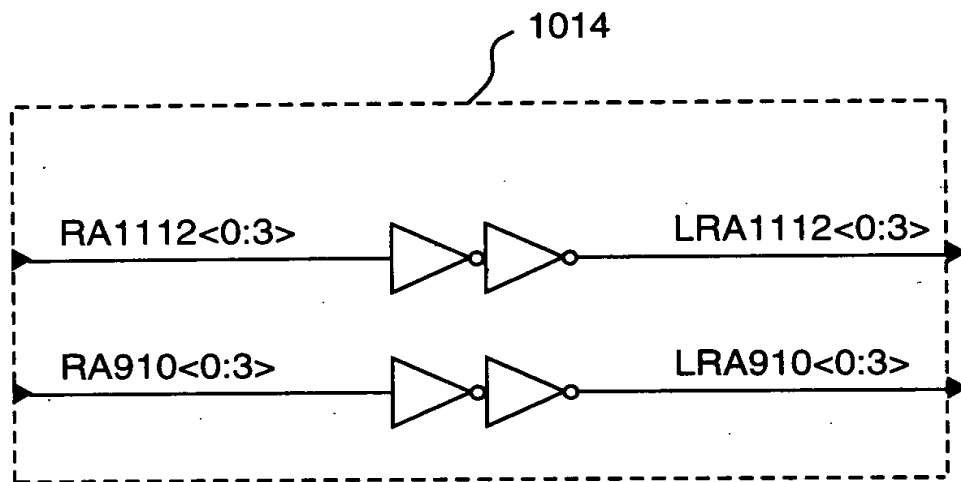
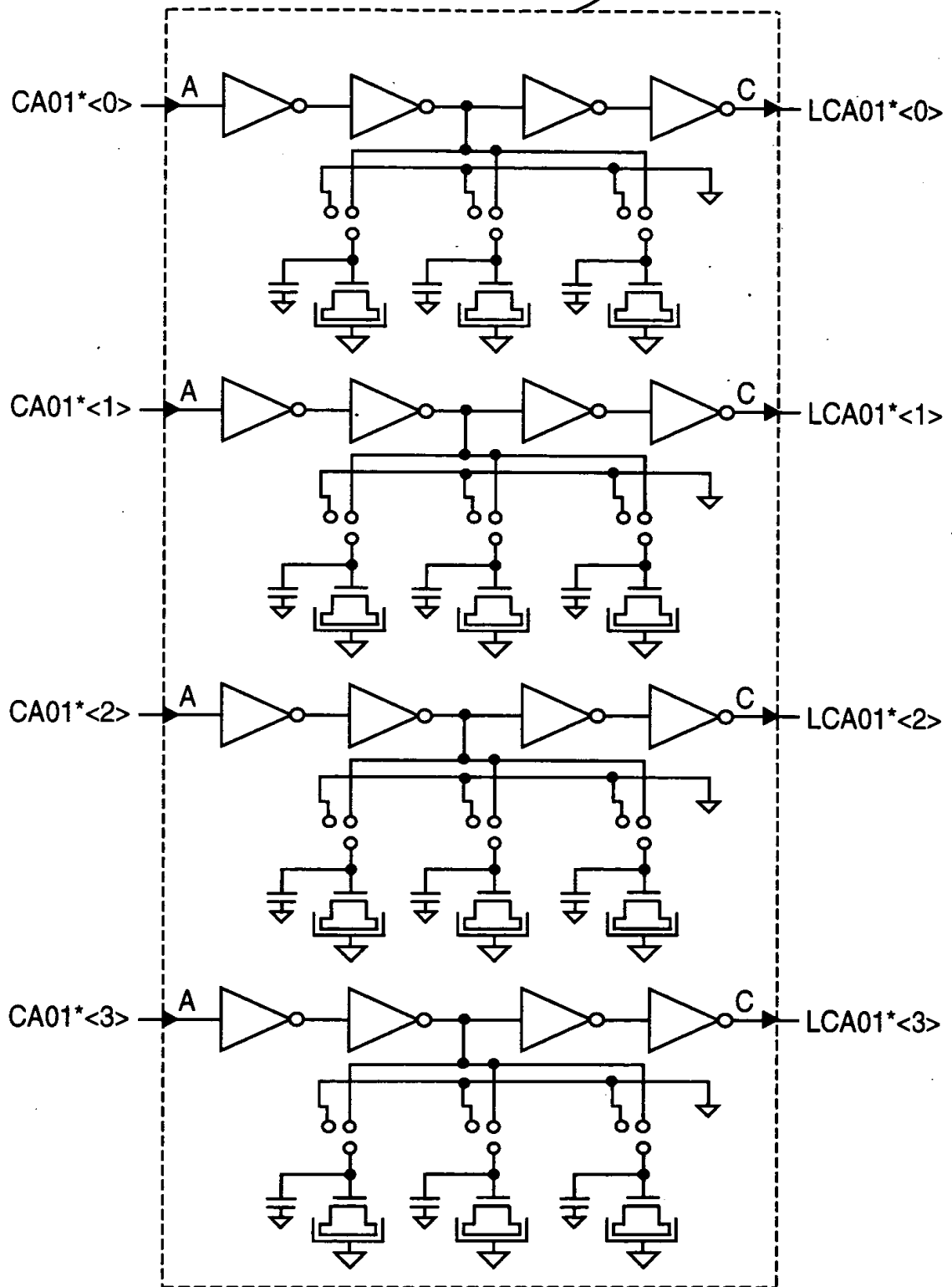
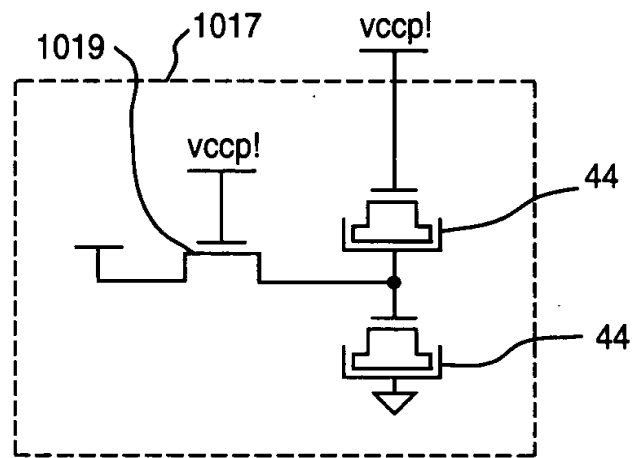
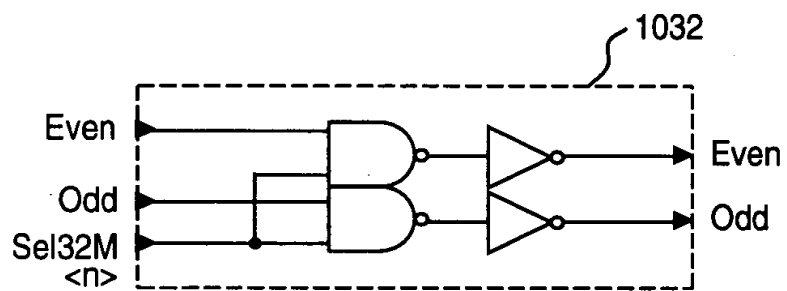


FIG. 67

**FIG. 68A**

**FIG. 68B**

**FIG. 69**

**FIG. 70**

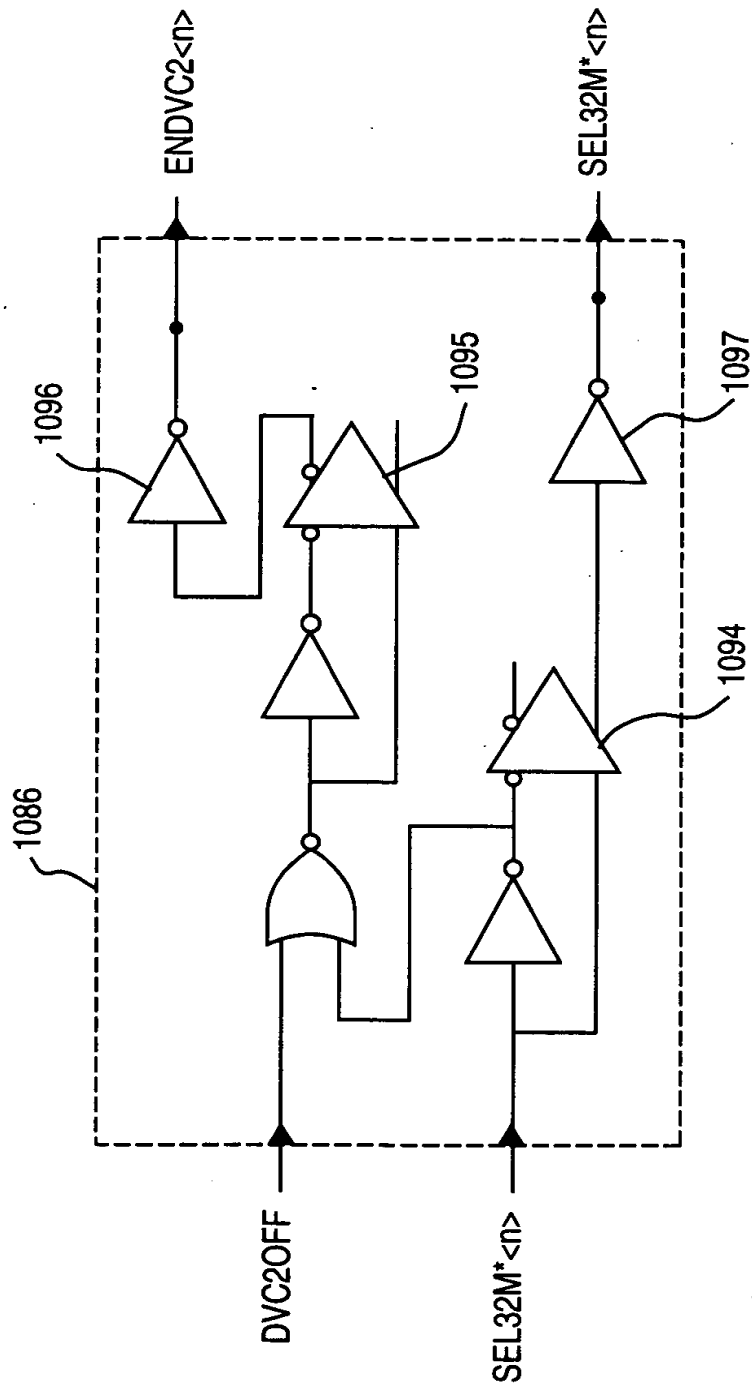
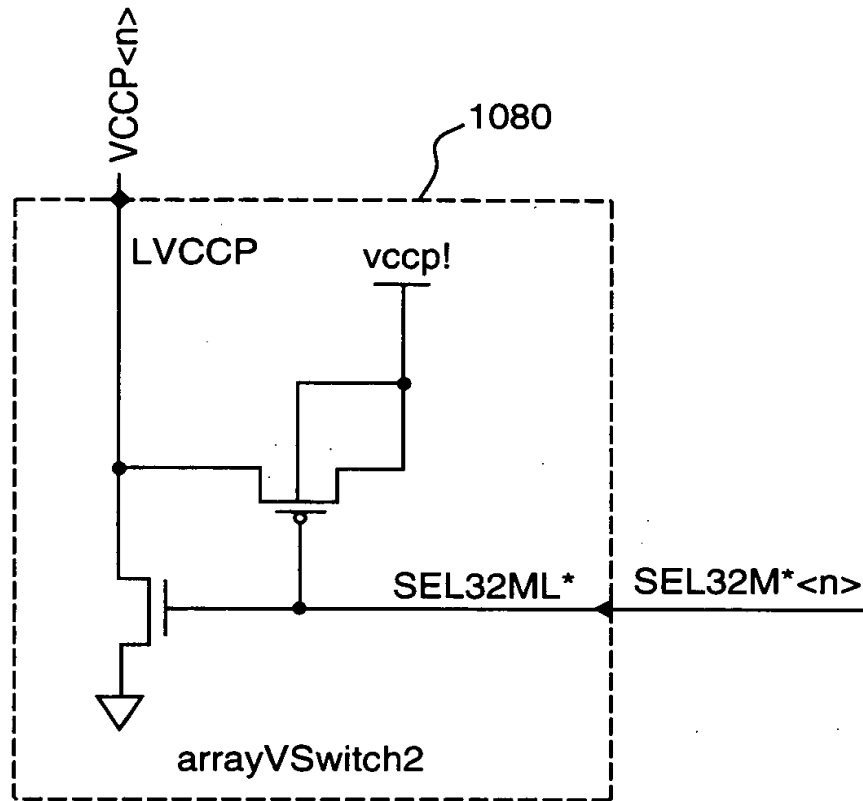


FIG. 71A

**FIG. 71B**

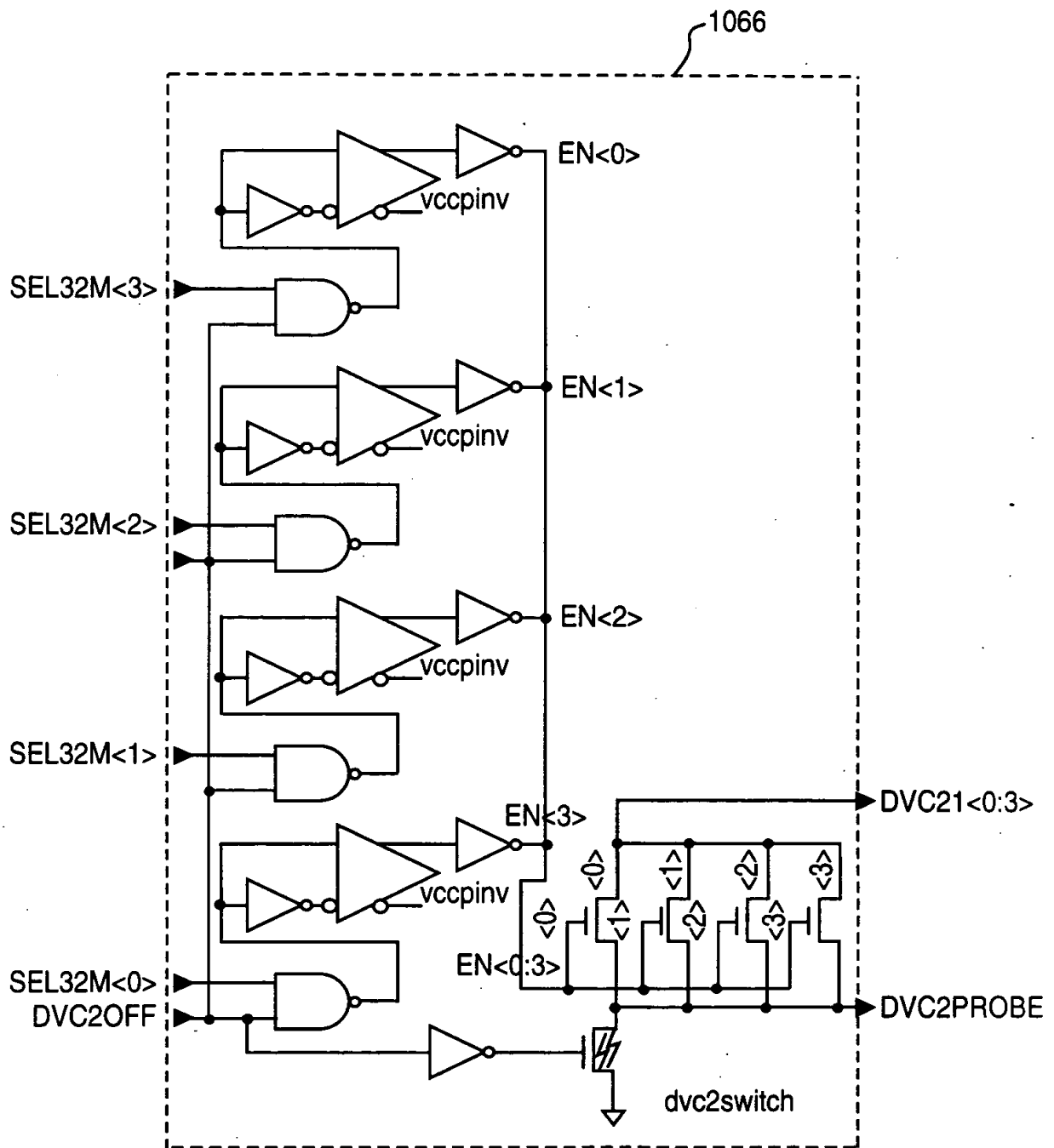
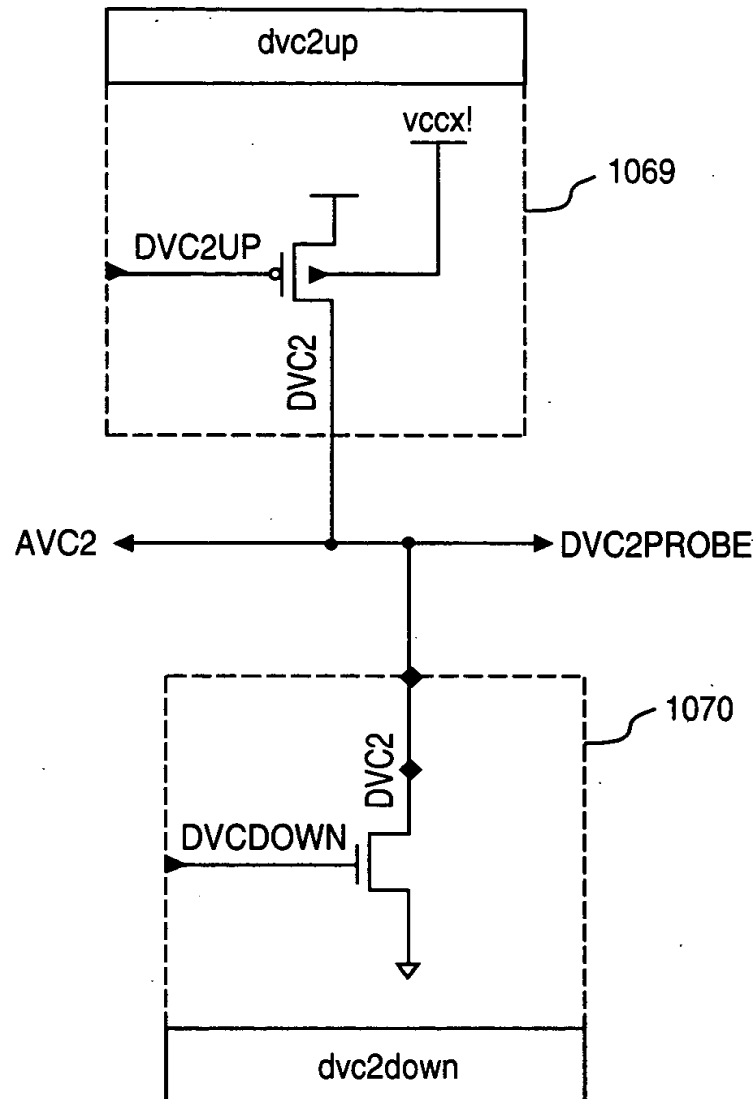


FIG. 72A

**FIG. 72B**

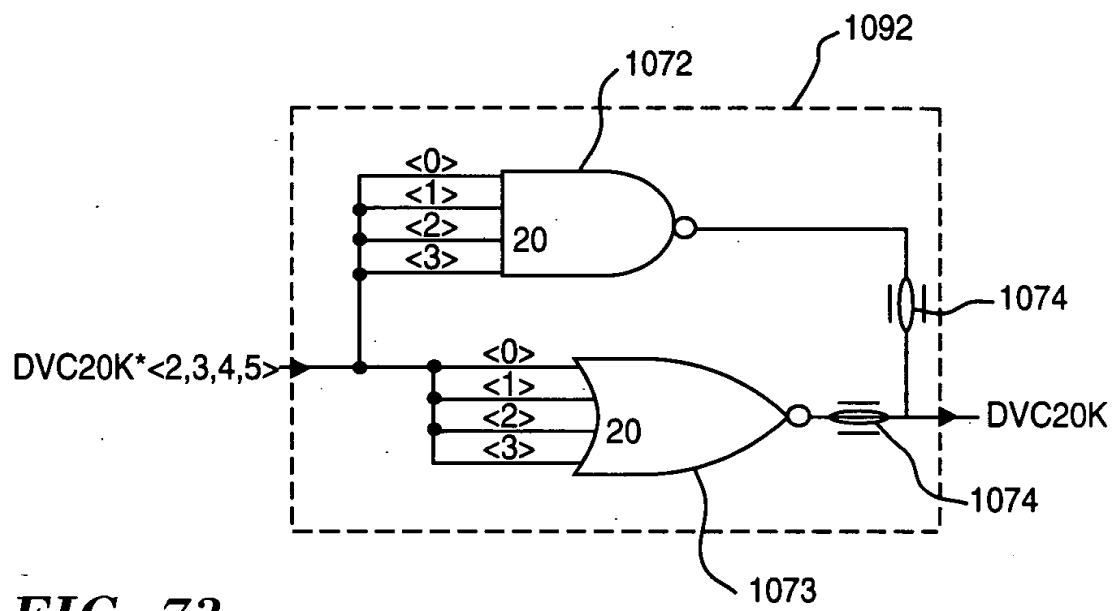
**FIG. 73**

FIG. 74

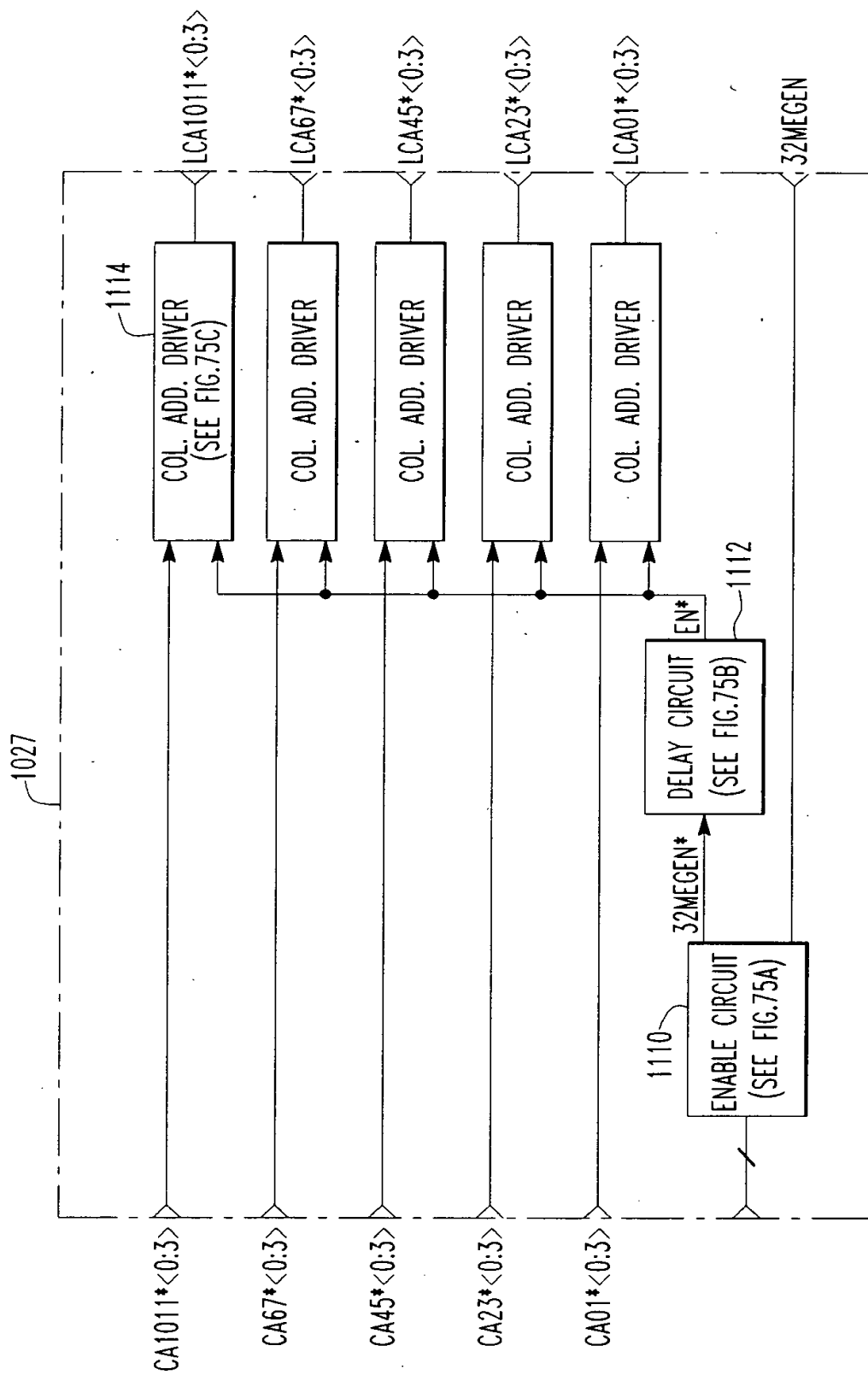


FIG. 74

FIG. 75A

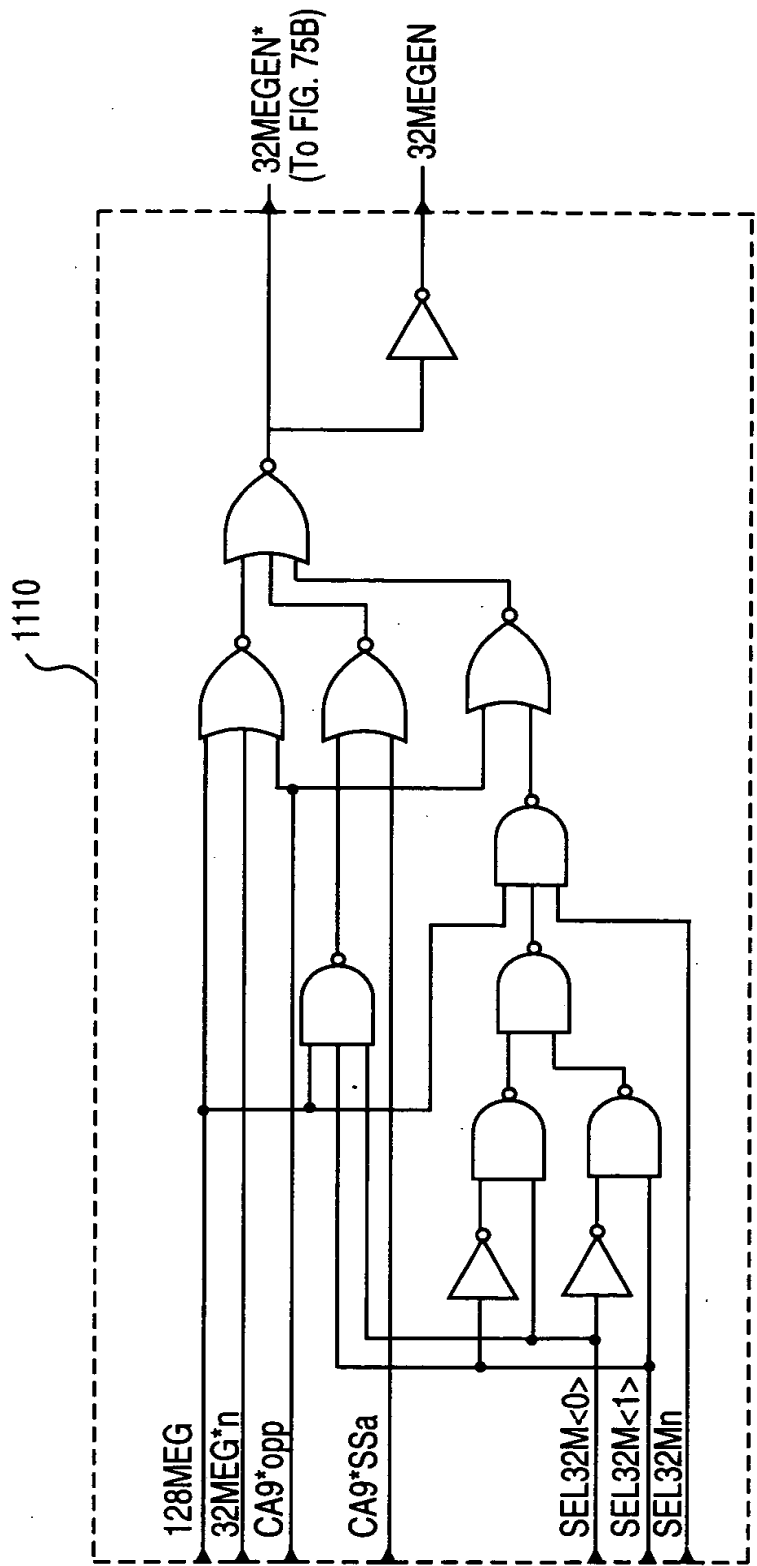


FIG. 75A

FIG. 75B

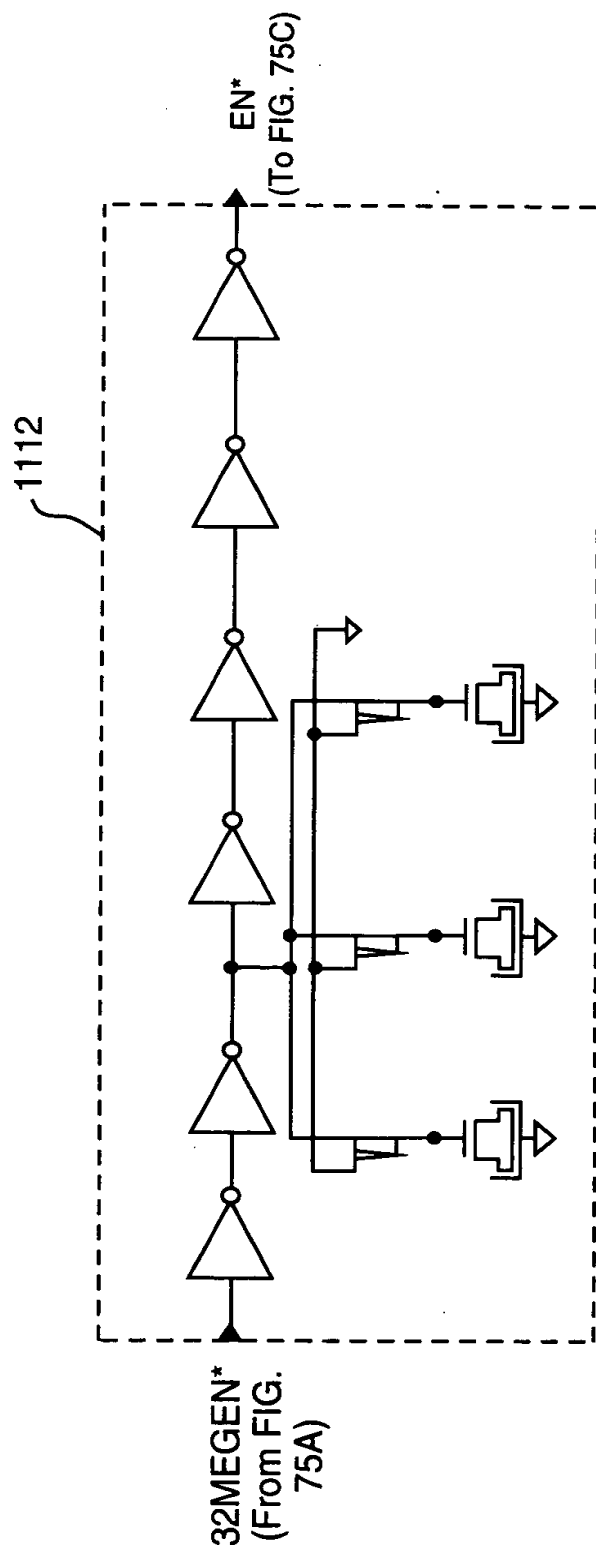


FIG. 75B

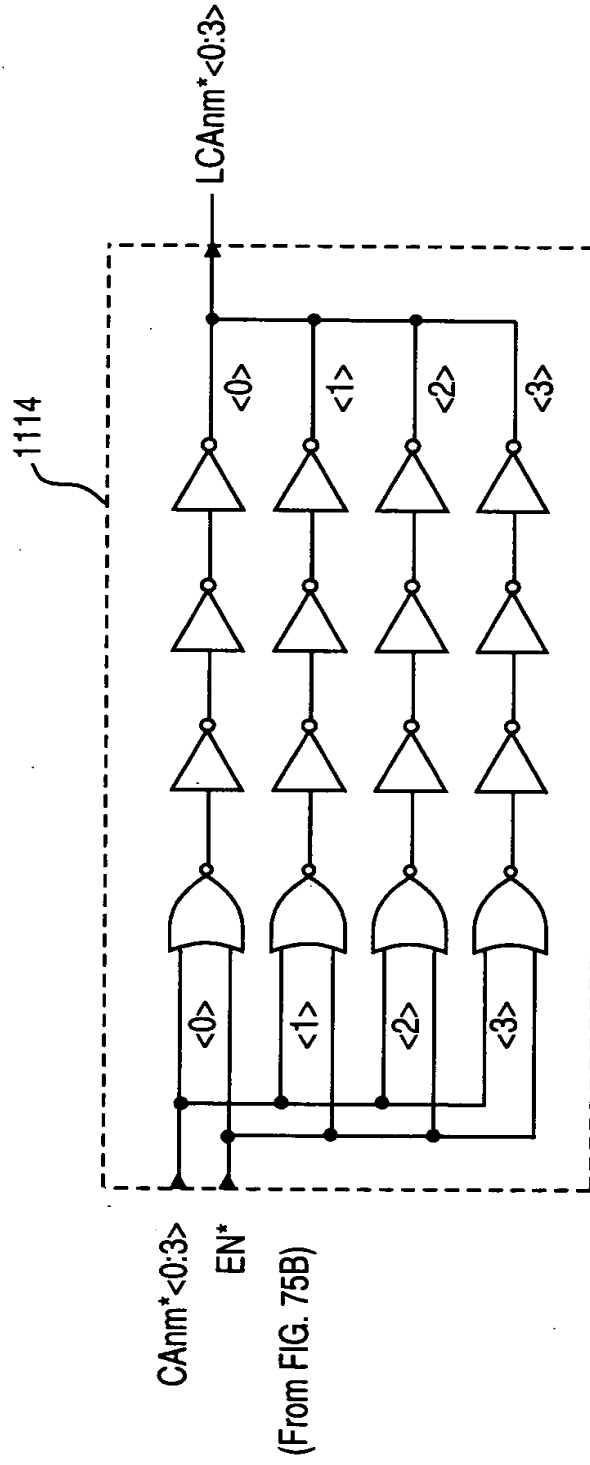


FIG. 75C

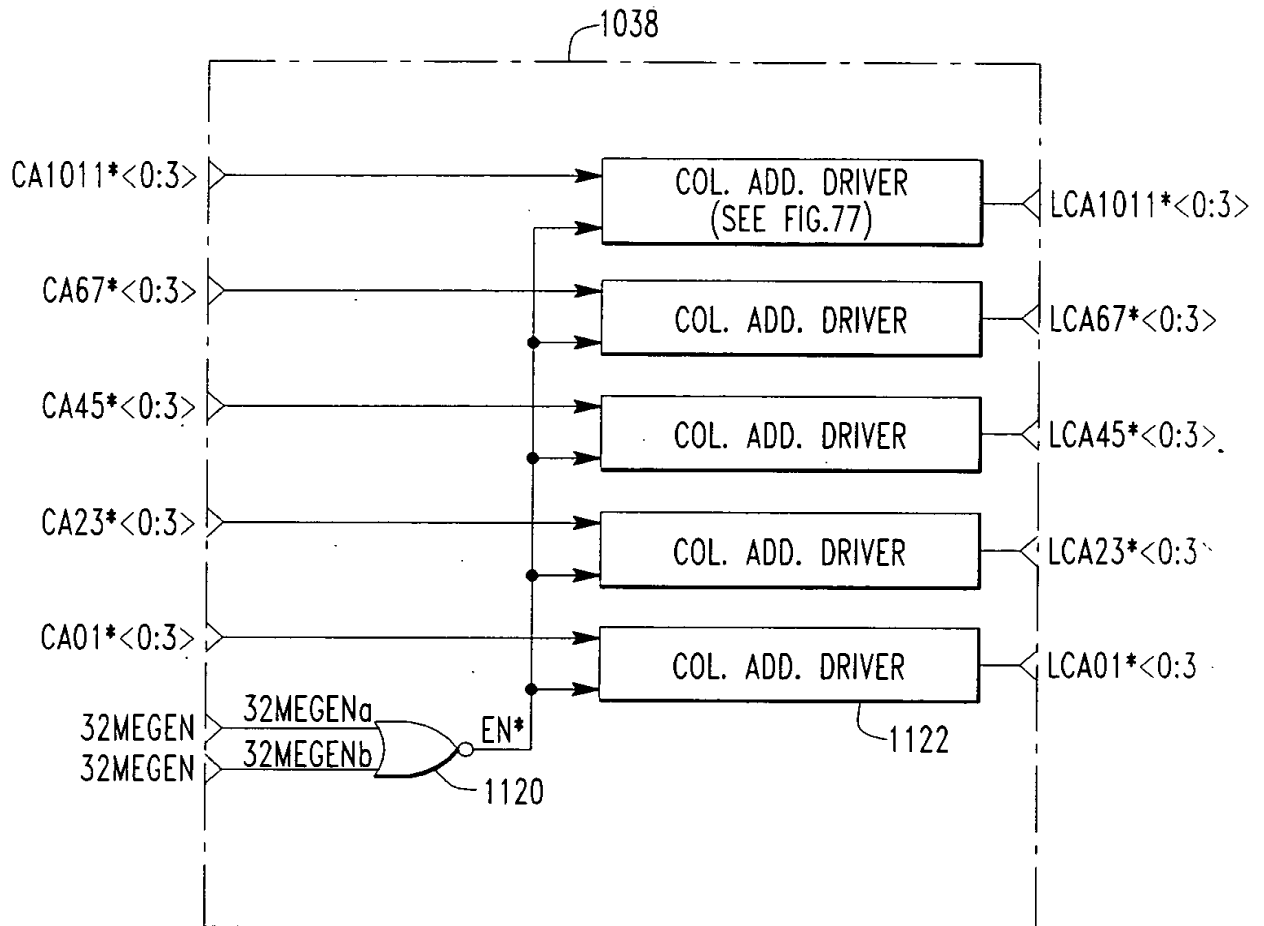


FIG. 76

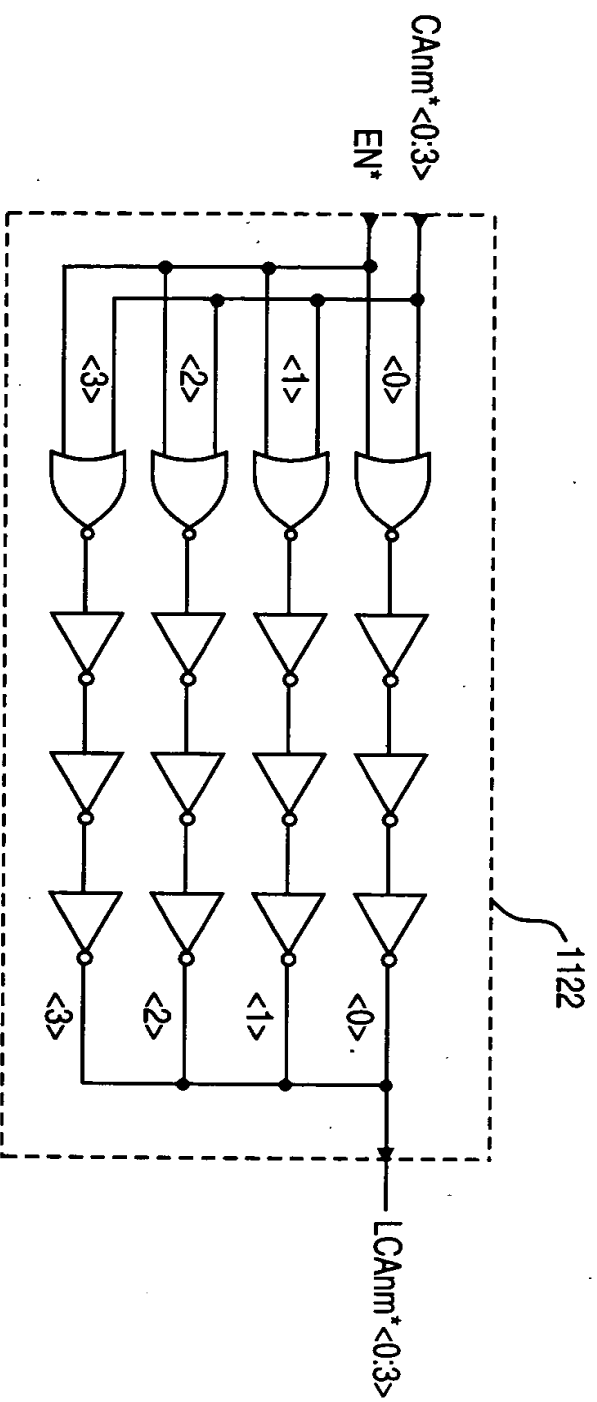


FIG. 77

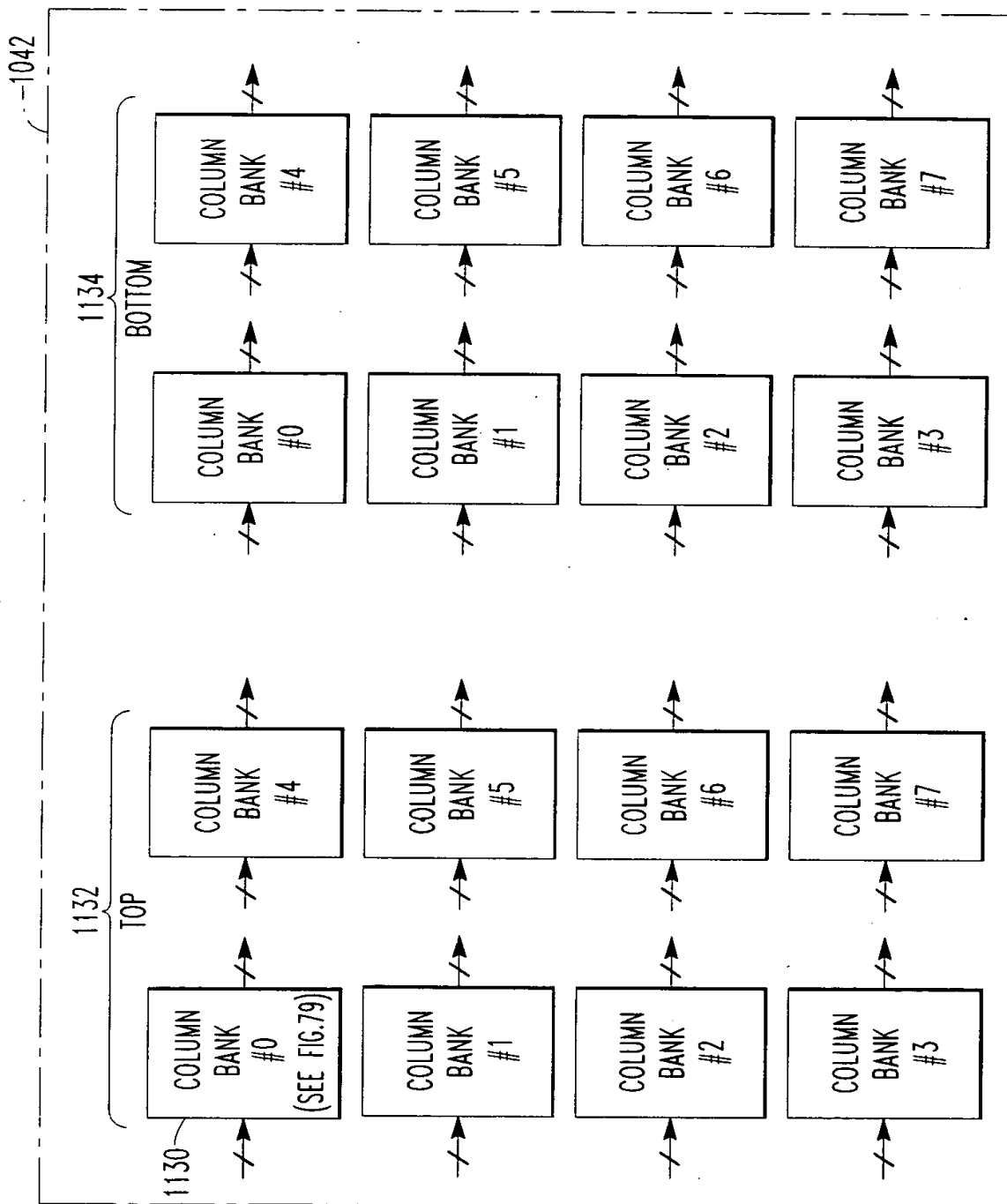
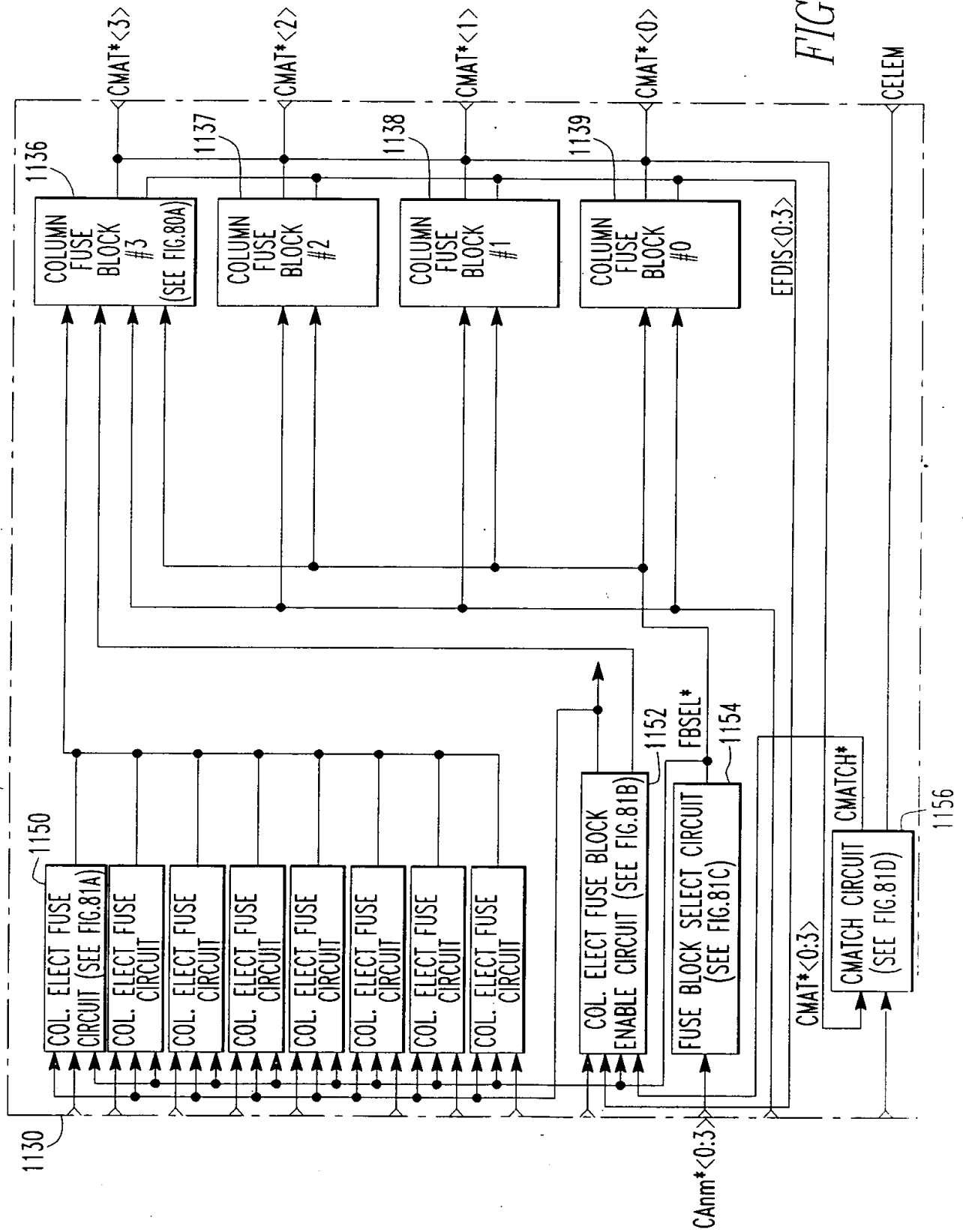


FIG. 78

FIG. 79



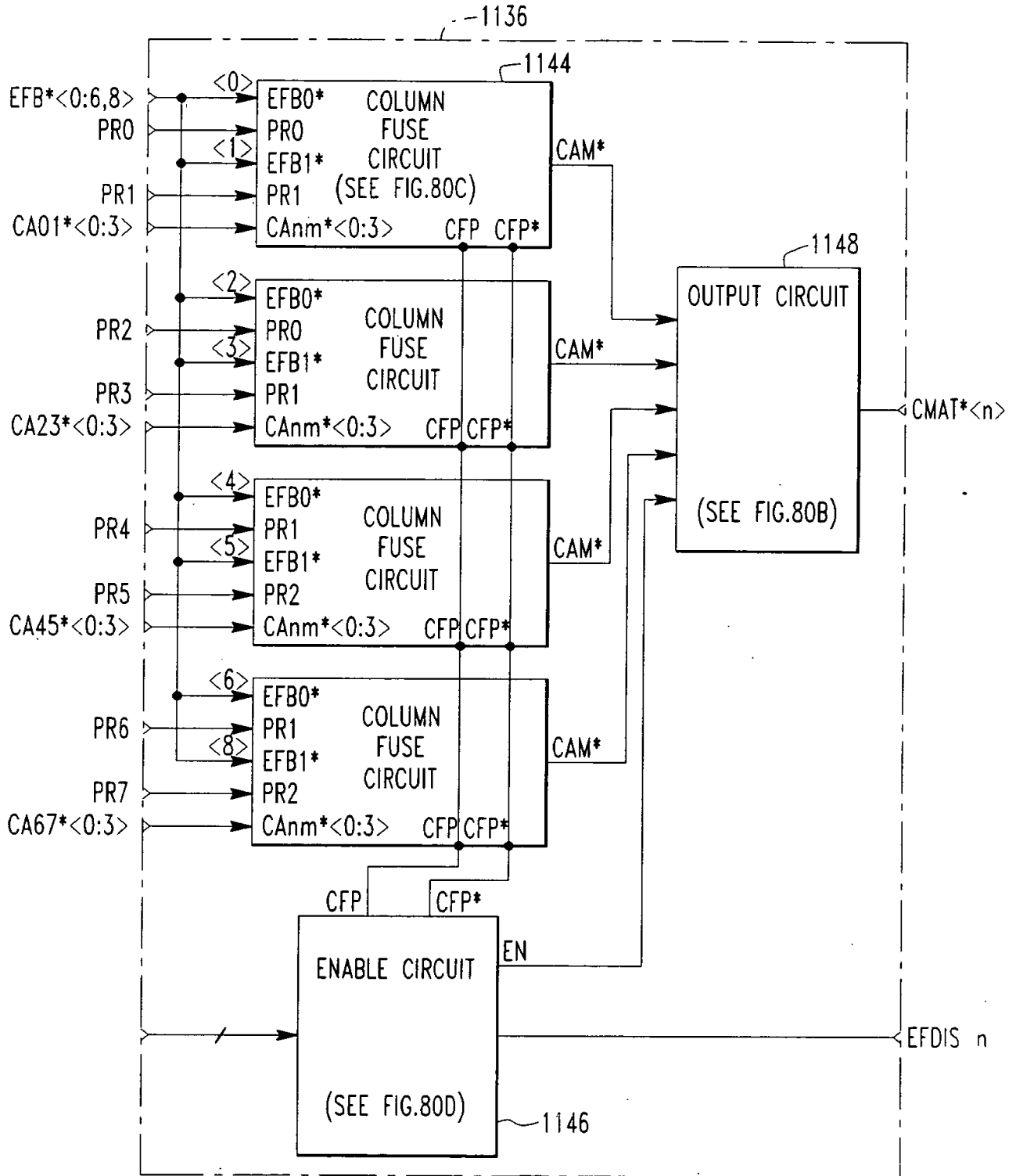
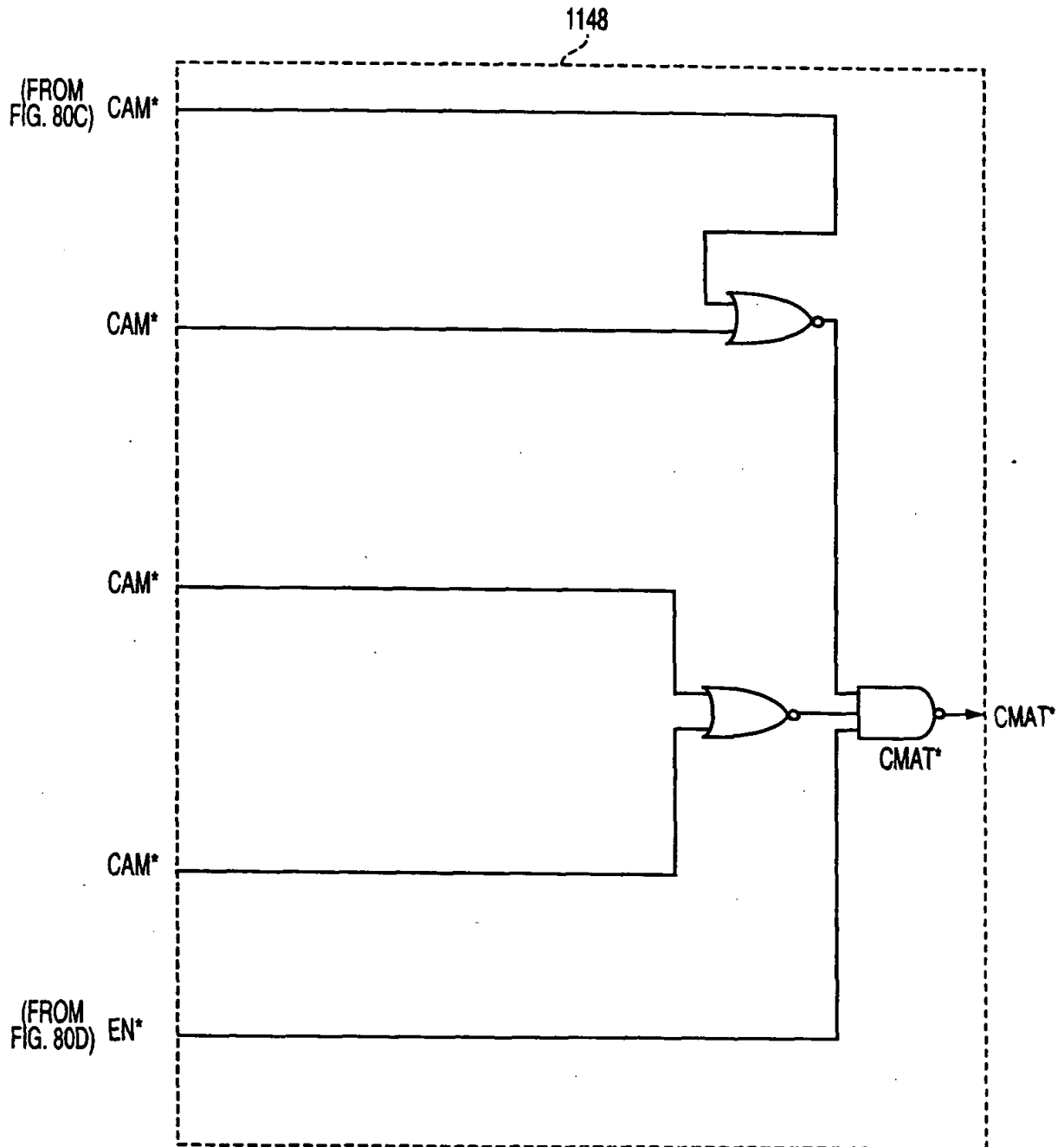


FIG. 80A

**FIG. 80B**

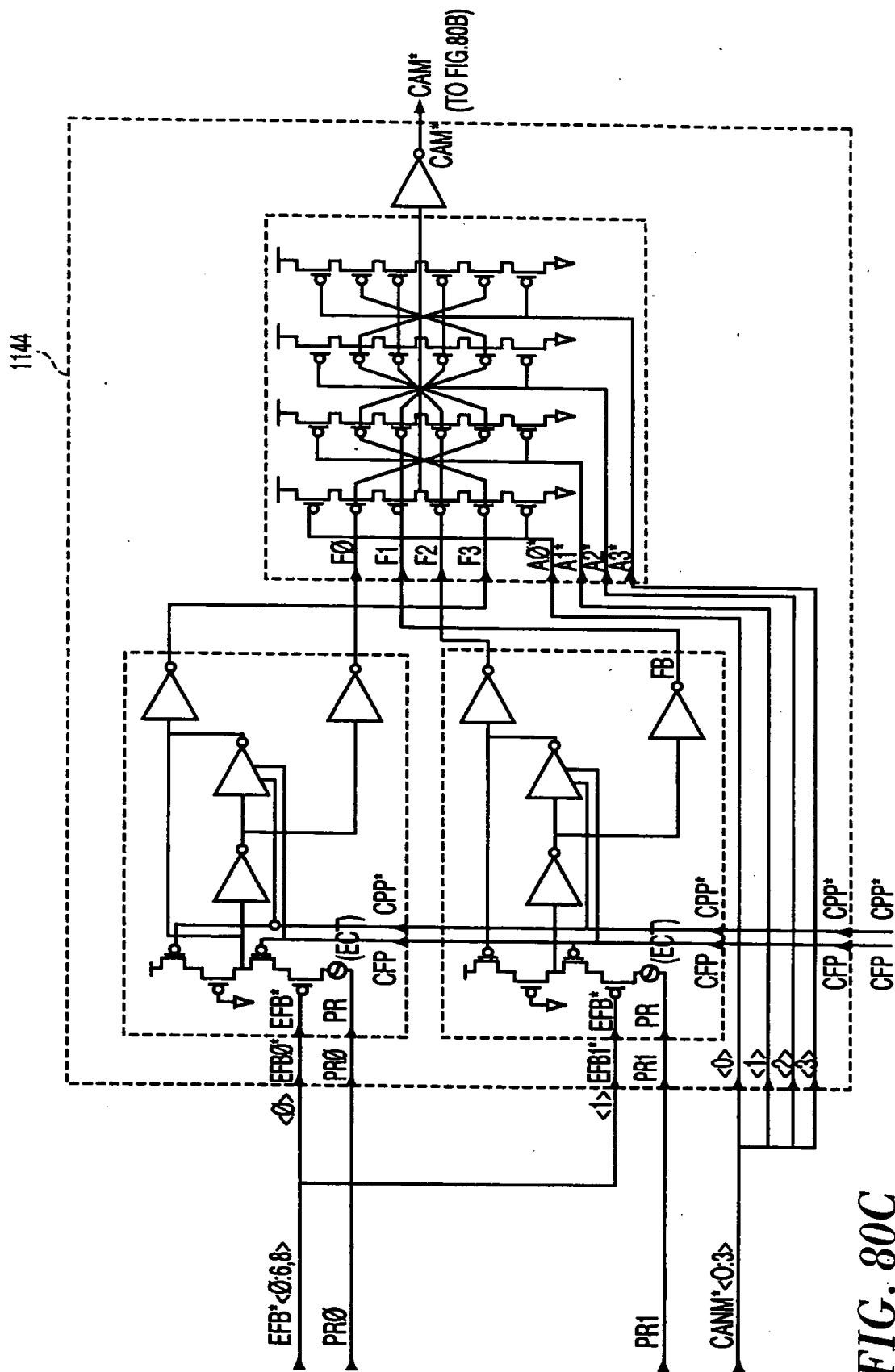


FIG. 80C

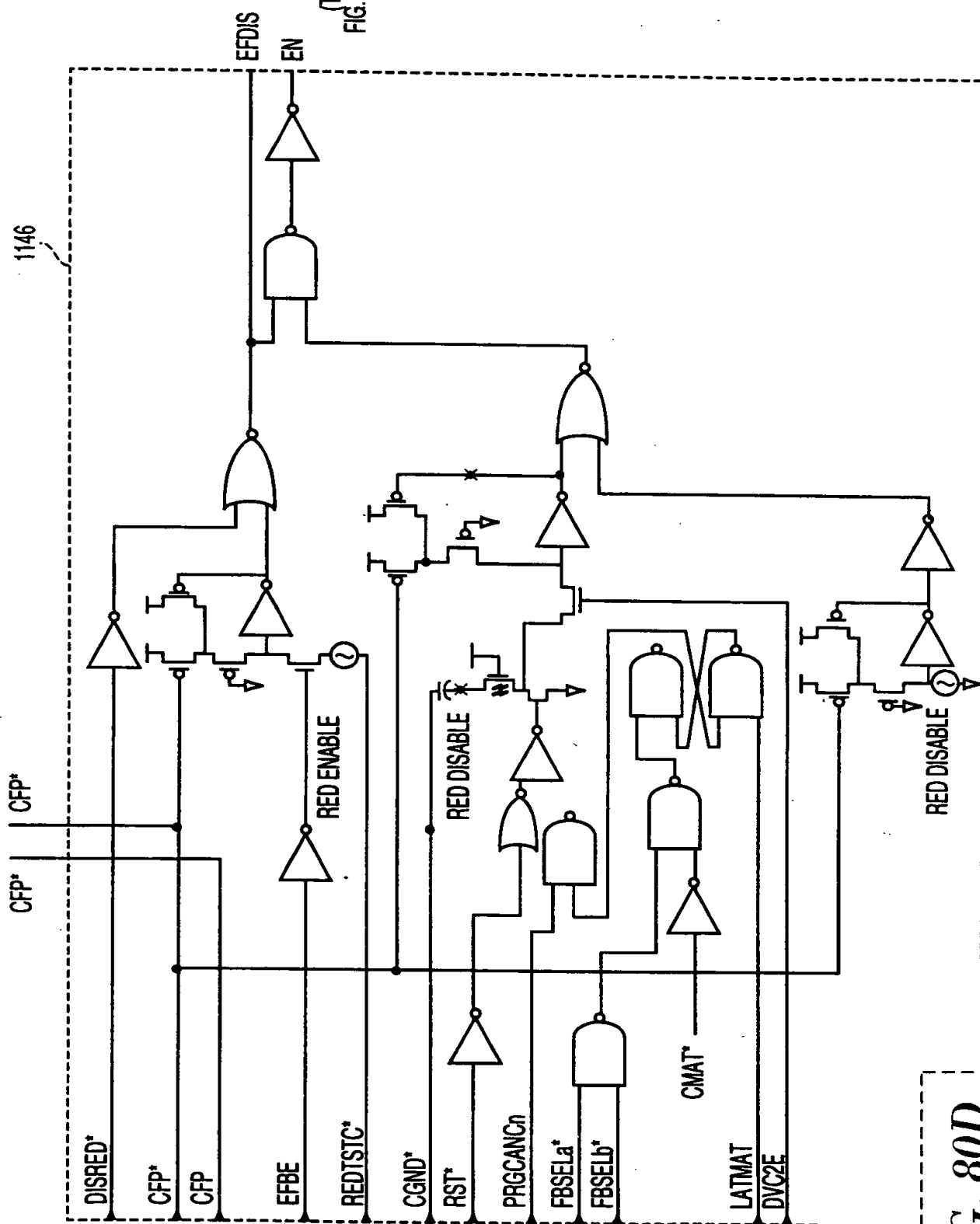


FIG. 80D

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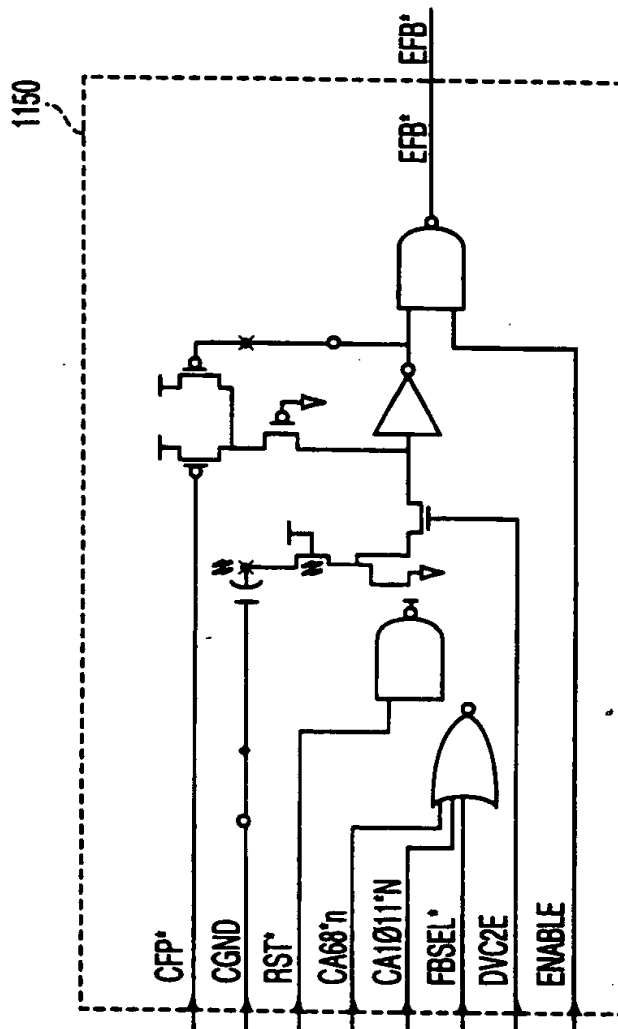


FIG. 81A

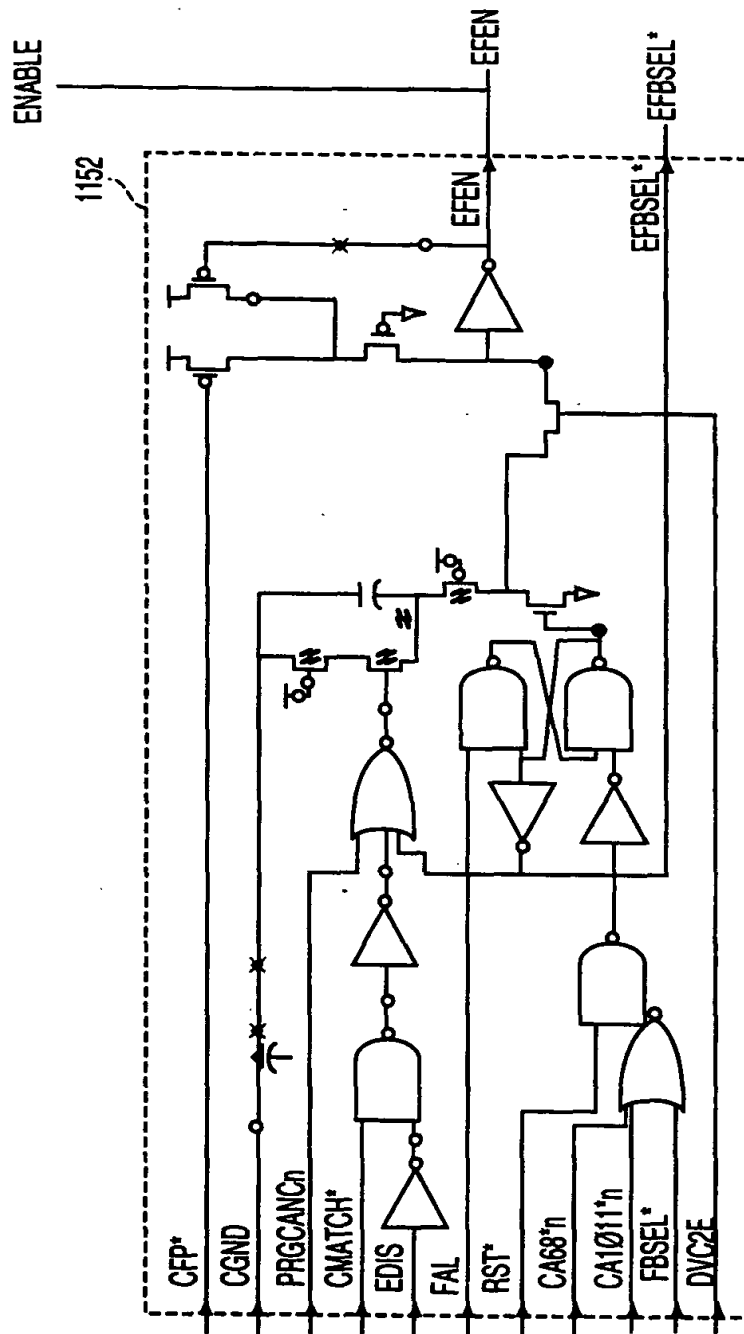


FIG. 81B

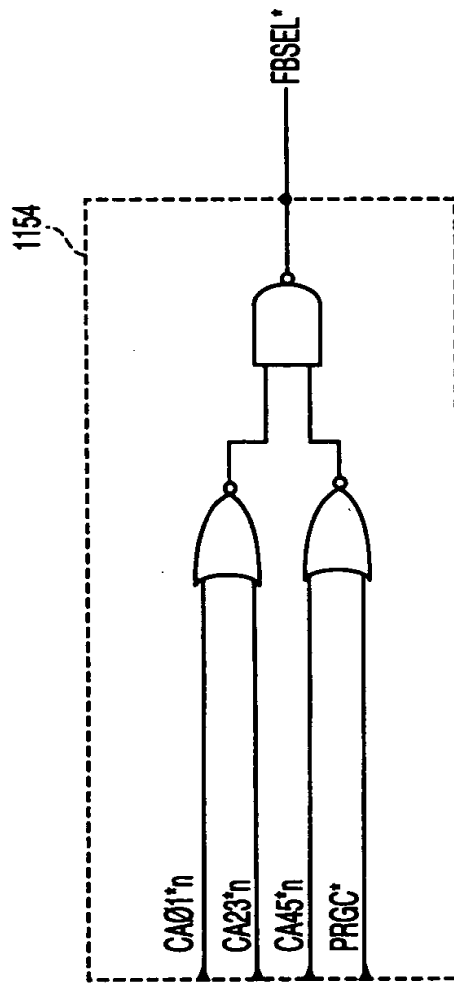


FIG. 81C

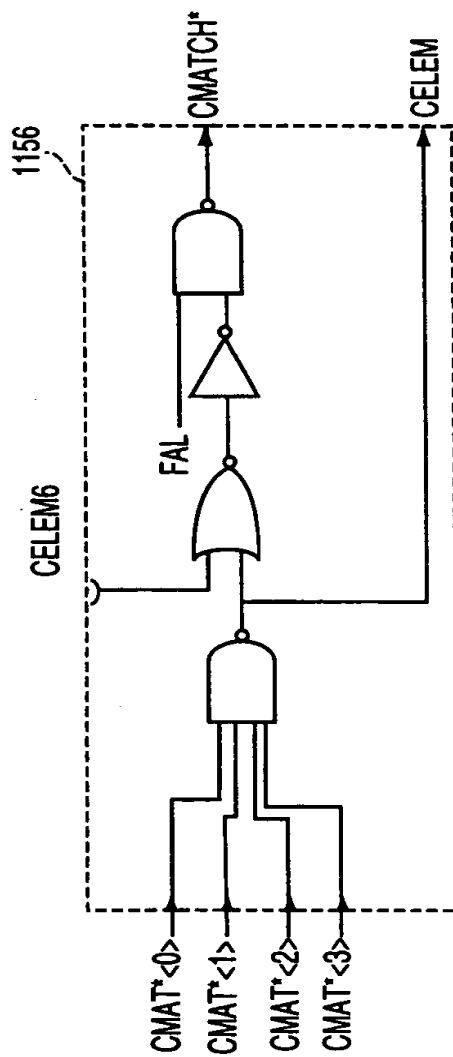


FIG. 81D

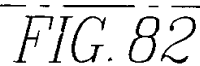


FIG. 82

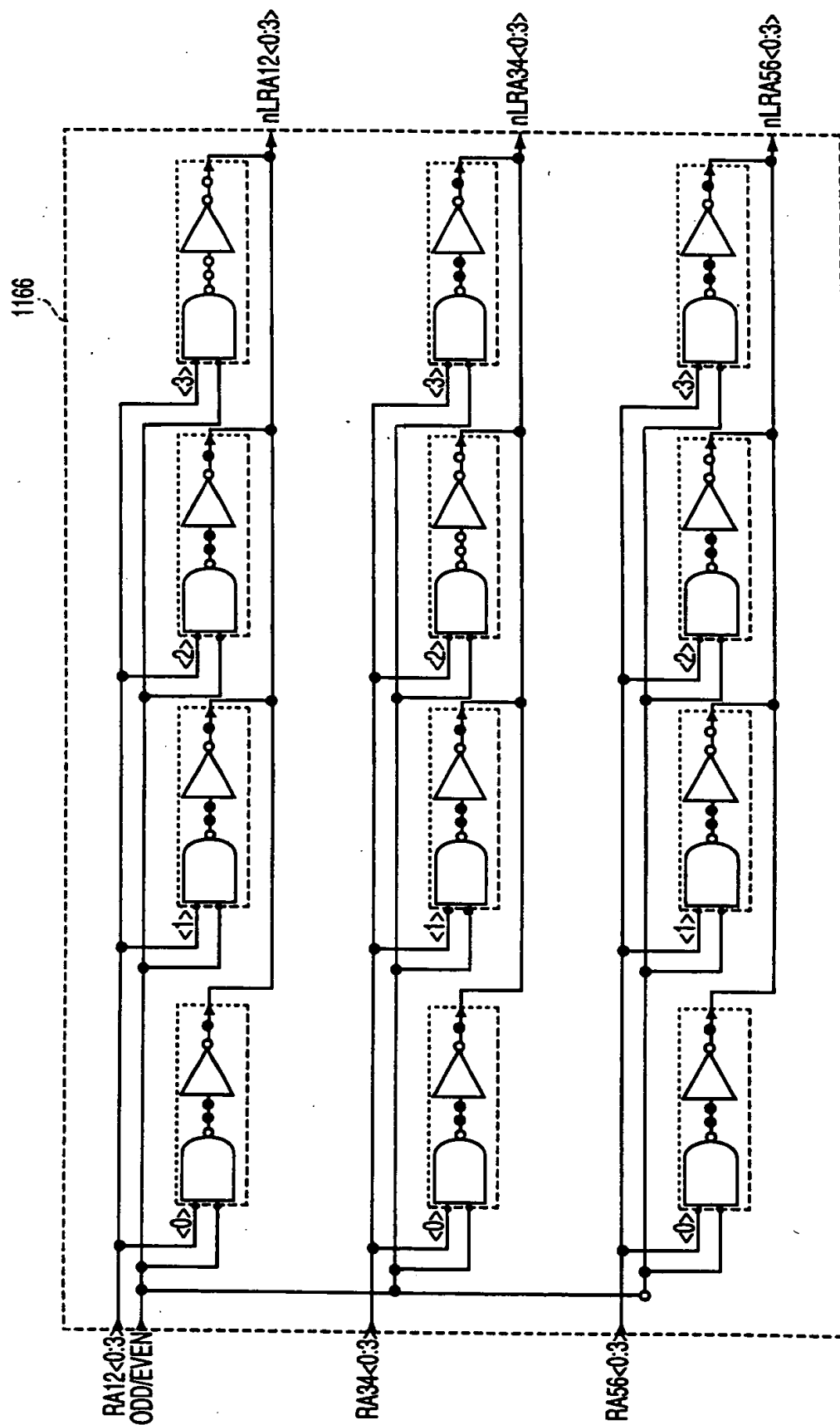


FIG. 83A

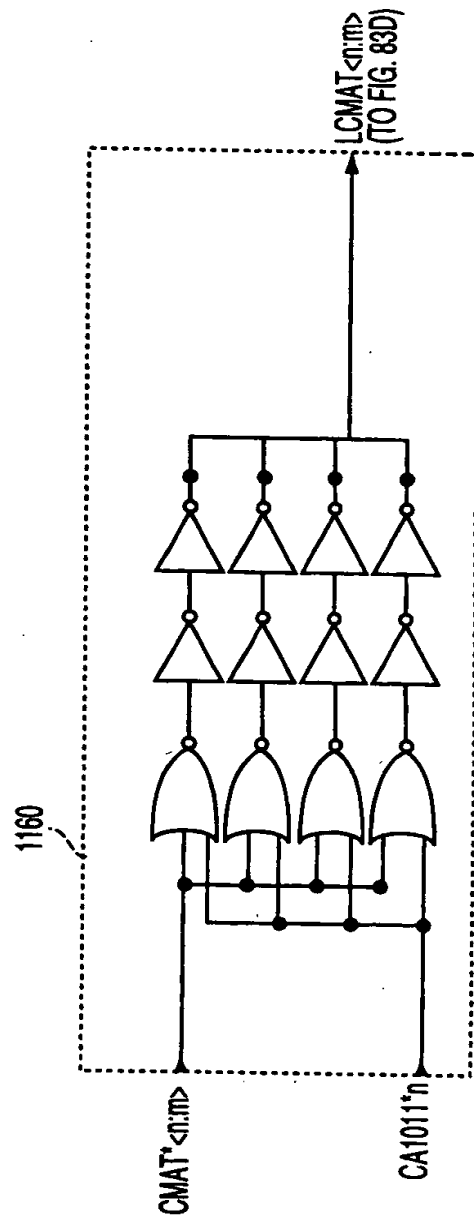


FIG. 83B

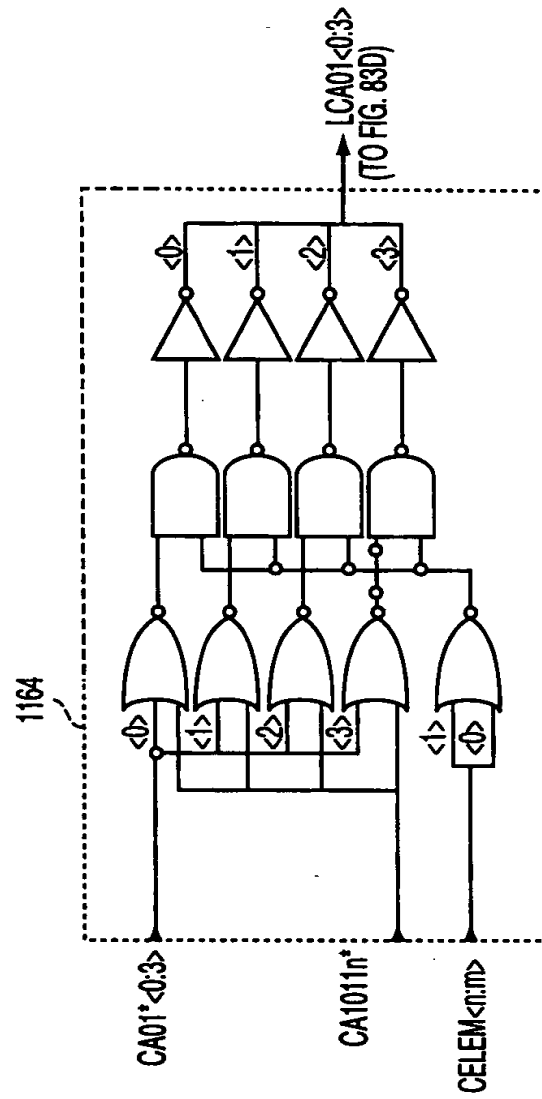


FIG. 83C

FIG. 84A

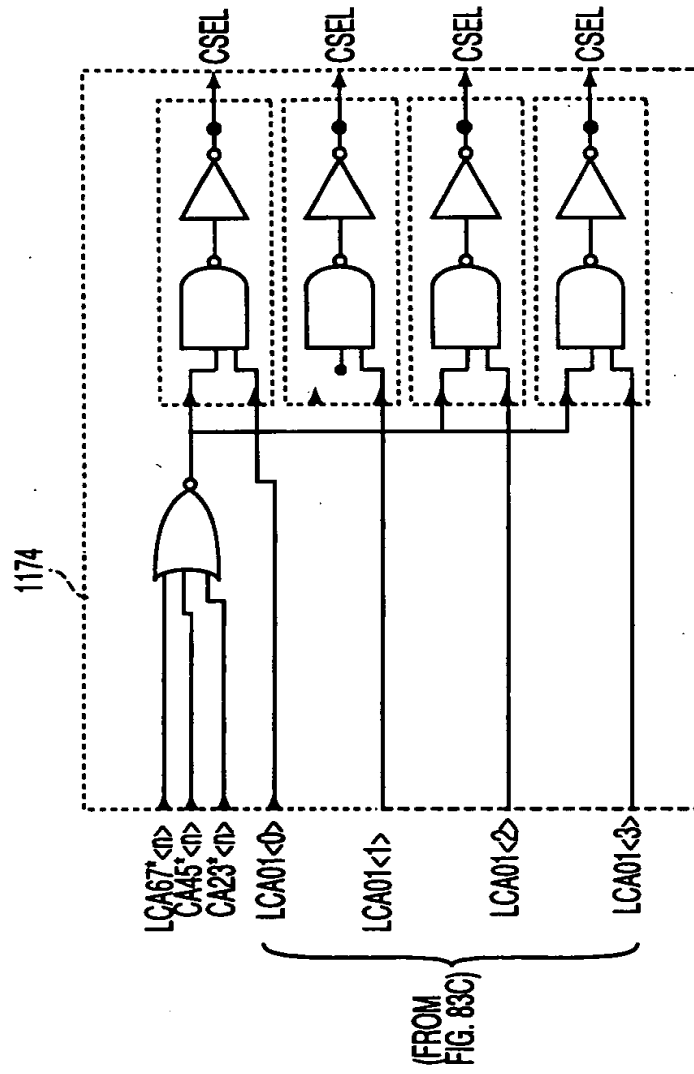
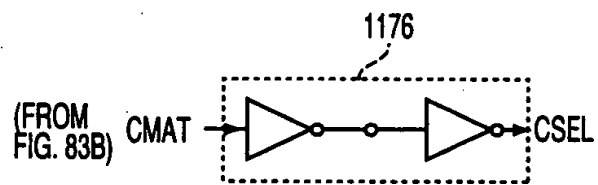


FIG. 84A

**FIG. 84B**

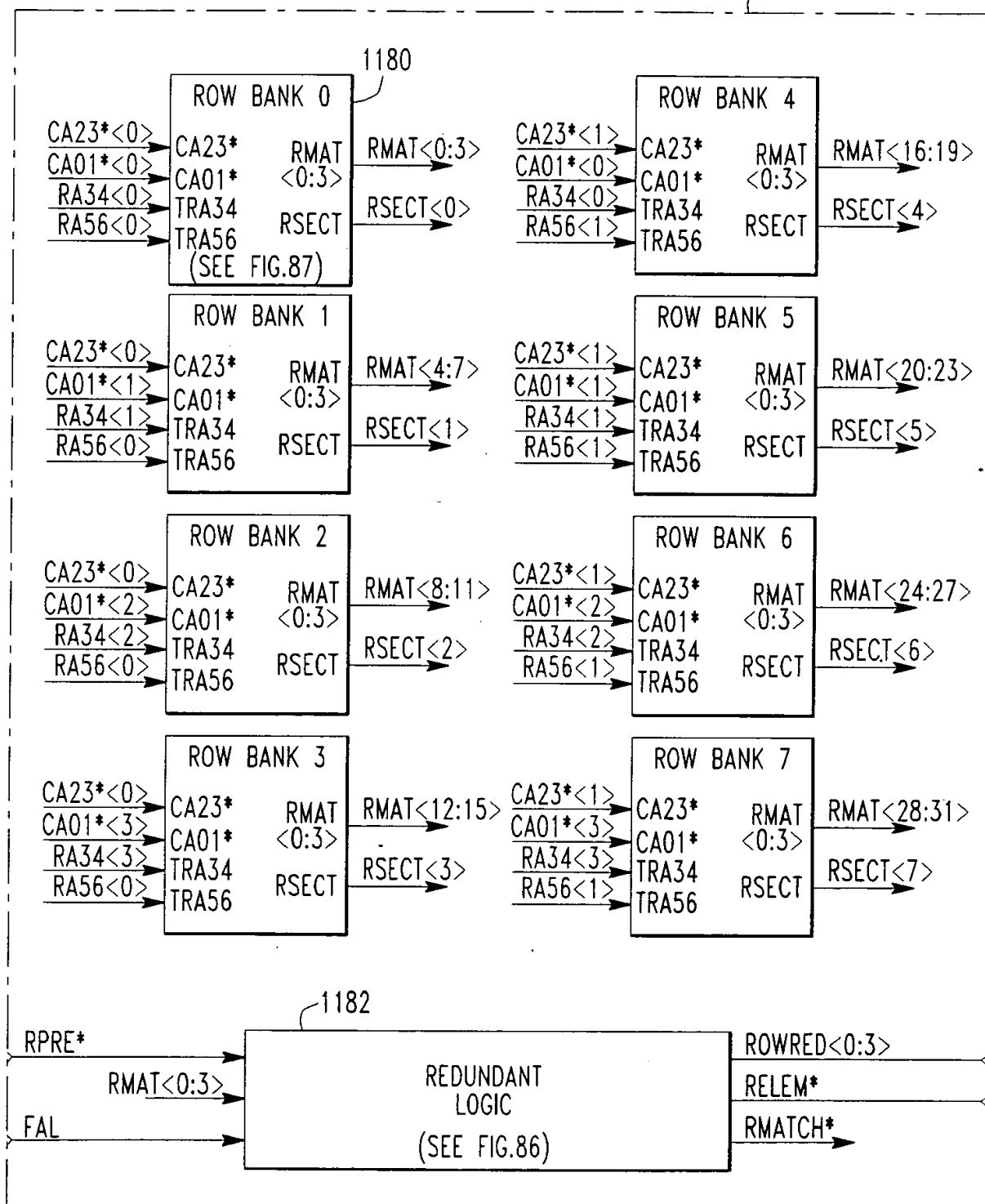


FIG. 85

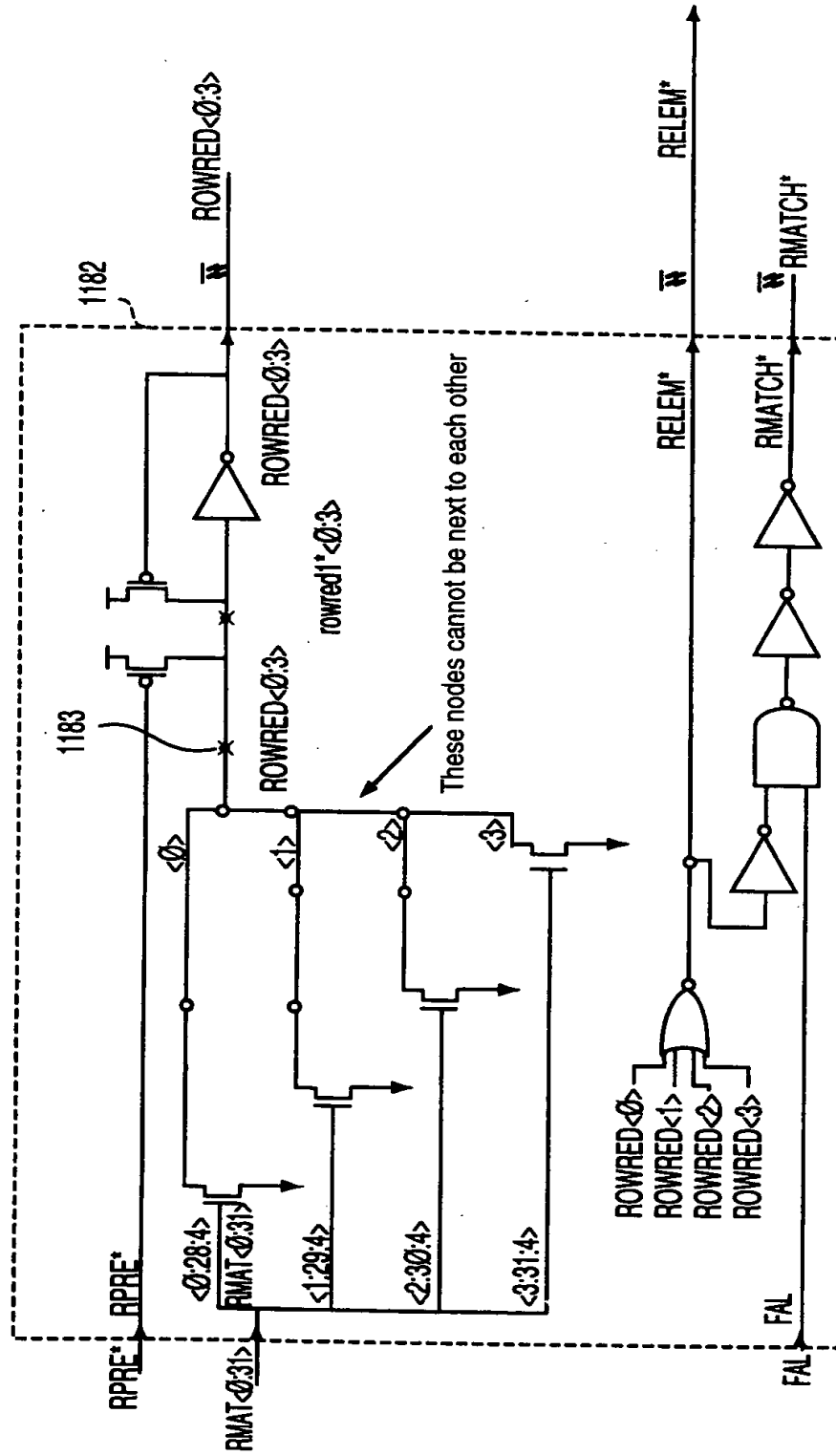
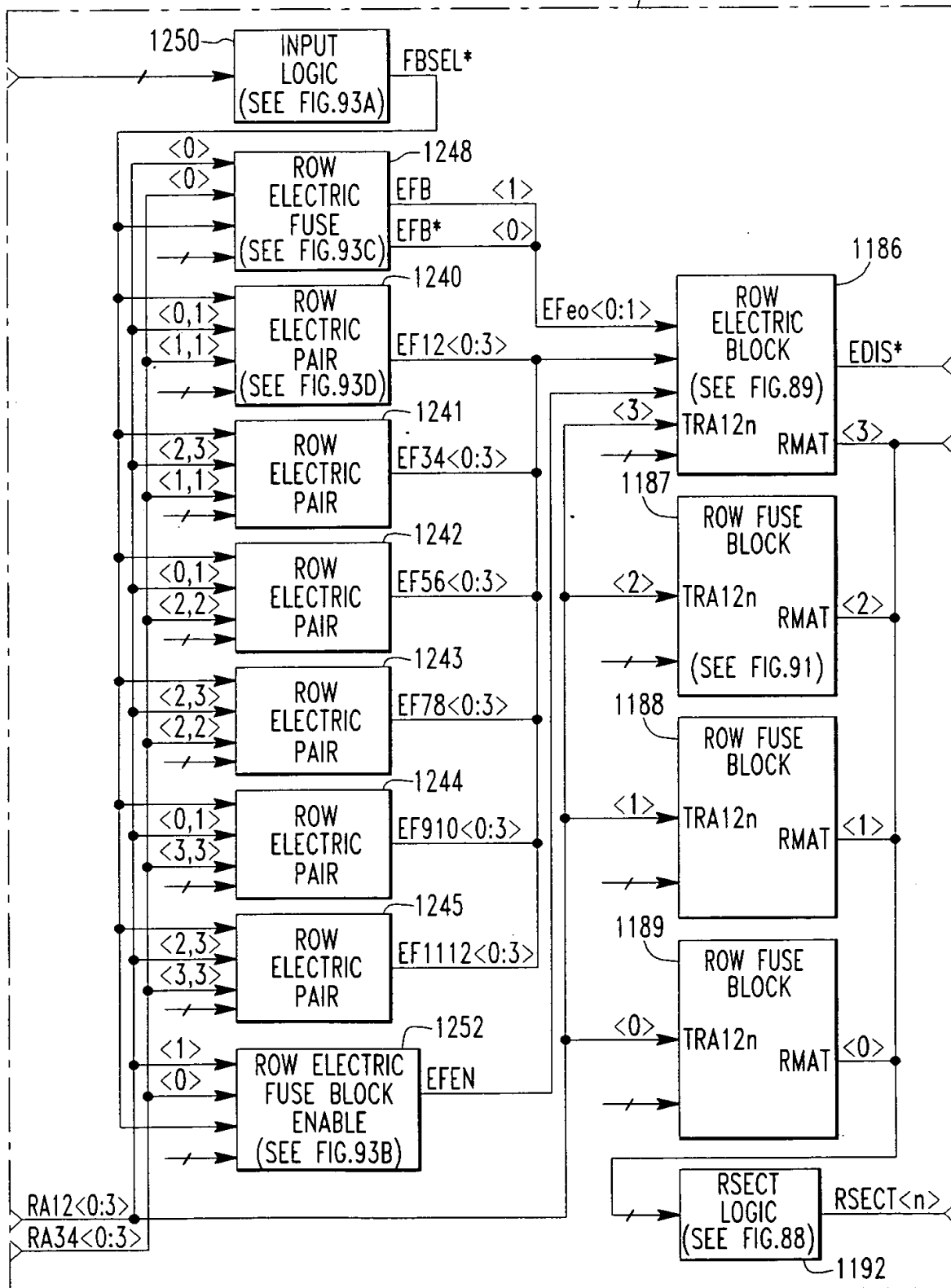
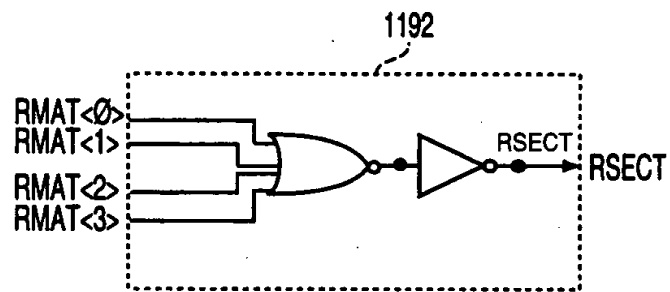


FIG. 86



**FIG. 88**

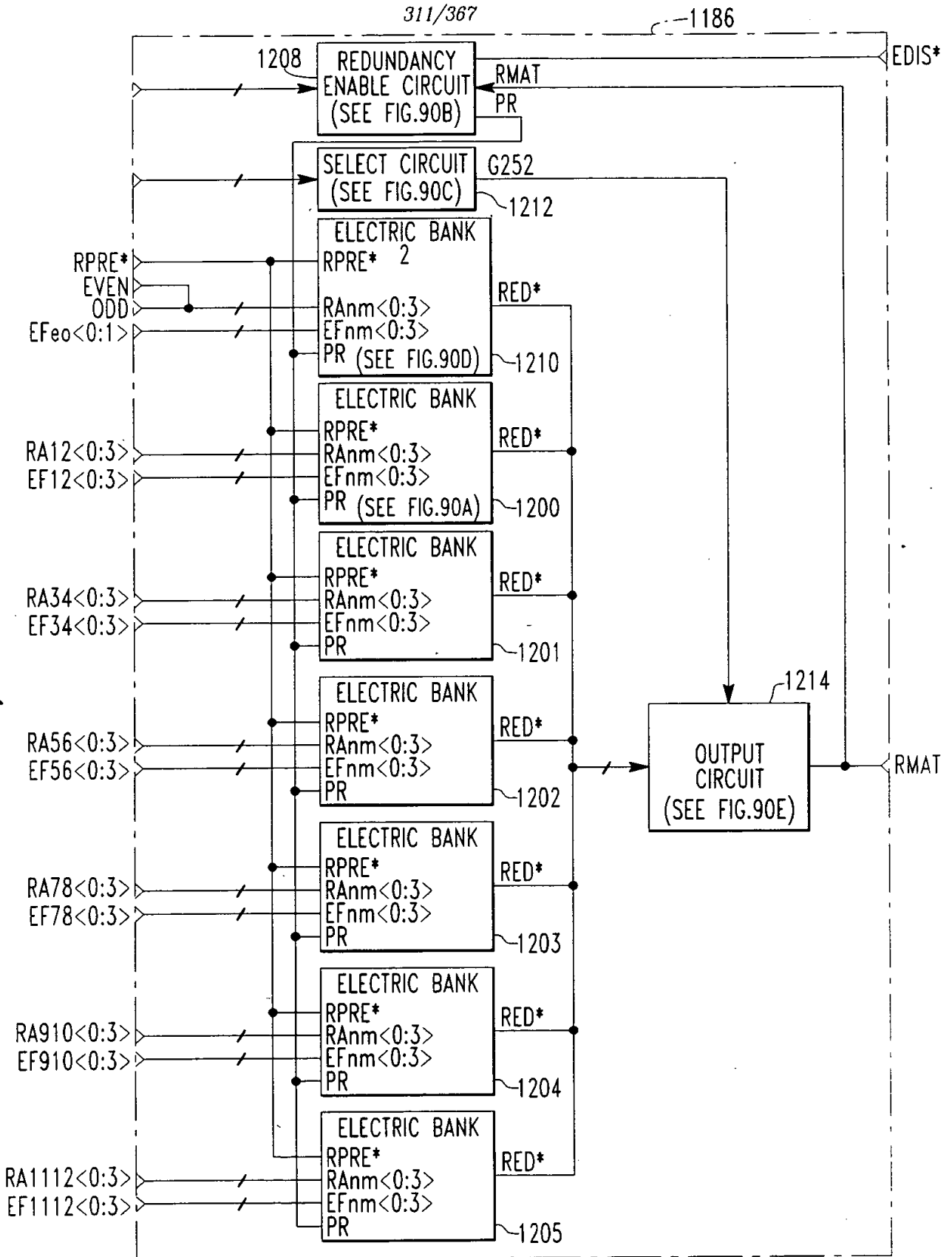


FIG. 89

FIG. 90A

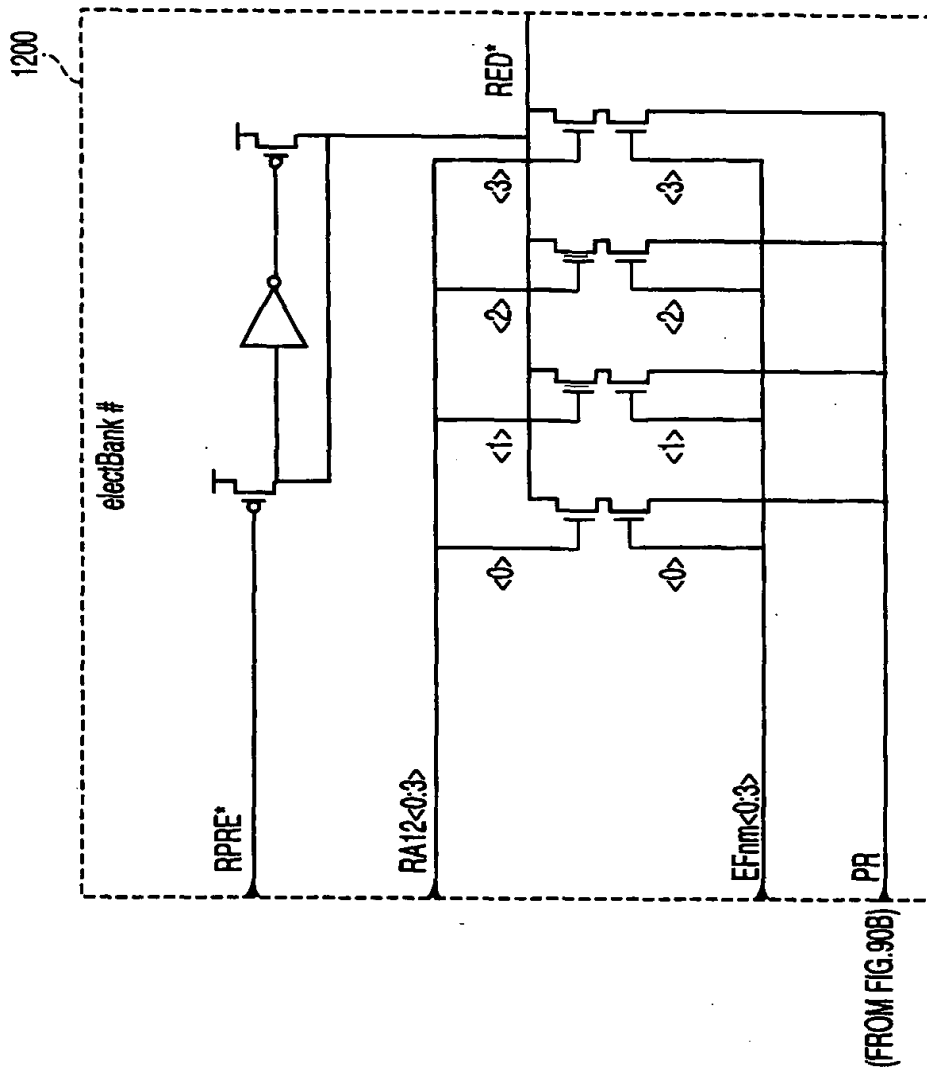


FIG. 90A

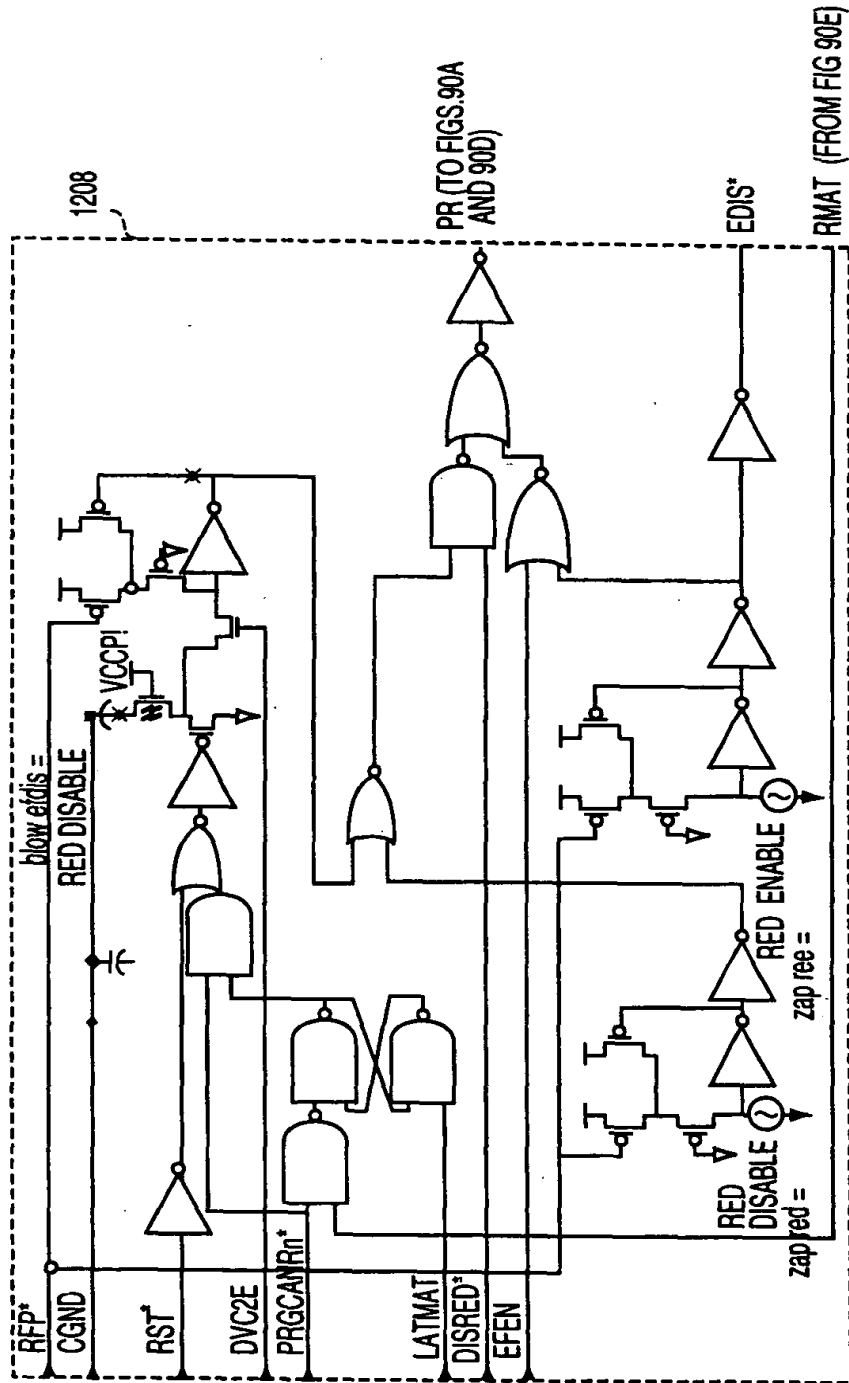


FIG. 90B

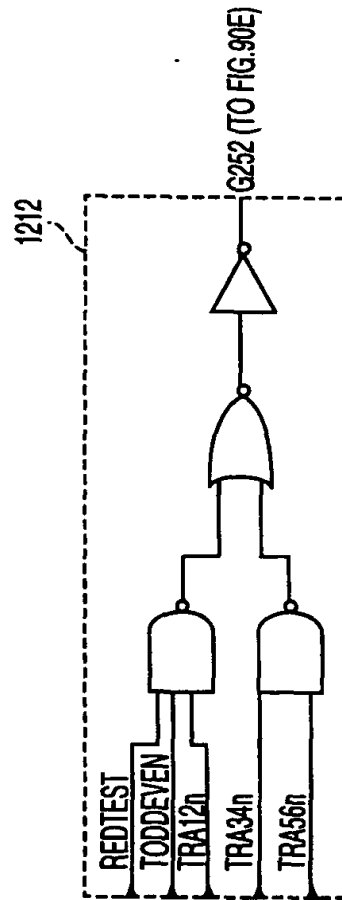


FIG. 90C

FIG. 90C

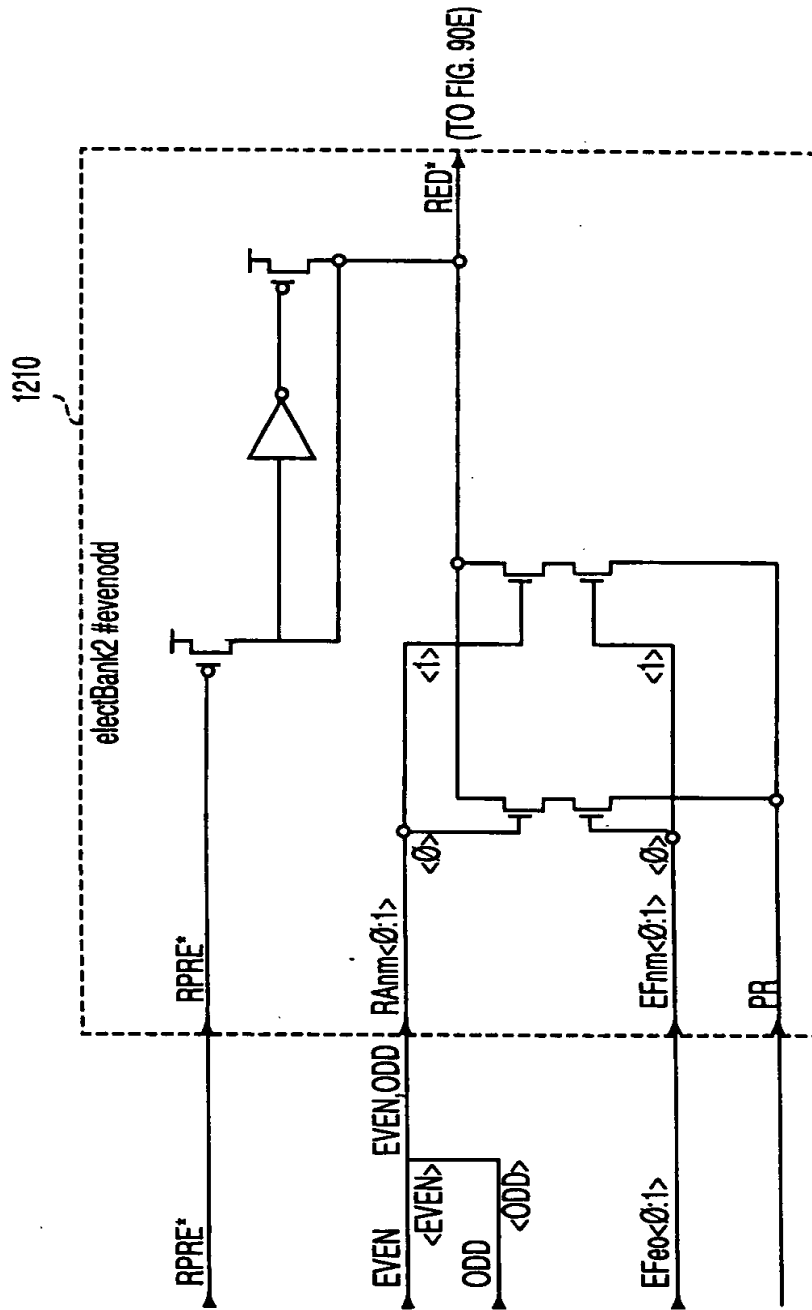
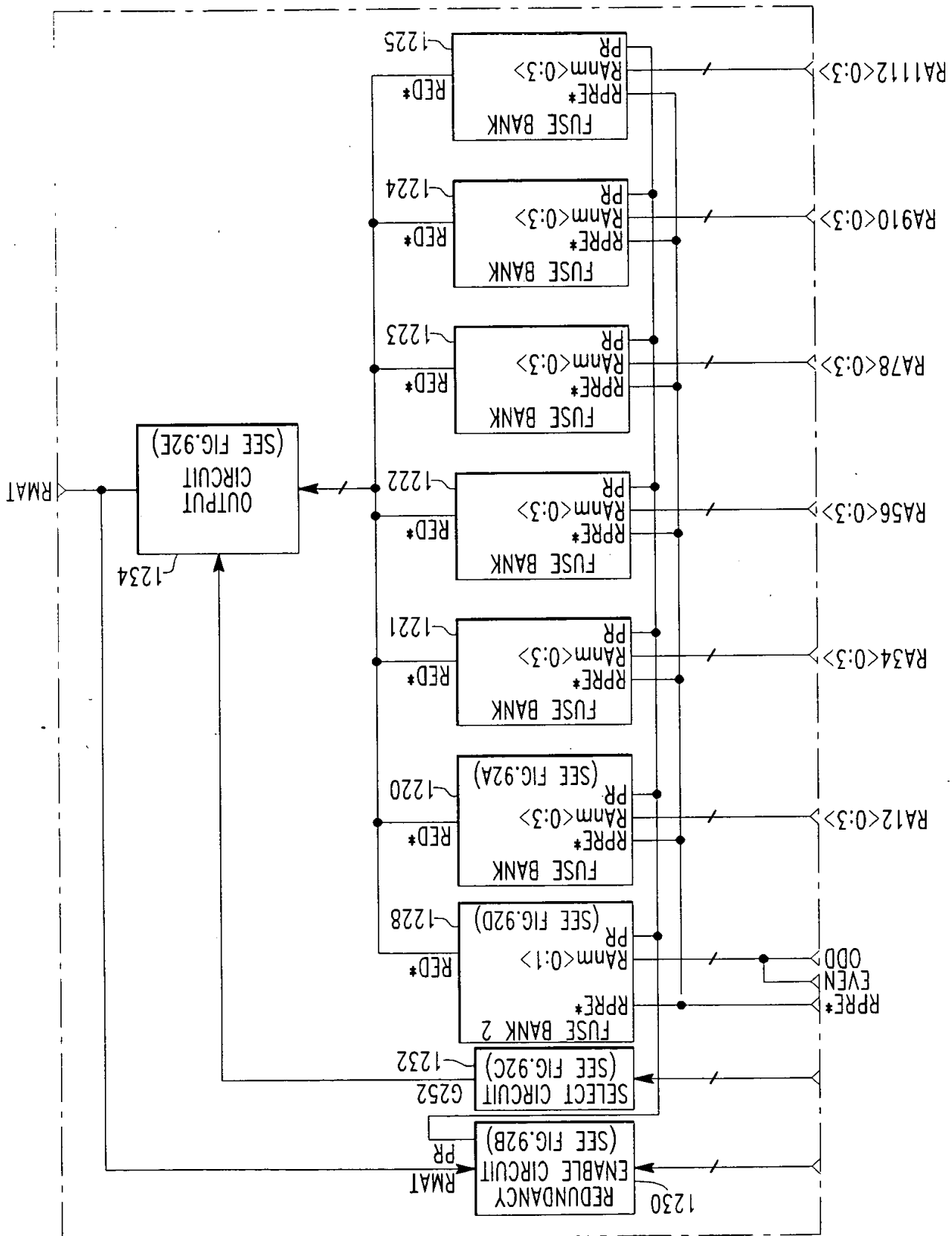


FIG. 90D



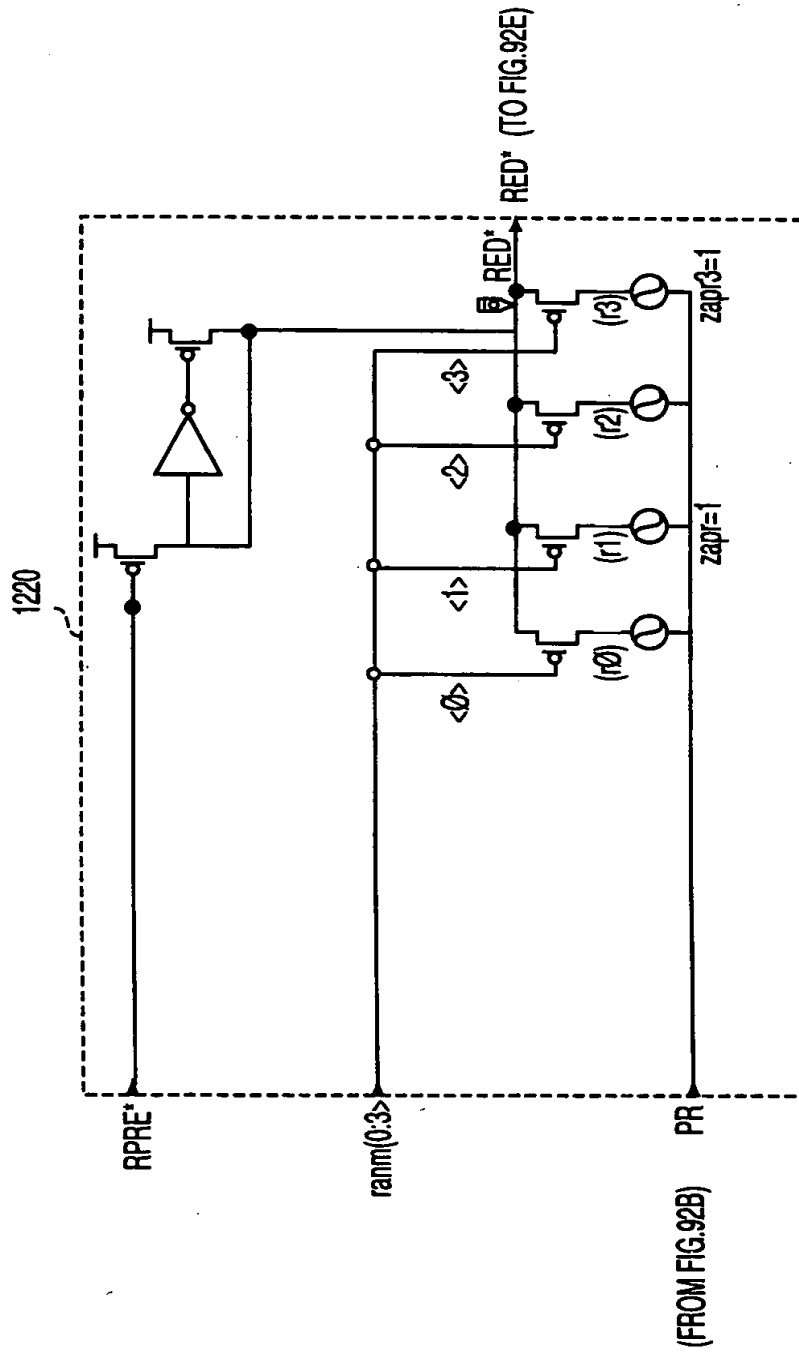


FIG. 92A

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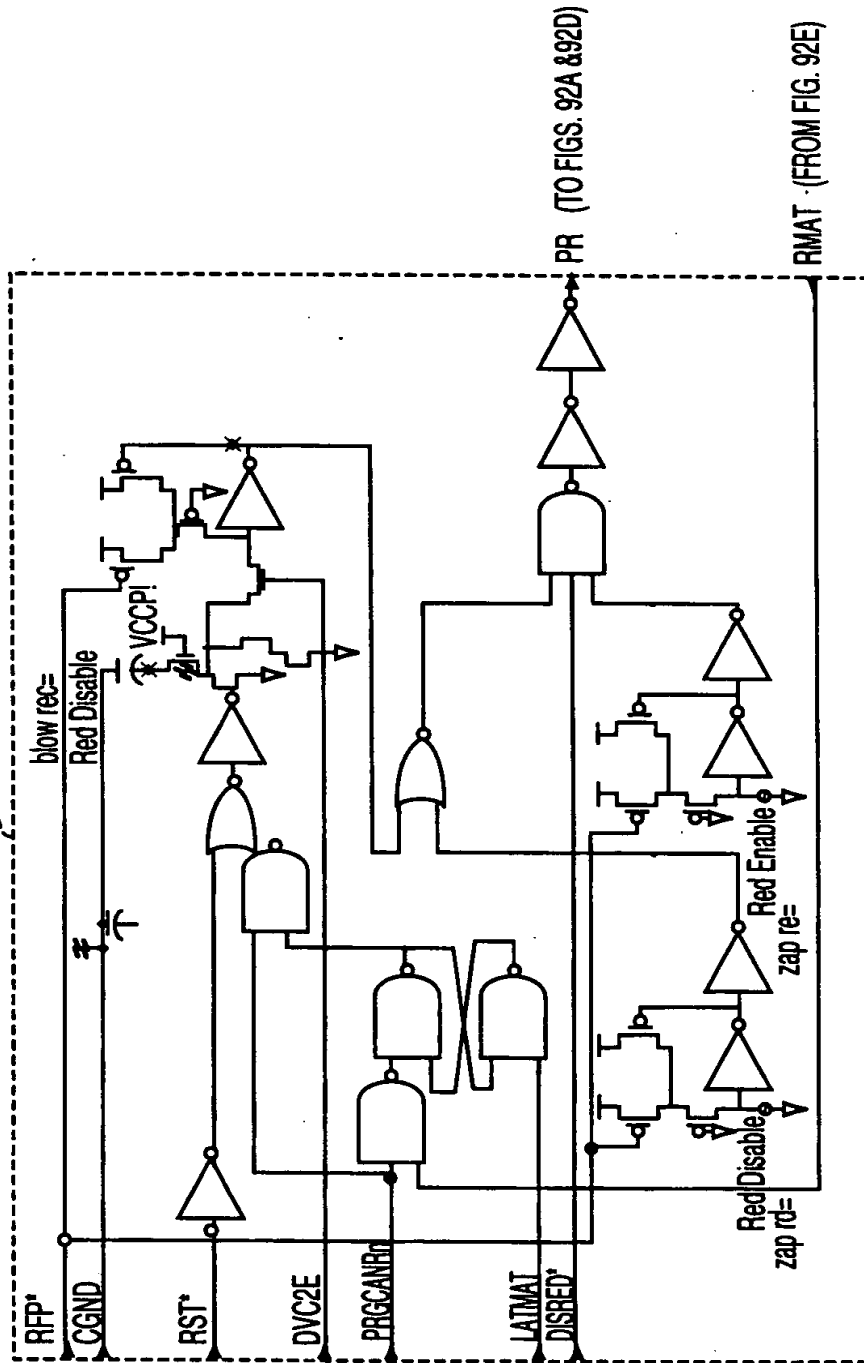


FIG. 92B

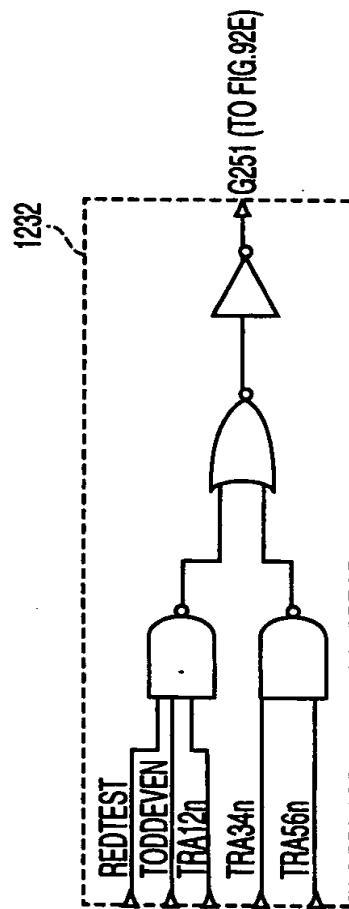


FIG. 92C

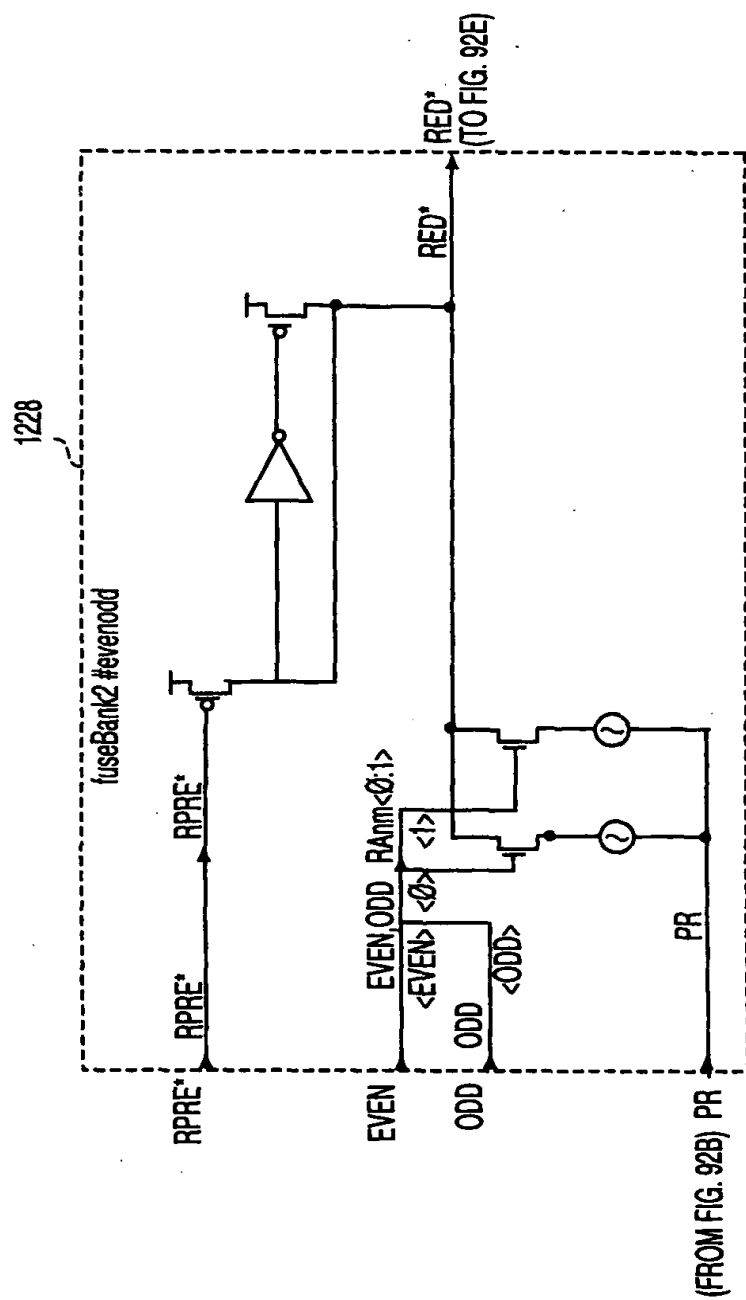


FIG. 92D

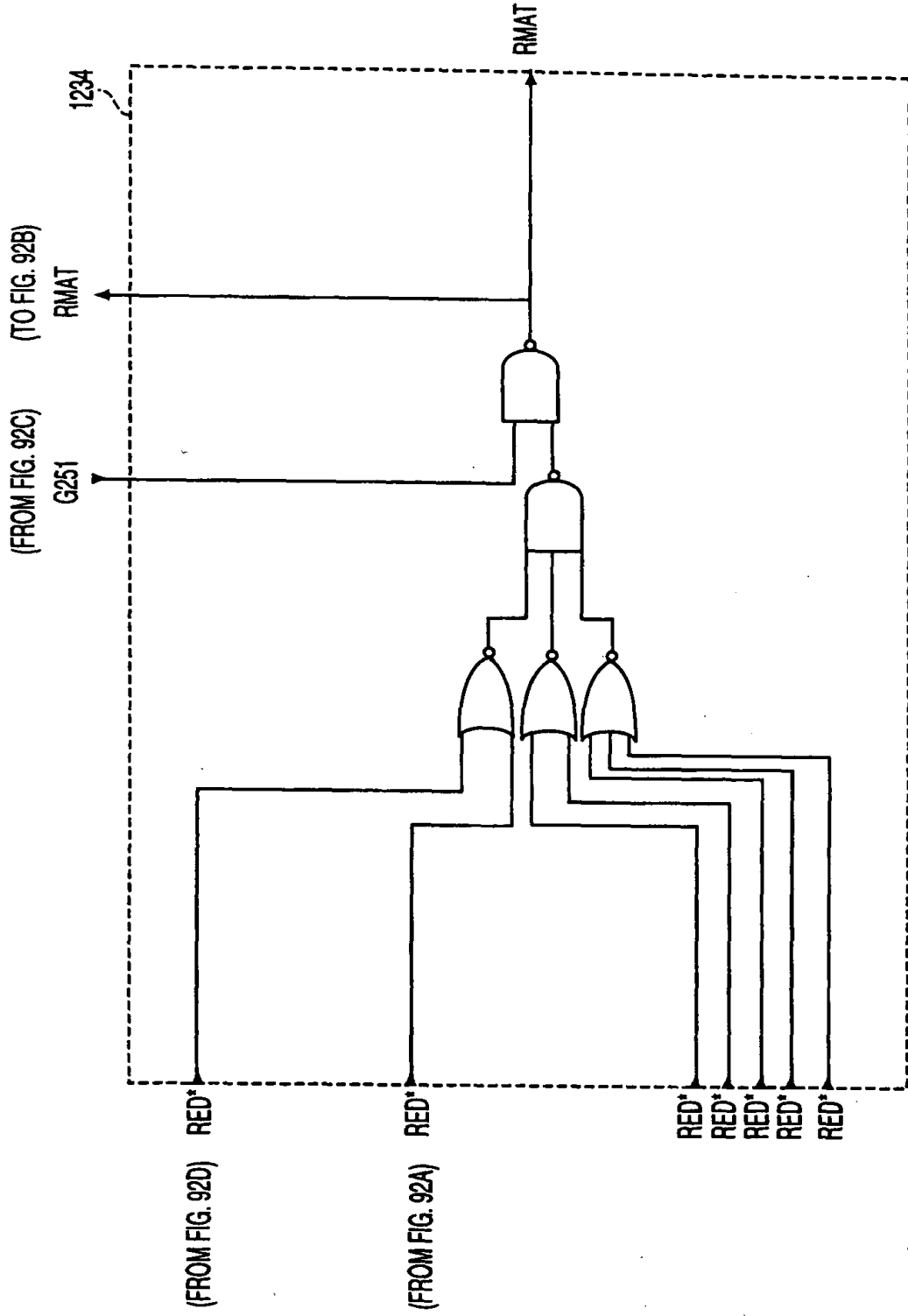
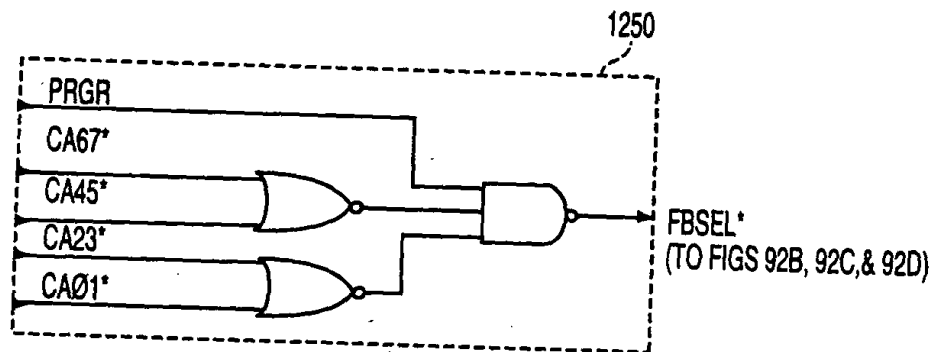


FIG. 92E



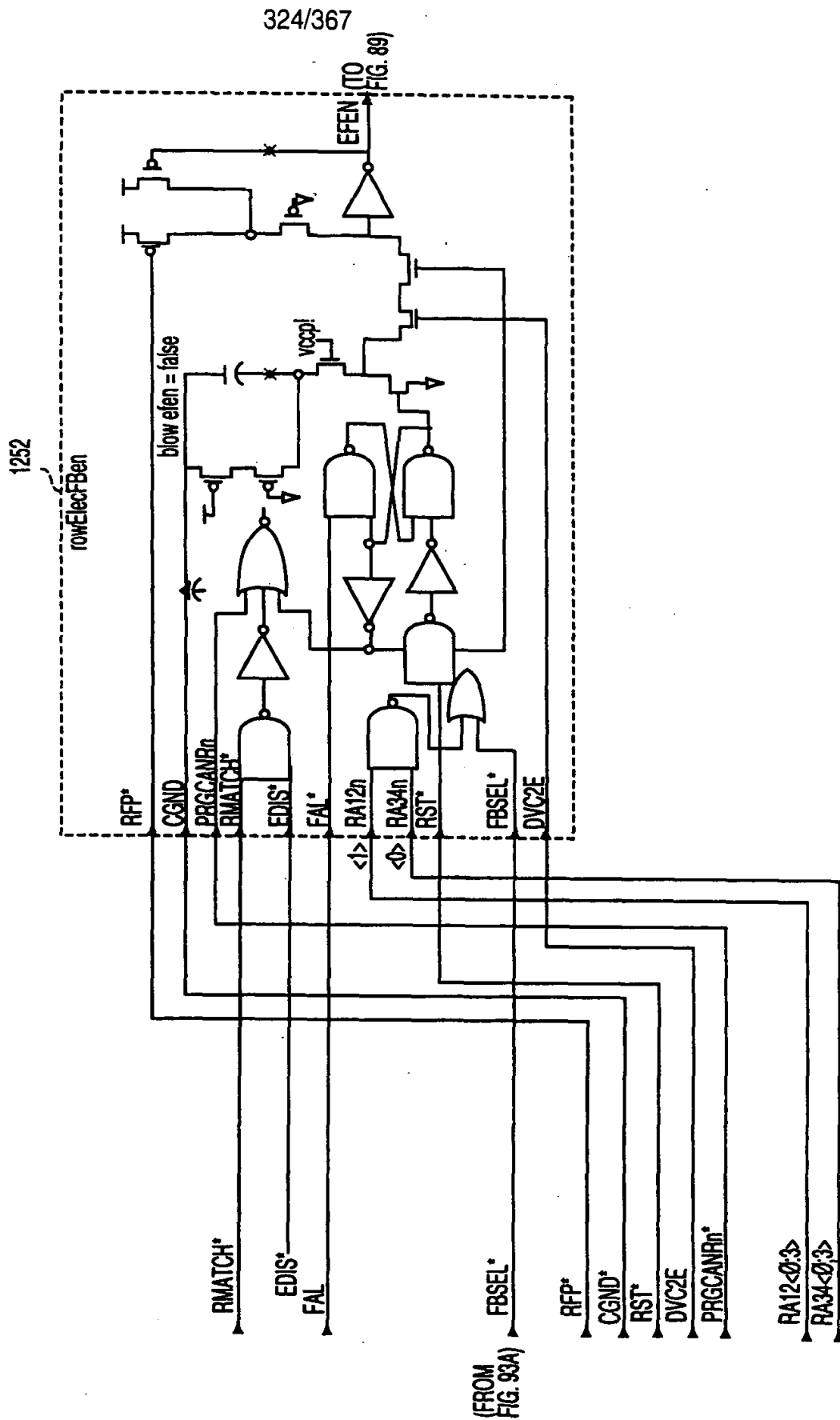


FIG. 93B

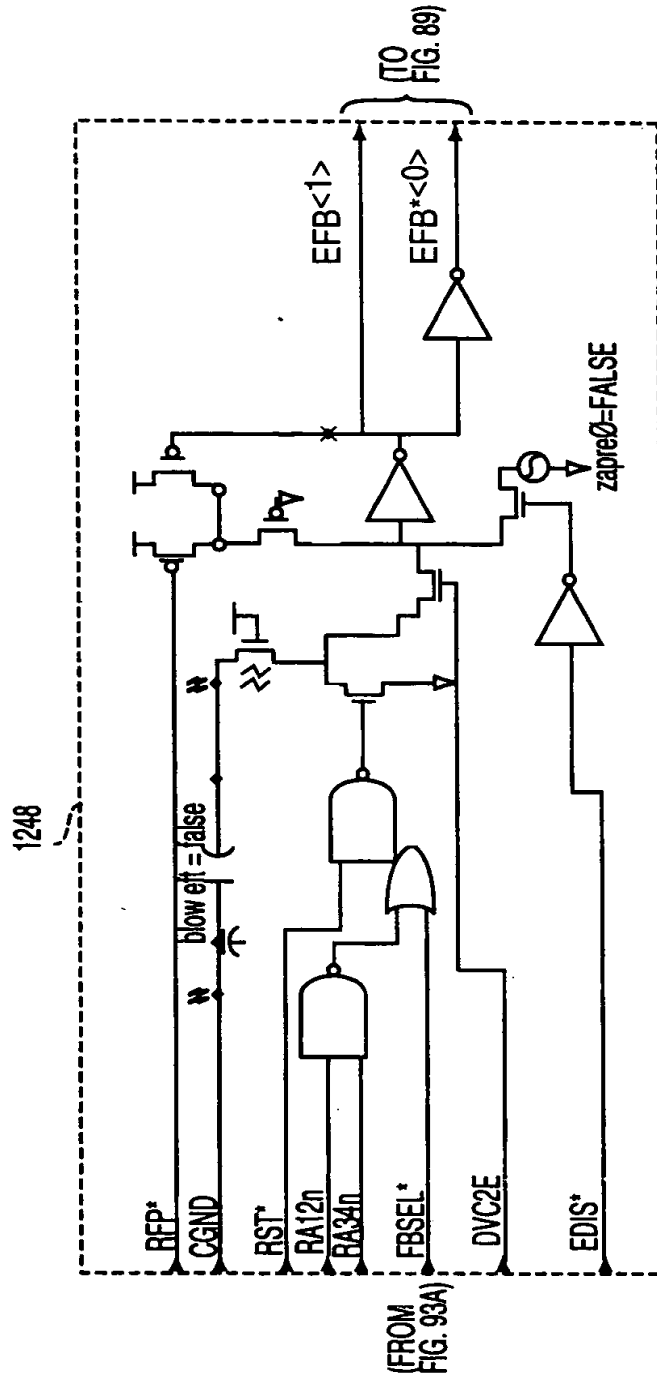
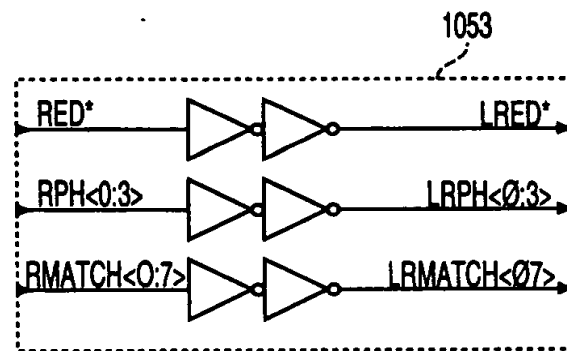


FIG. 93C



FIG. 93D

**FIG. 94**

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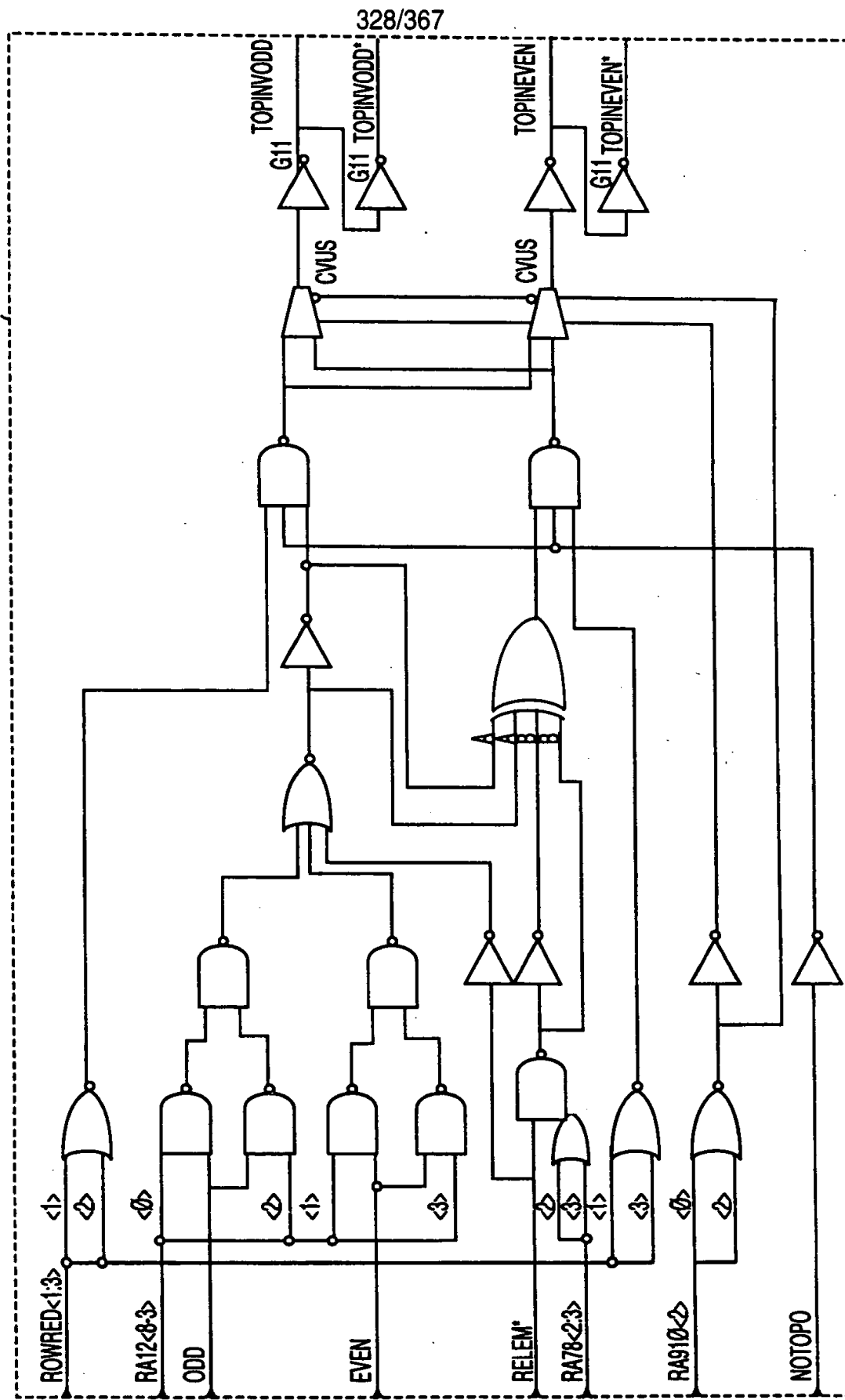


FIG. 95

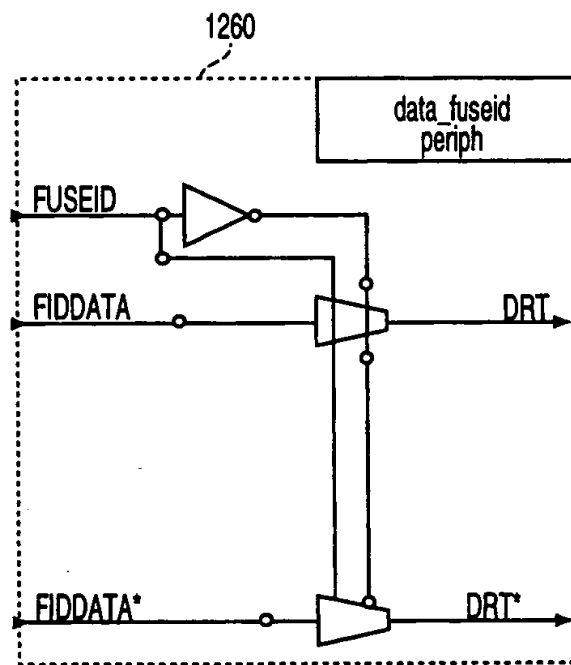
**FIG. 96**



FIG. 97-1 | FIG. 97-2

FIG. 97-1

FIG. 97-2

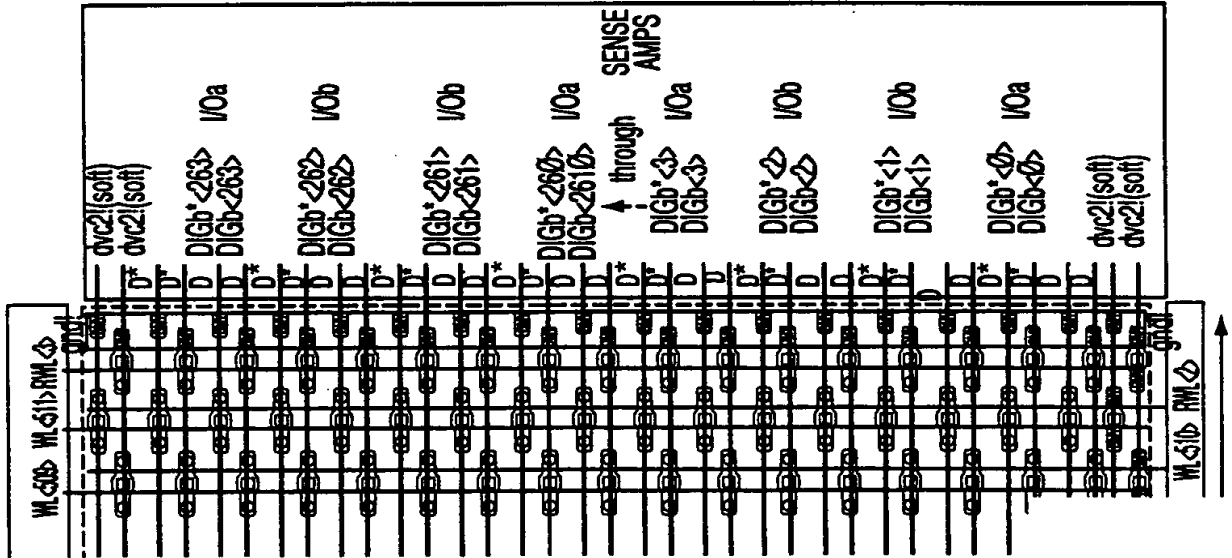
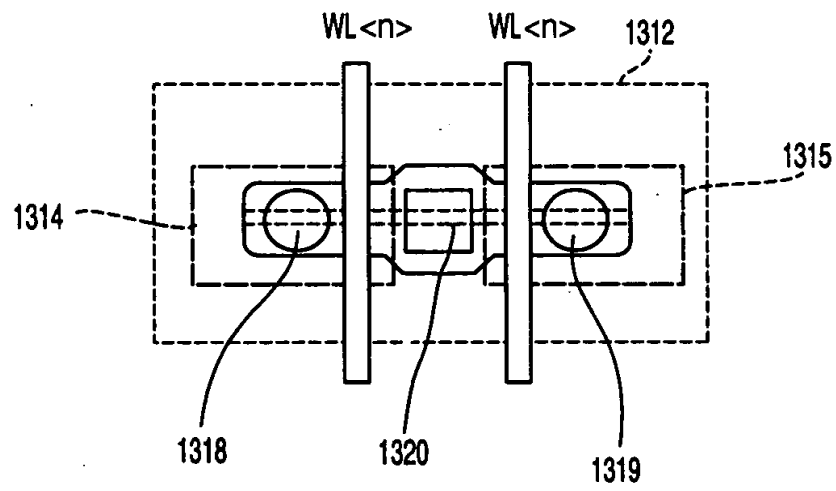


FIG. 97-1 FIG. 97-2

FIG. 97-2

**FIG. 98**

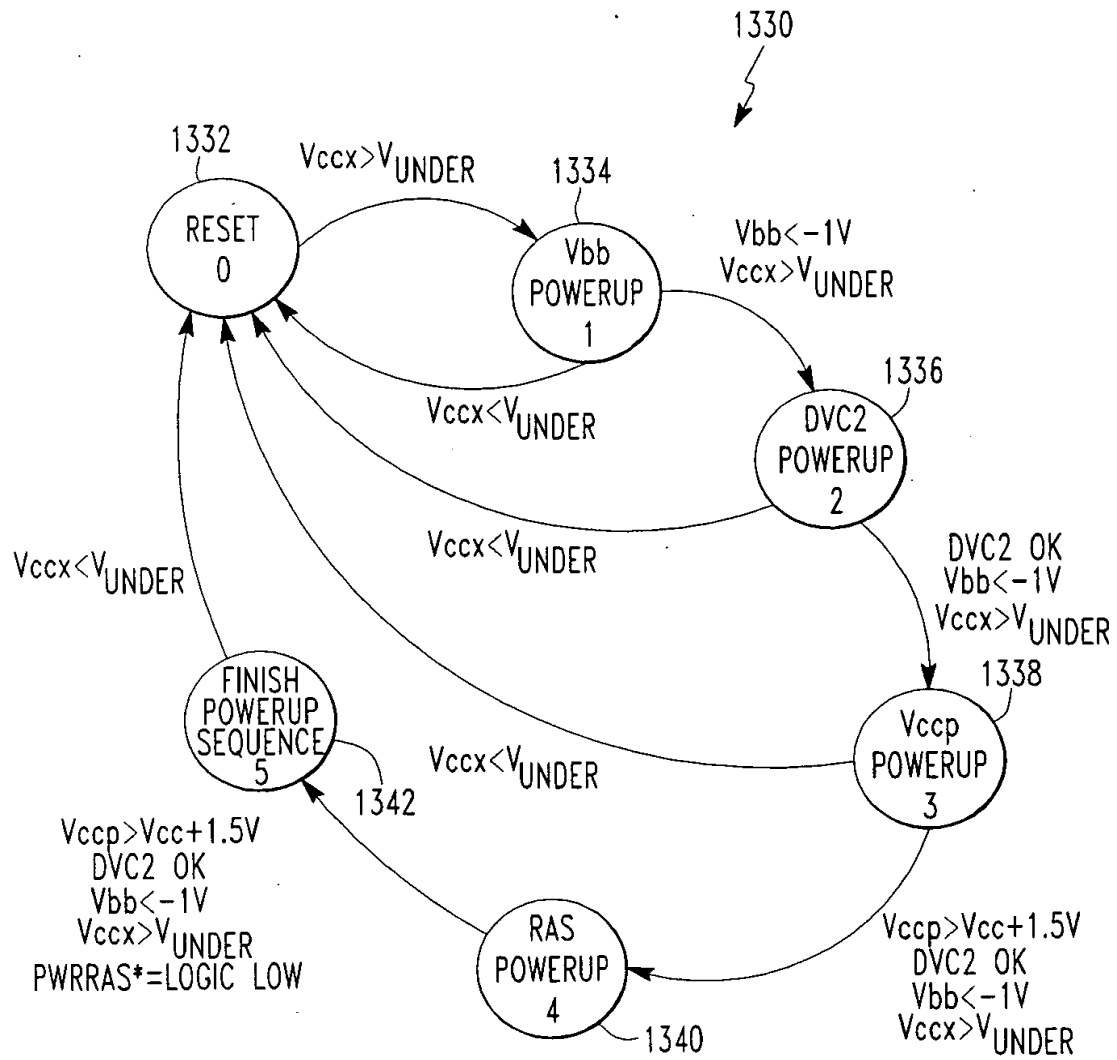


FIG. 99

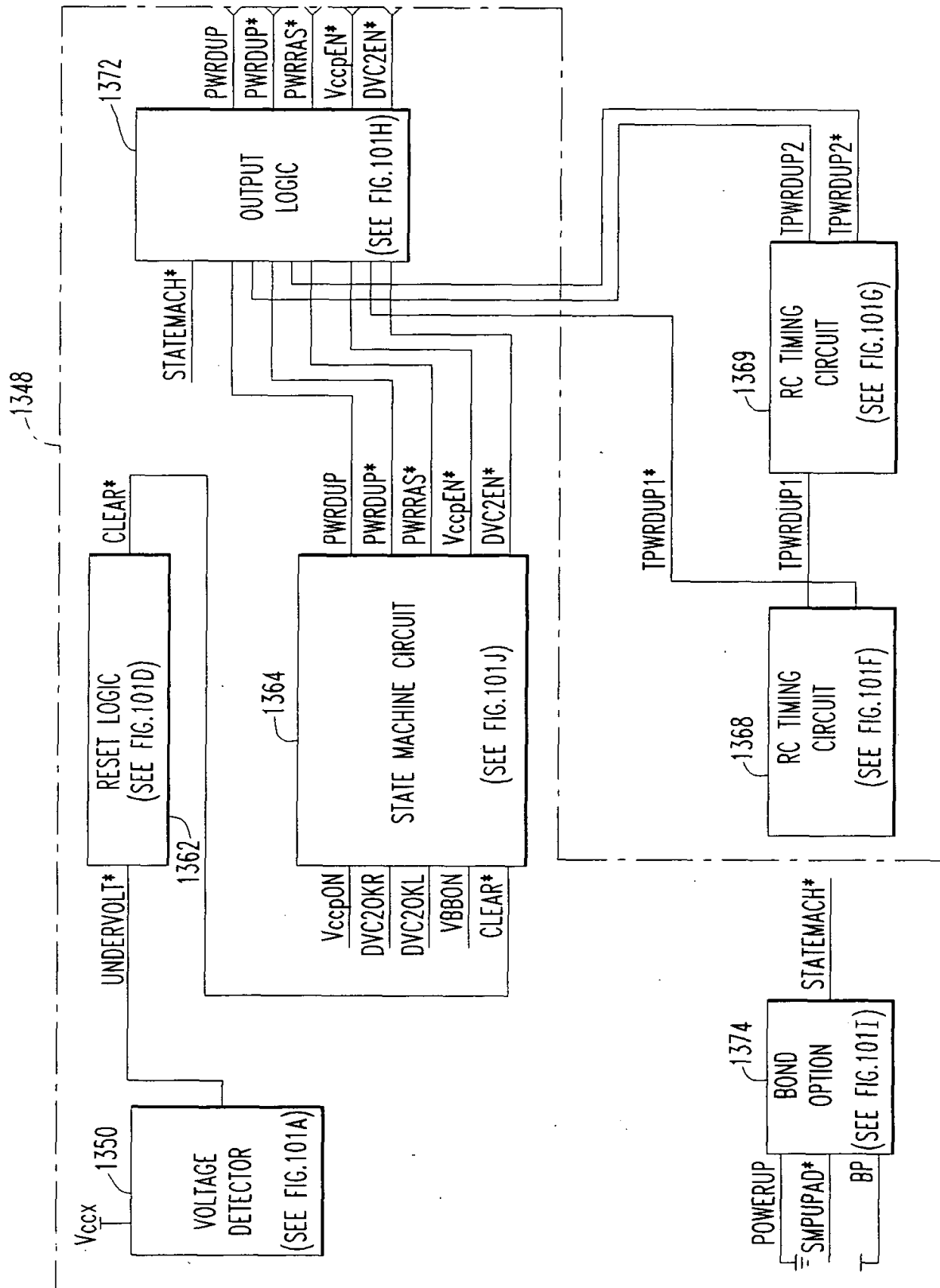


FIG. 100

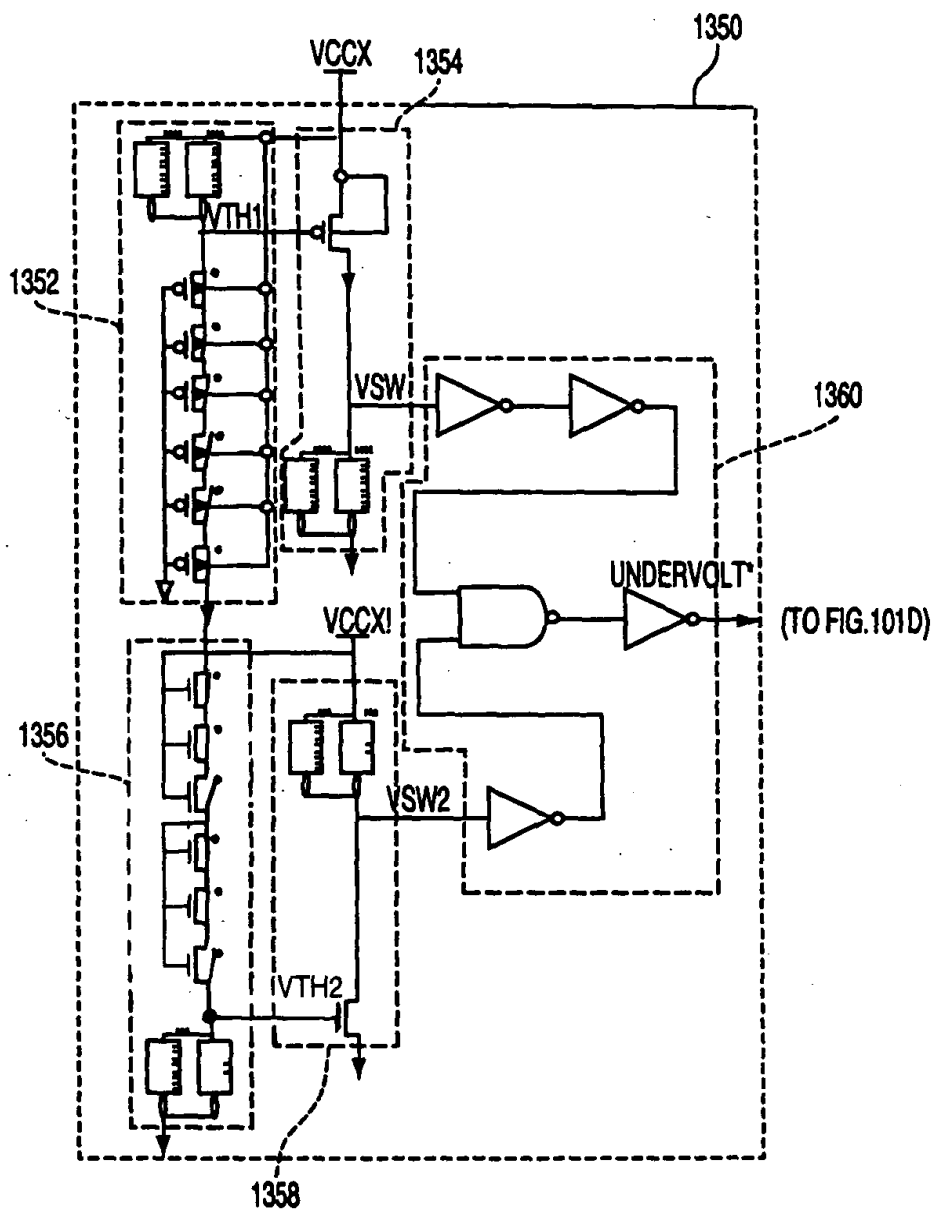
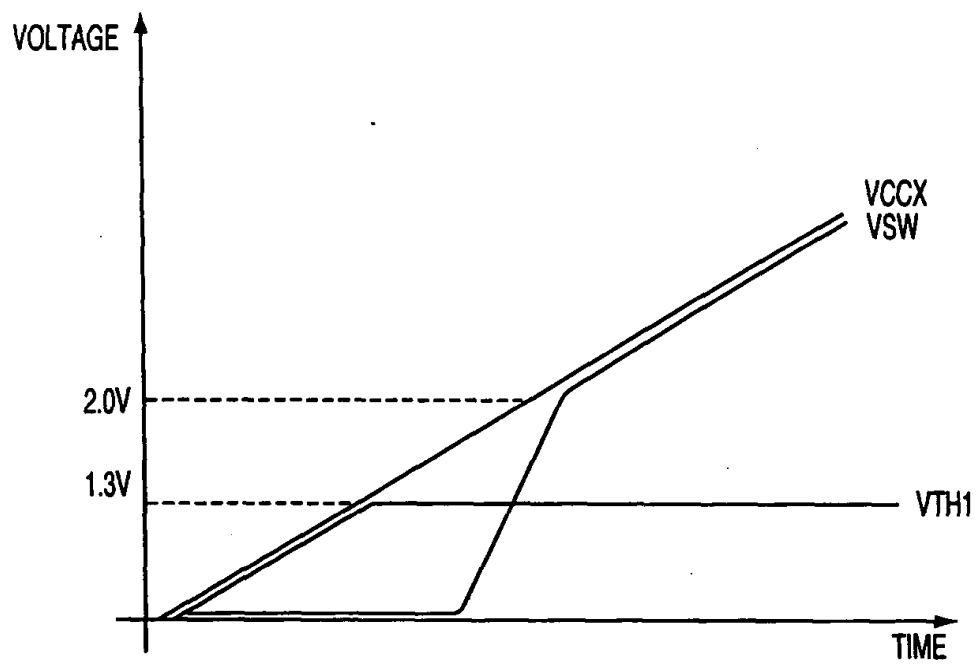
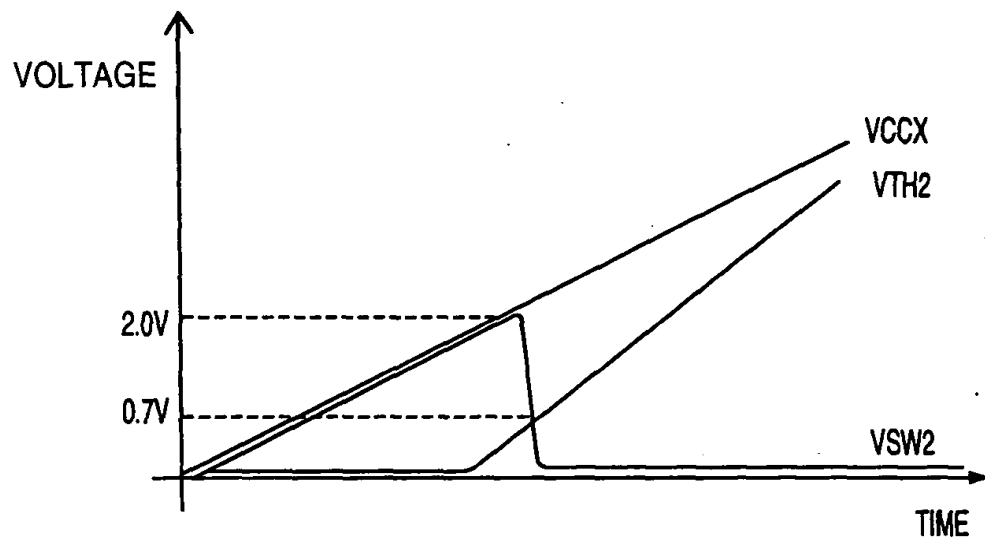


FIG. 101A

**FIG. 101B**

**FIG. 101C**

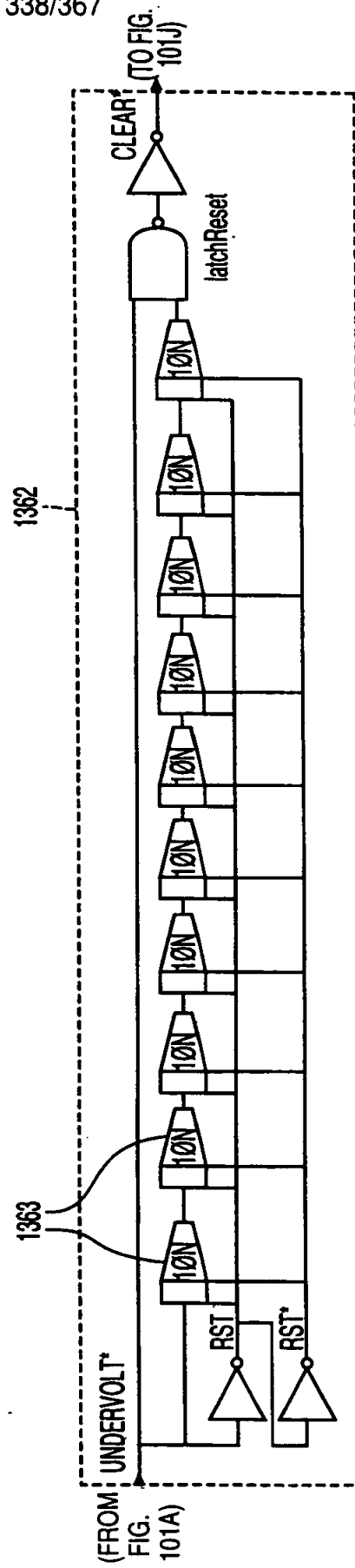


FIG. 101D

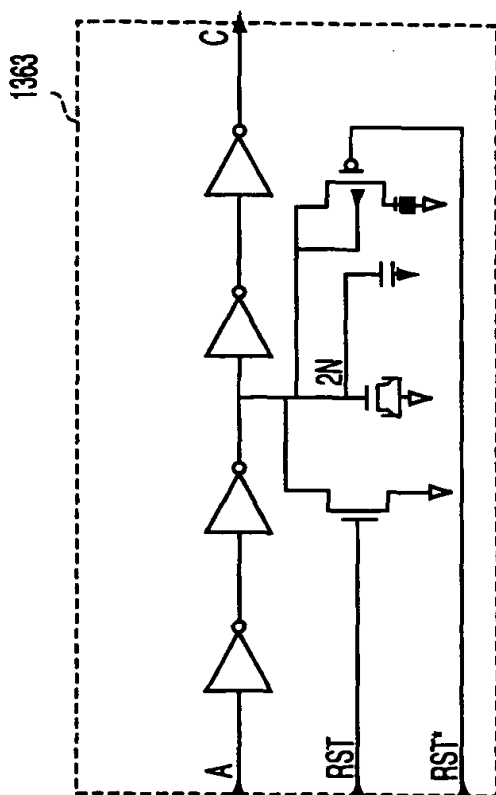


FIG. 101E

FIG. 101F

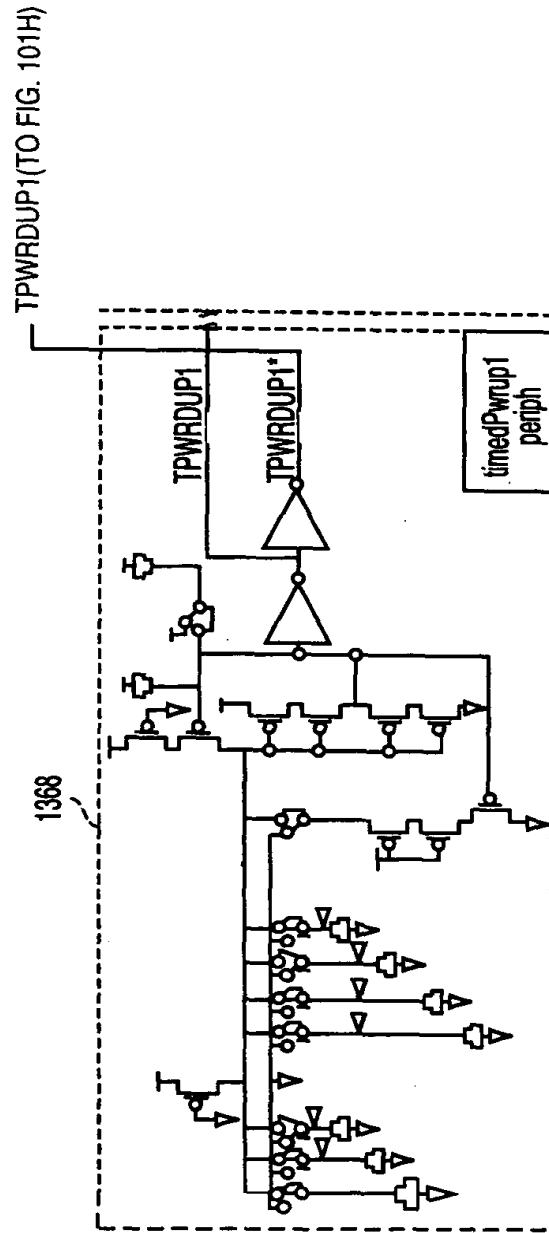


FIG. 101F

FIG. 101G

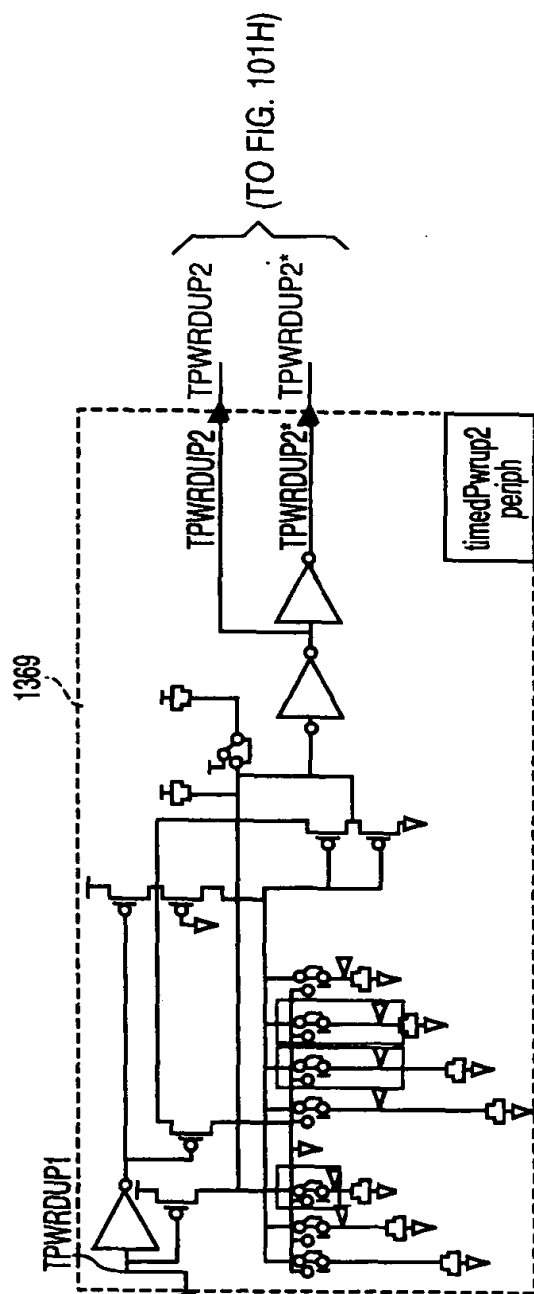


FIG. 101G

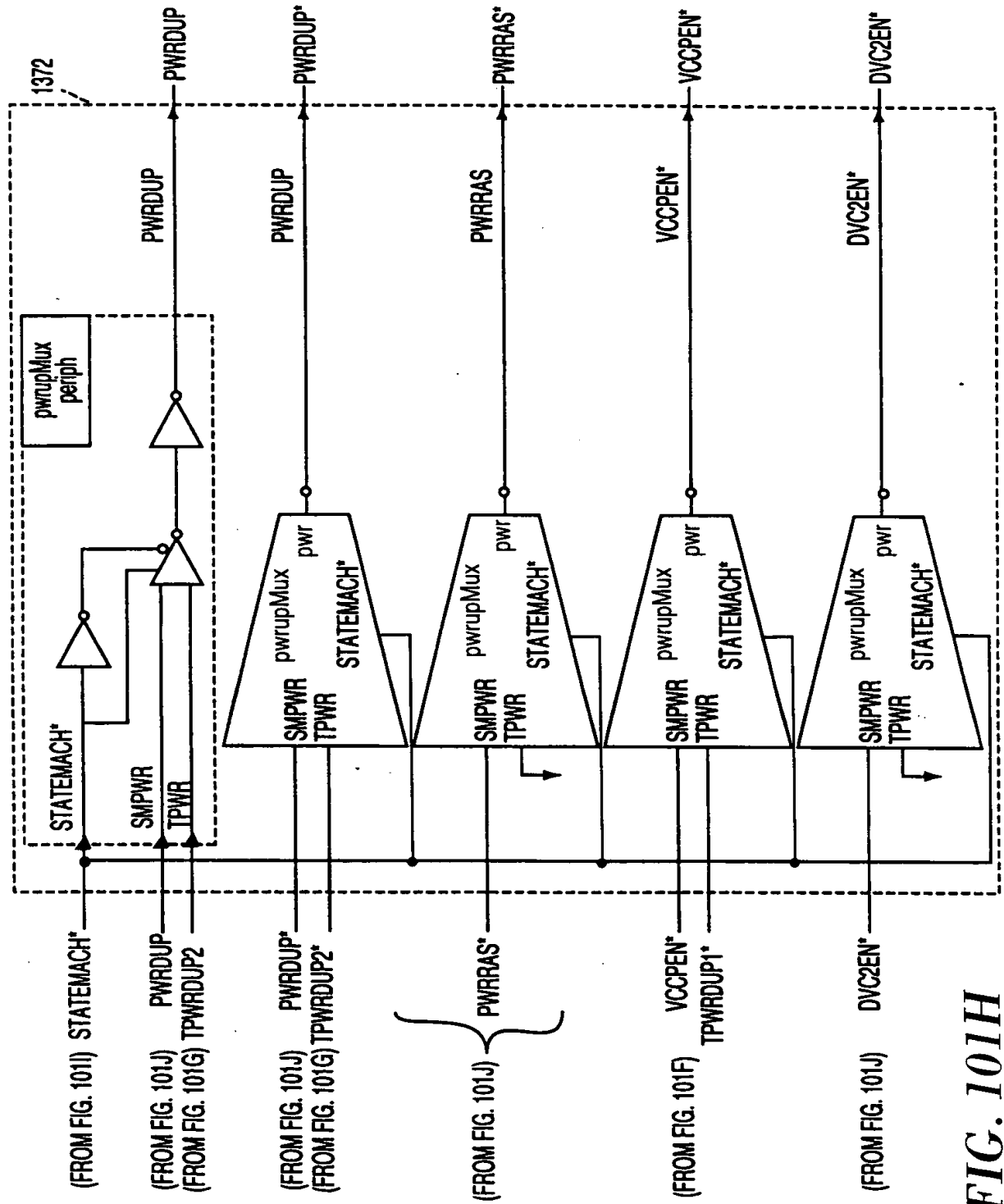


FIG. 101H

FIG. 1011

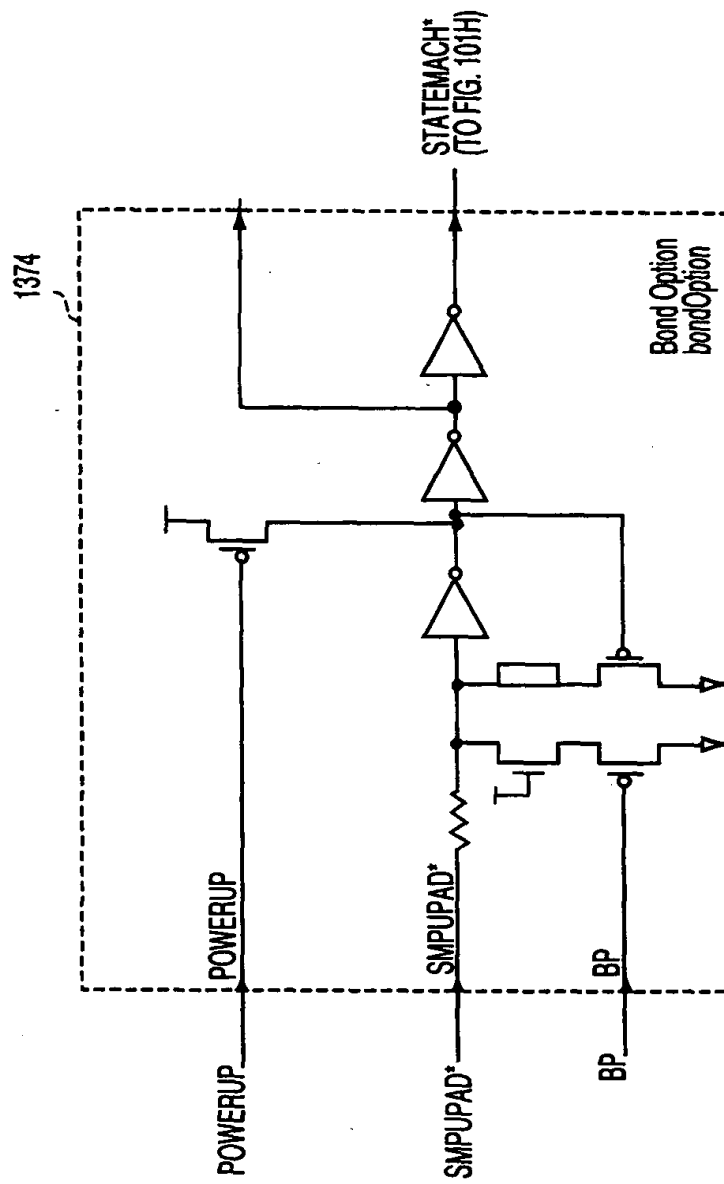


FIG. 1011

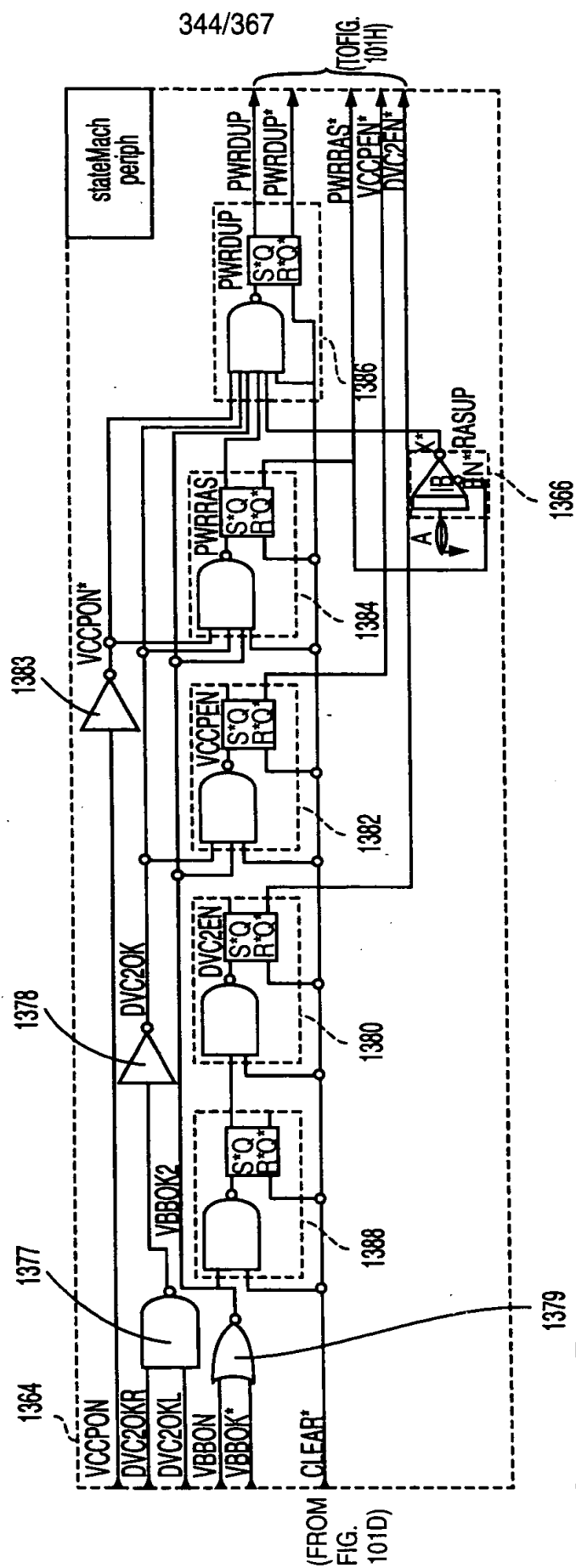
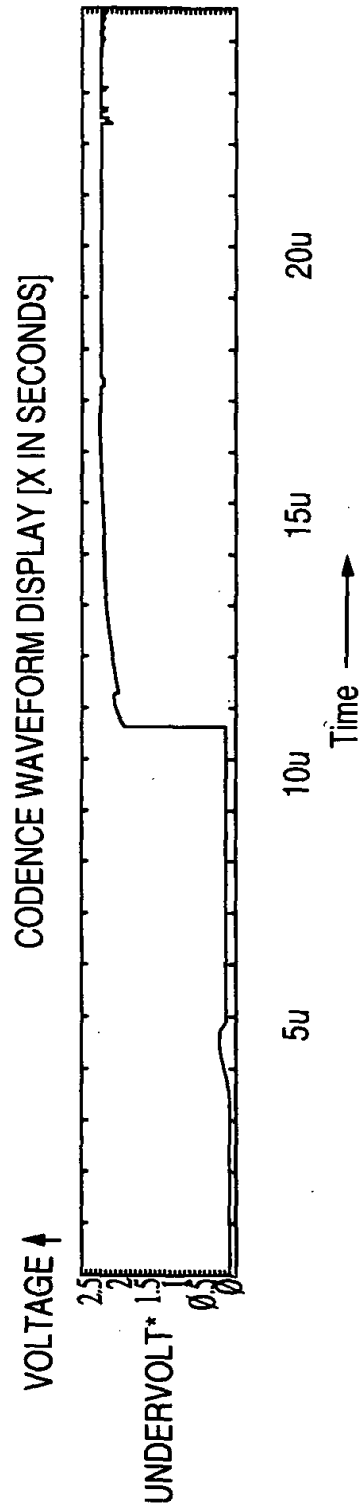
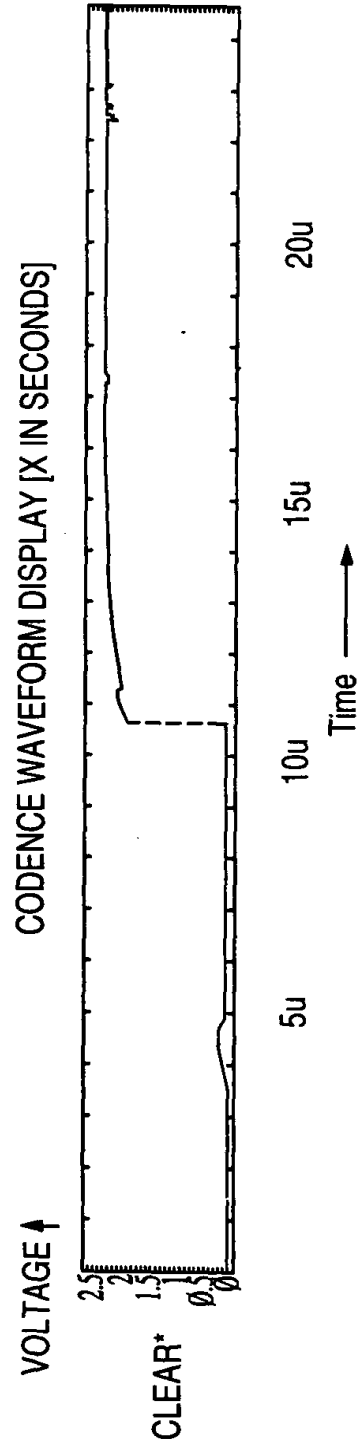


FIG. 101J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

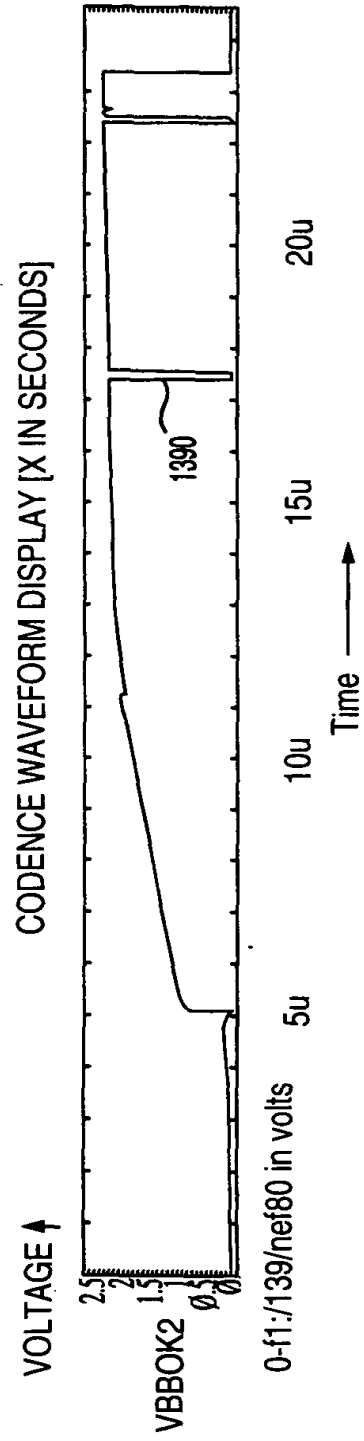
FIG. 102B



NOTE THAT PWRRAS* WAITED FOR DVC20KR

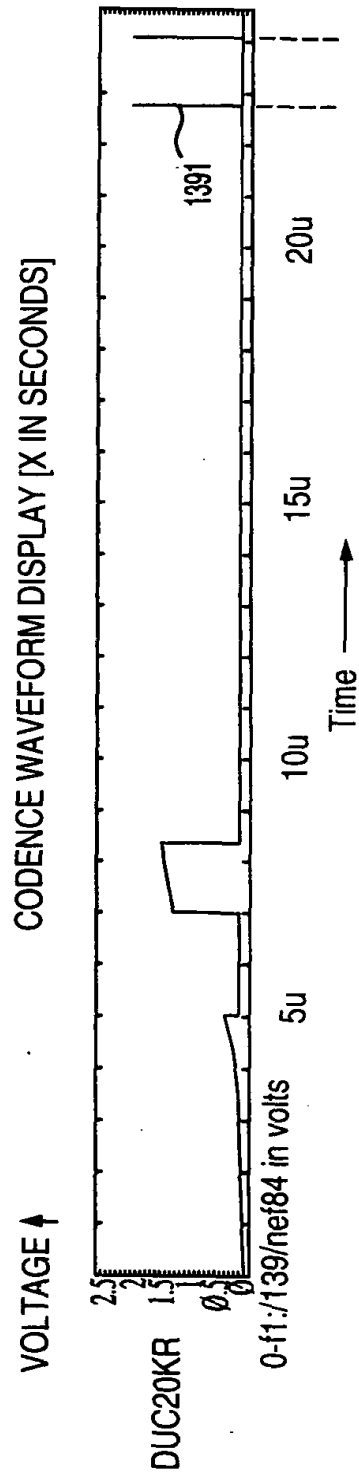
FIG. 102C

1.03000" 0.000000

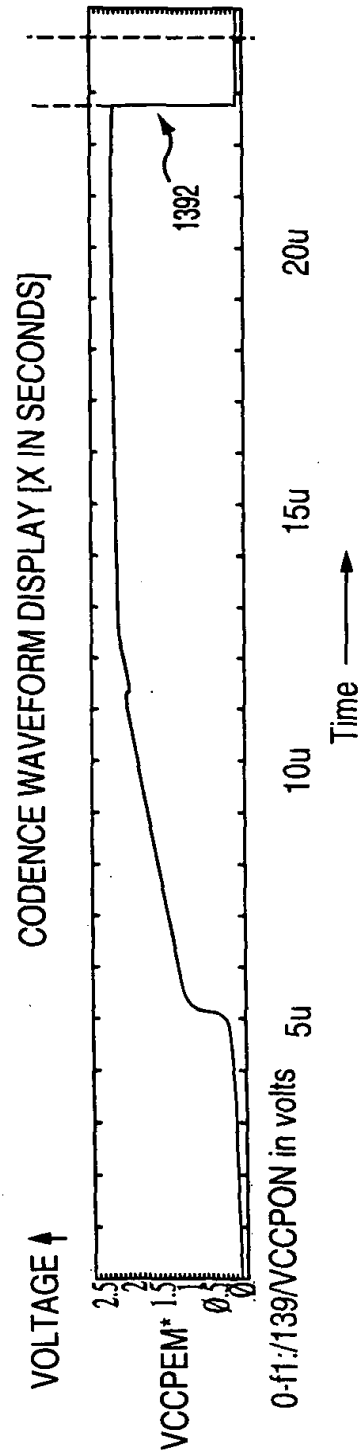


NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D

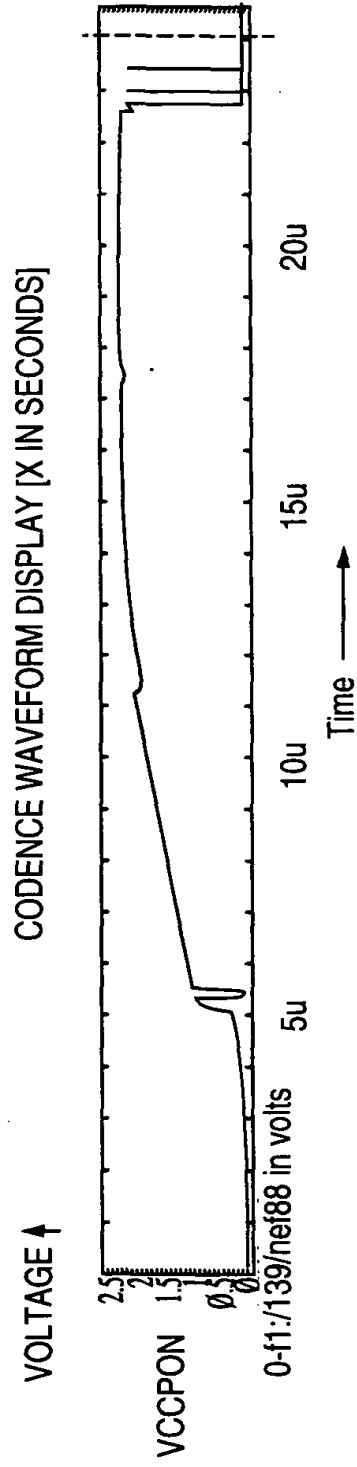


NOTE THAT PWRRAS* WAITED FOR DVC20KR



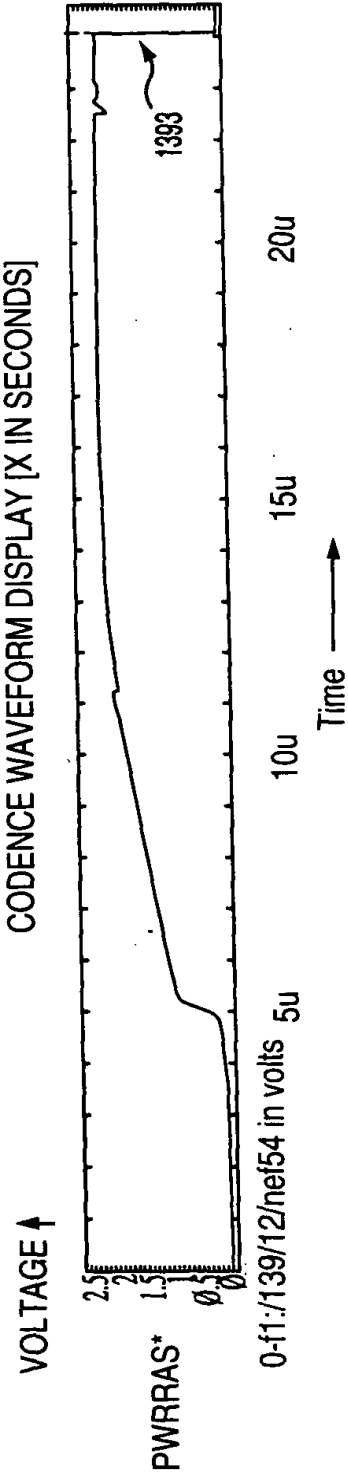
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



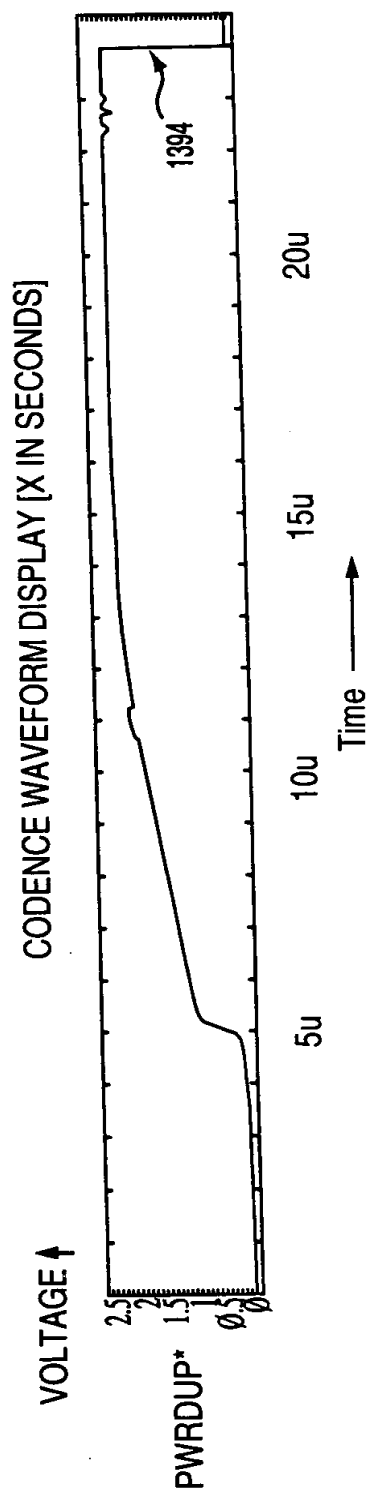
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102H



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102I



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

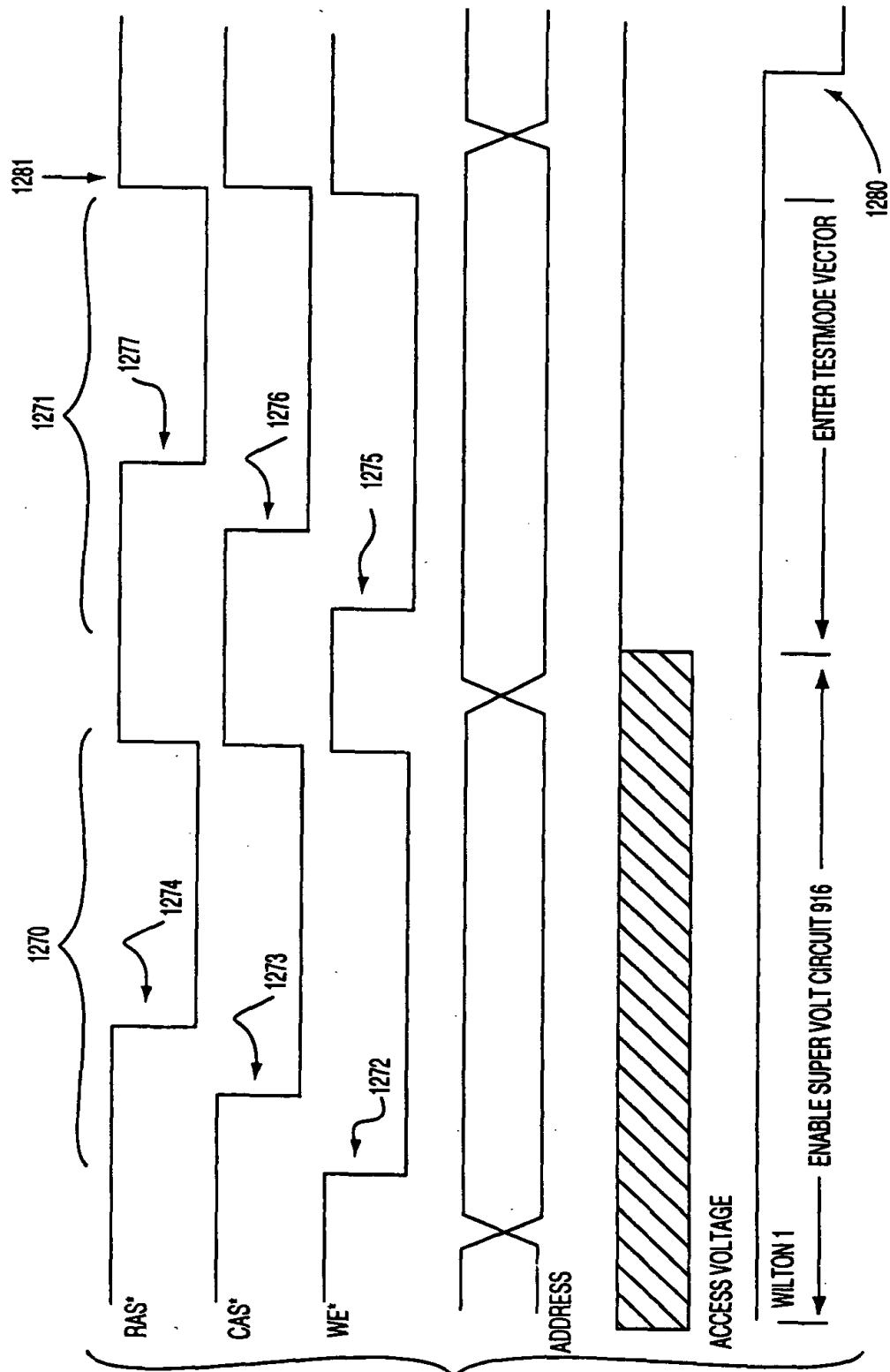


FIG.
103

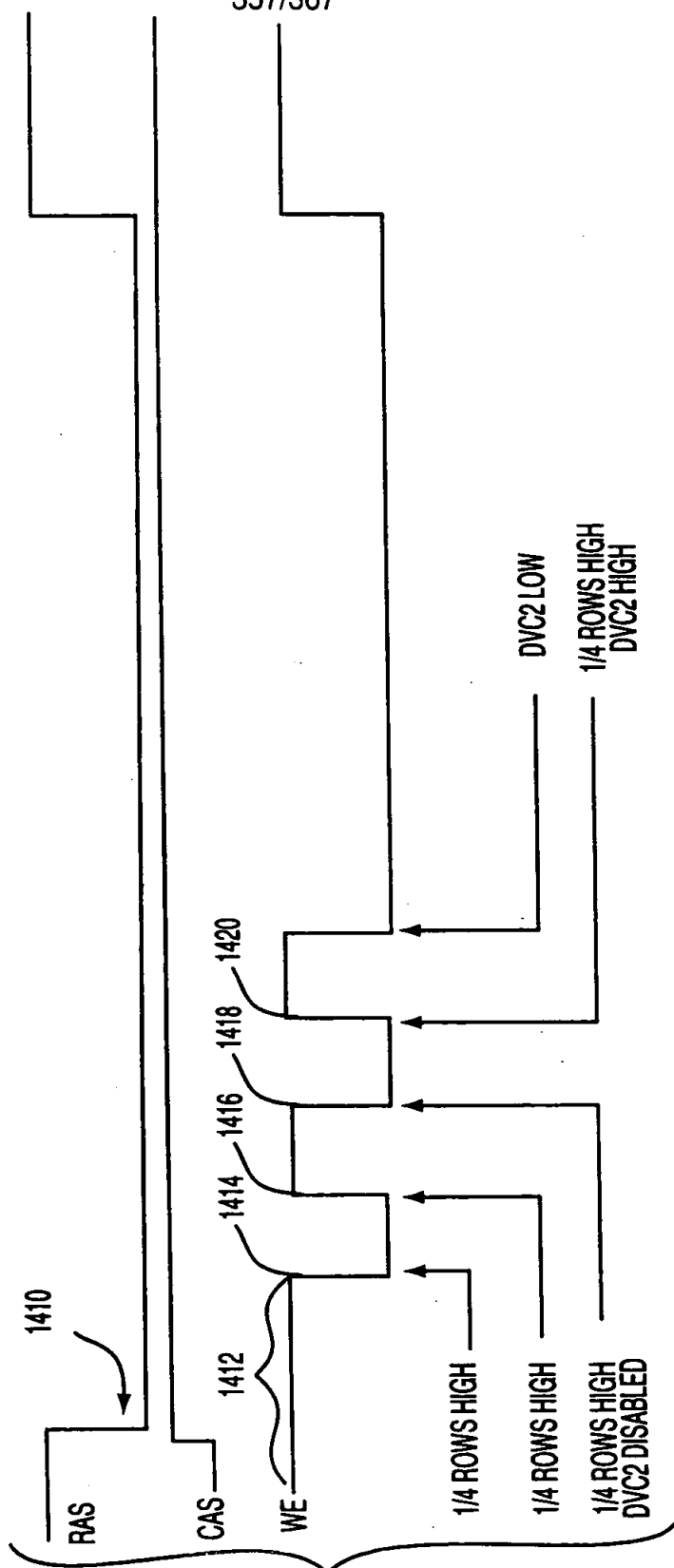
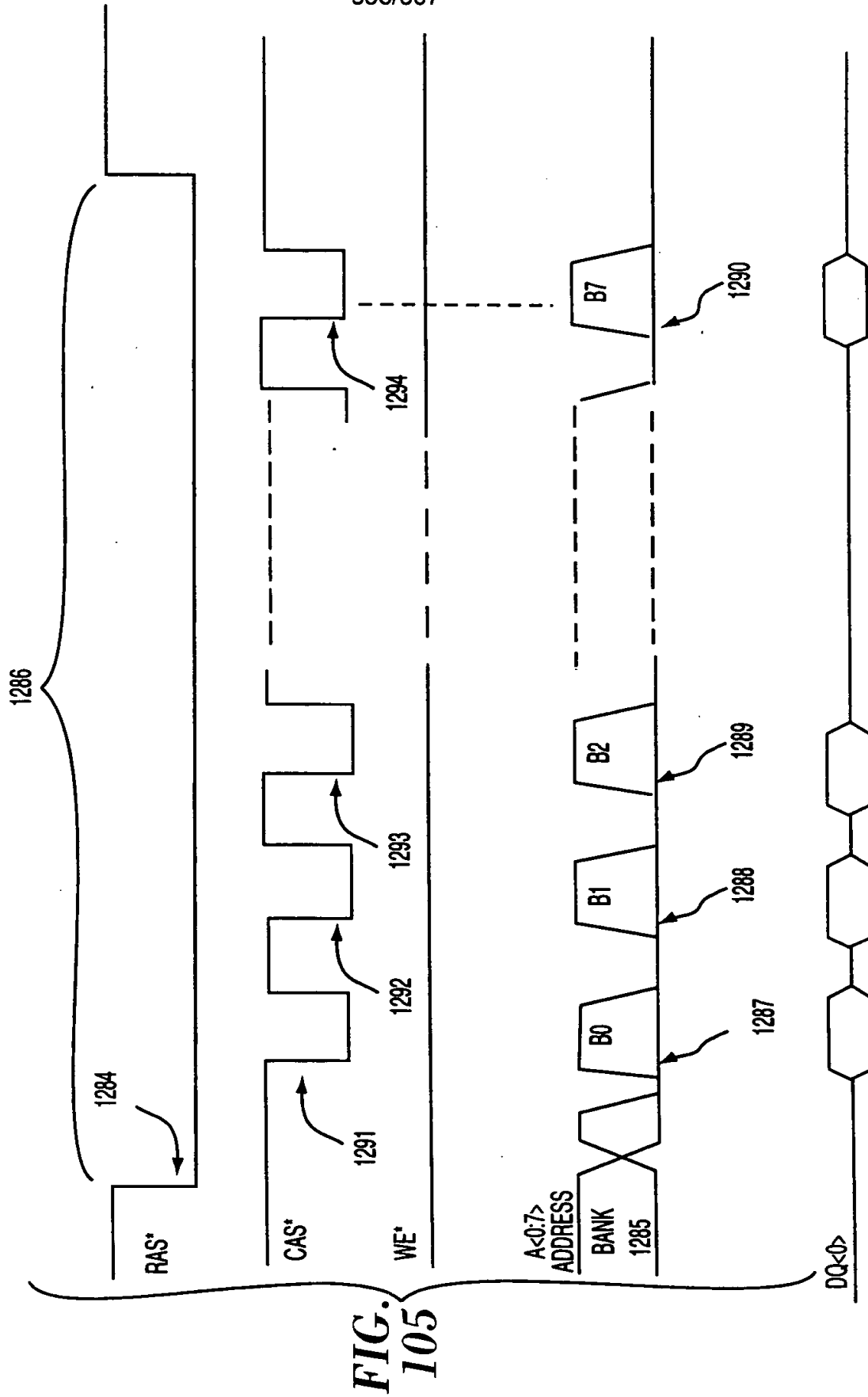


FIG.
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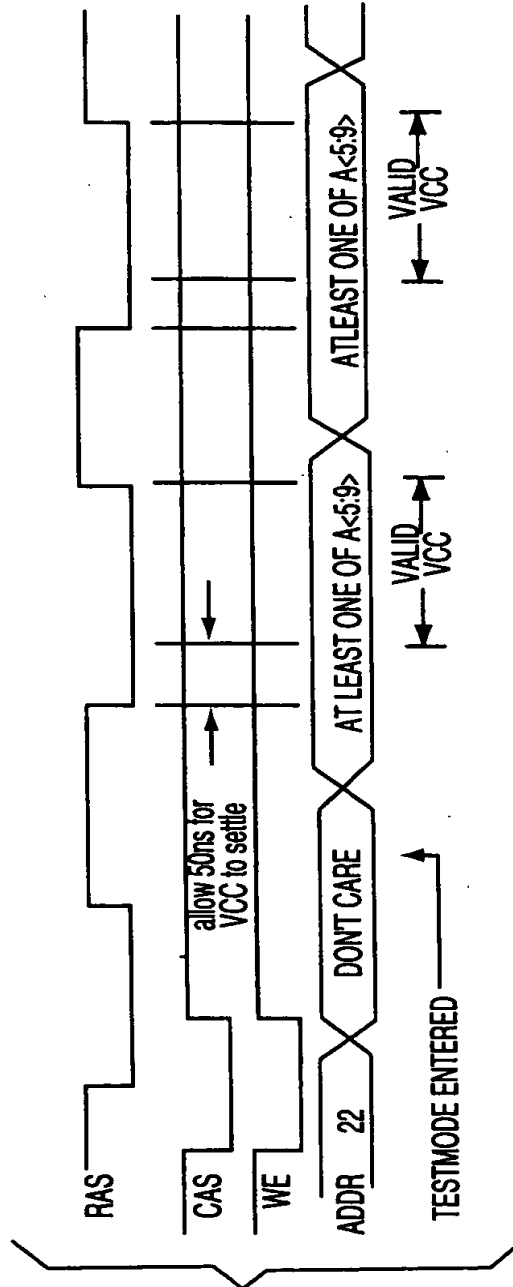


FIG. 106

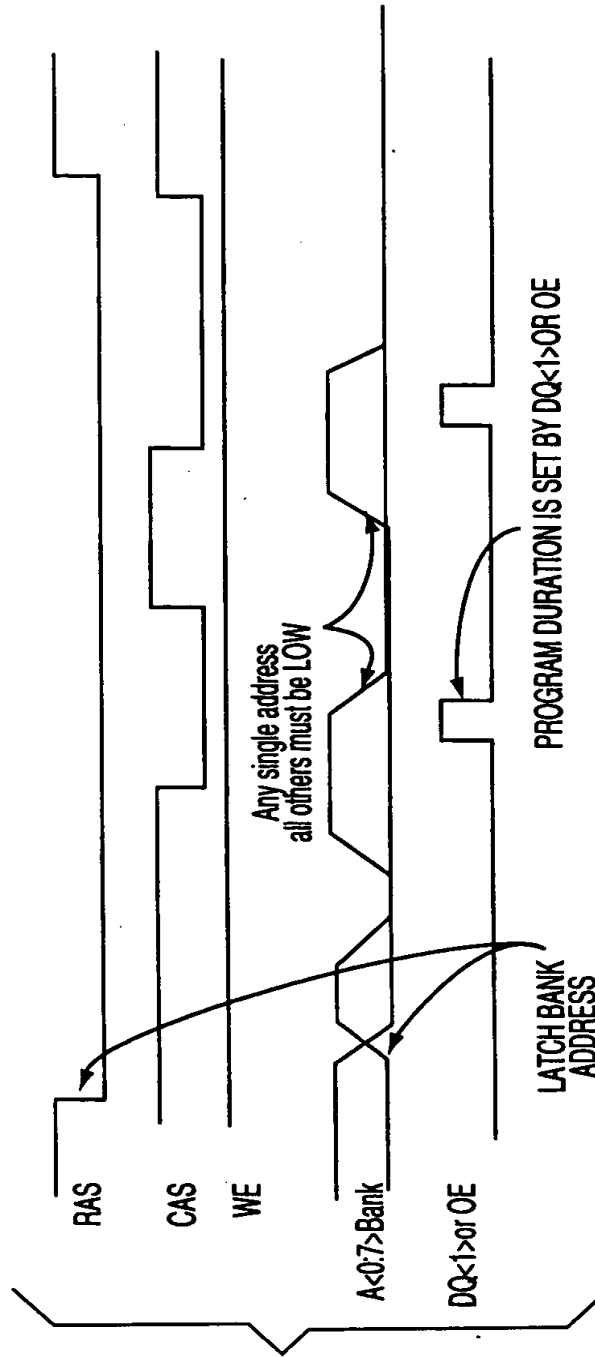


FIG. 107

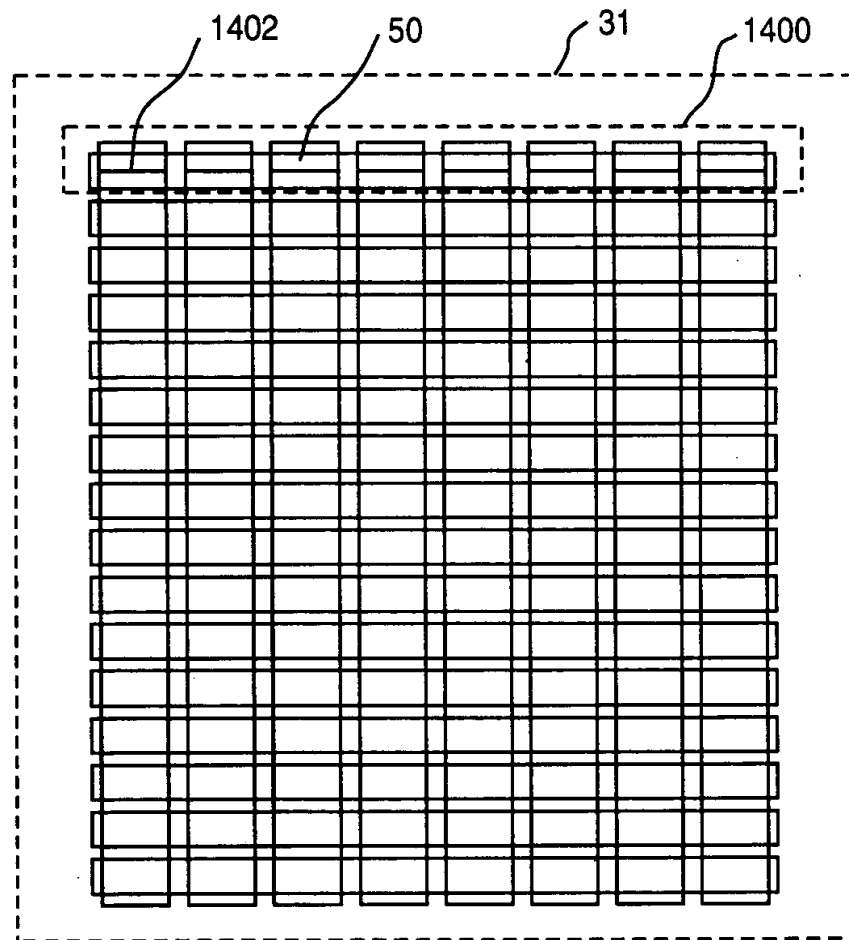
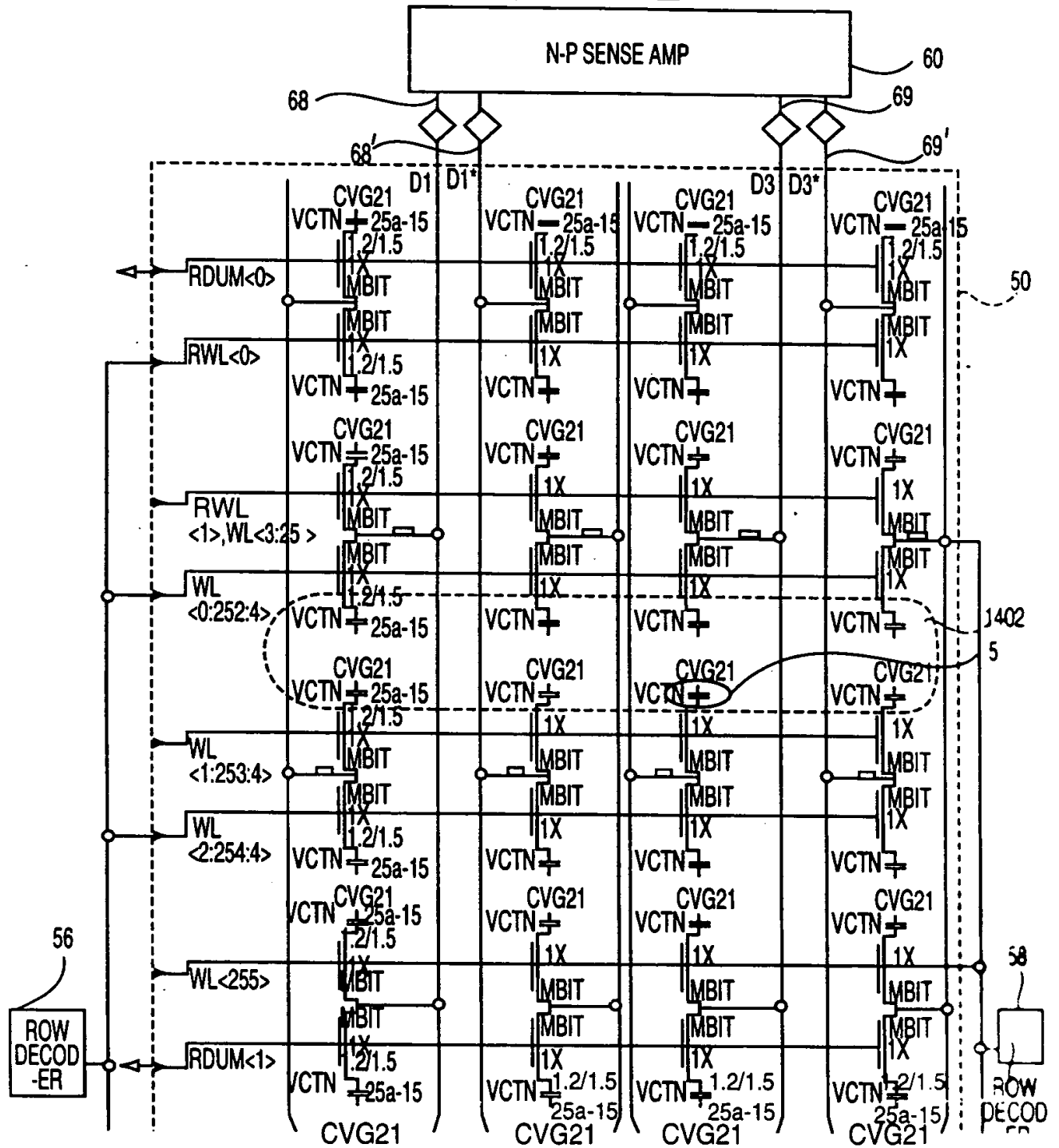
**FIG. 108**

FIG. 109-1

FIG. 109-1

FIG. 109-2



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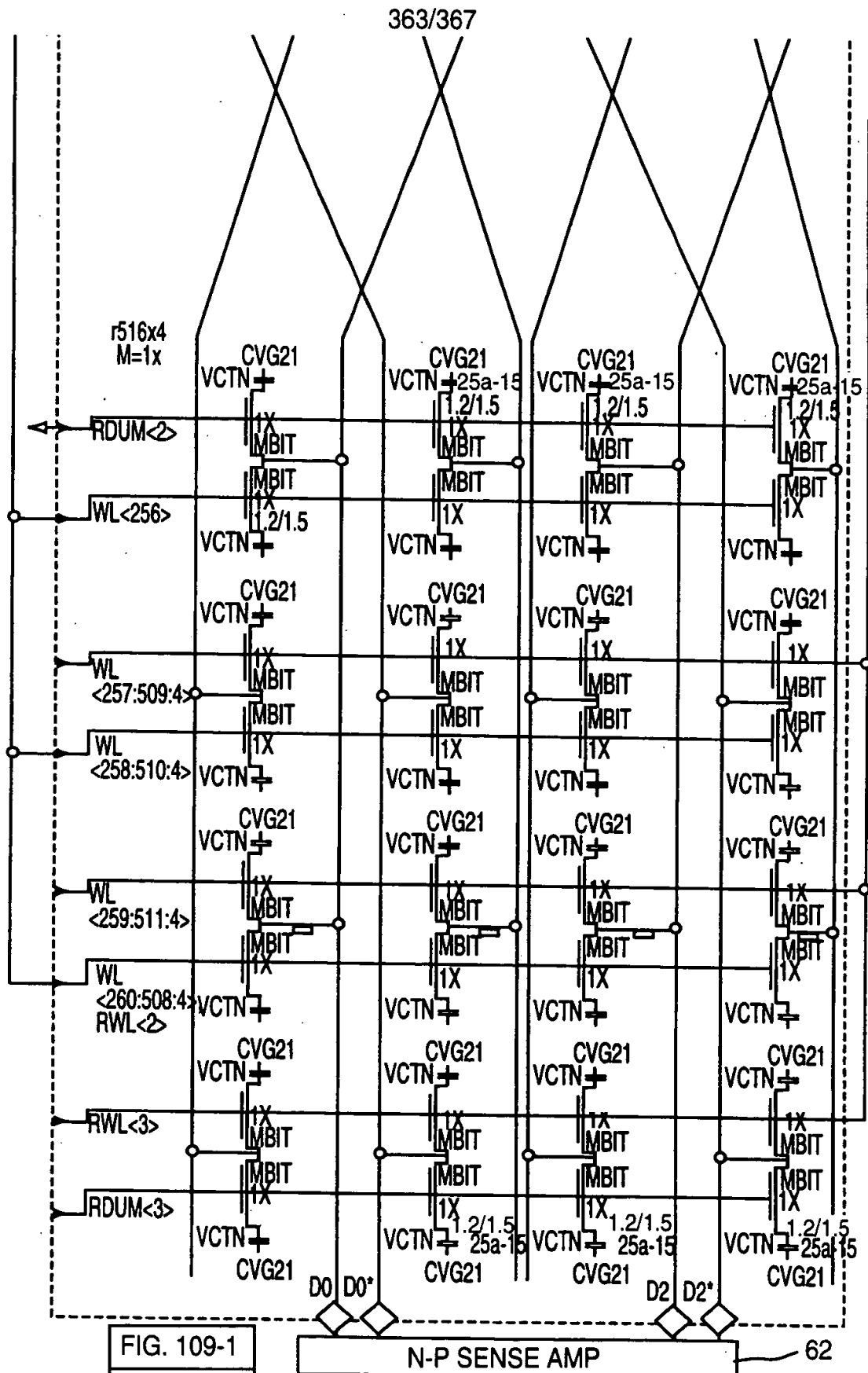


FIG. 109-1

FIG. 109-2

FIG. 109-2

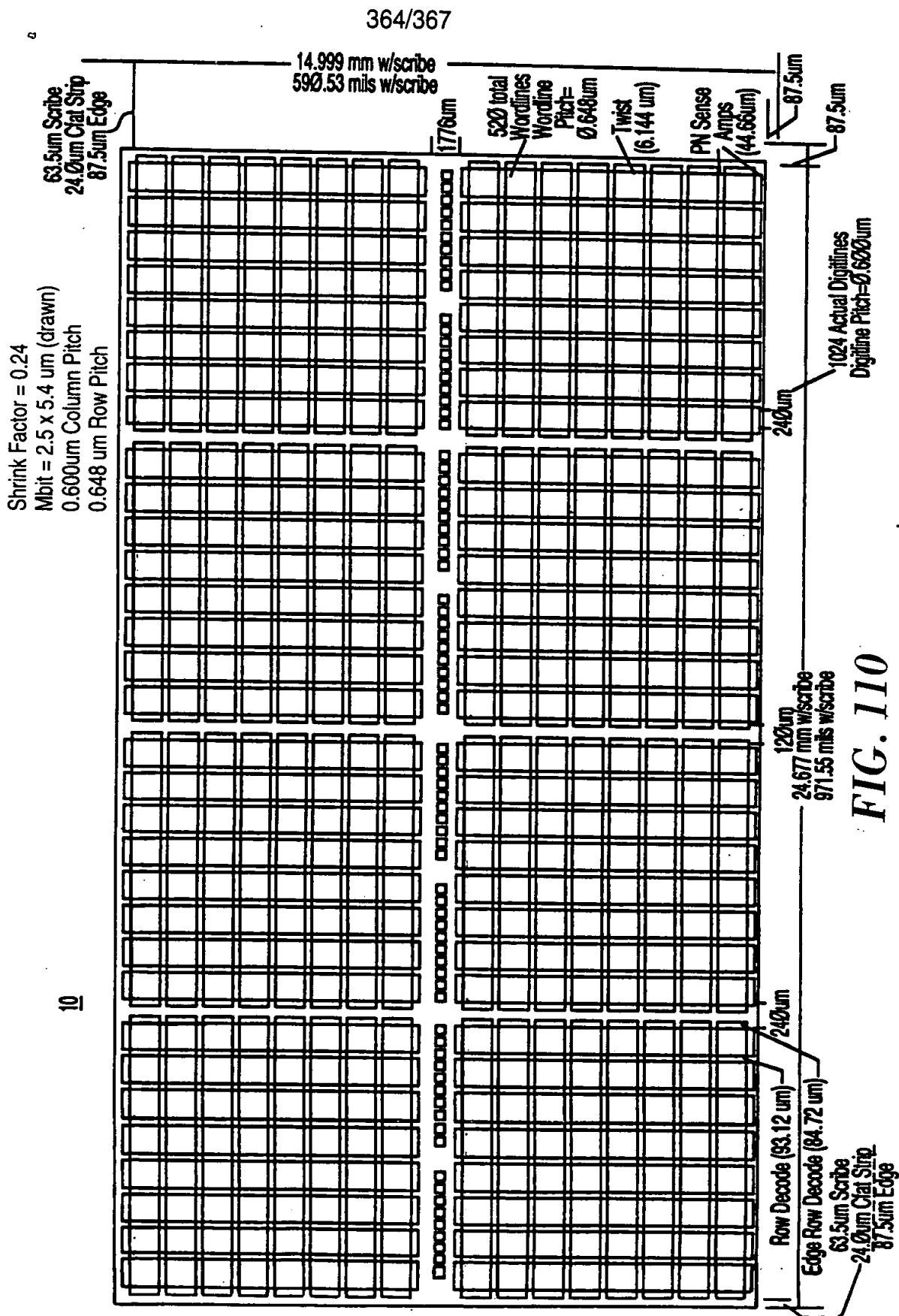


FIG. 110

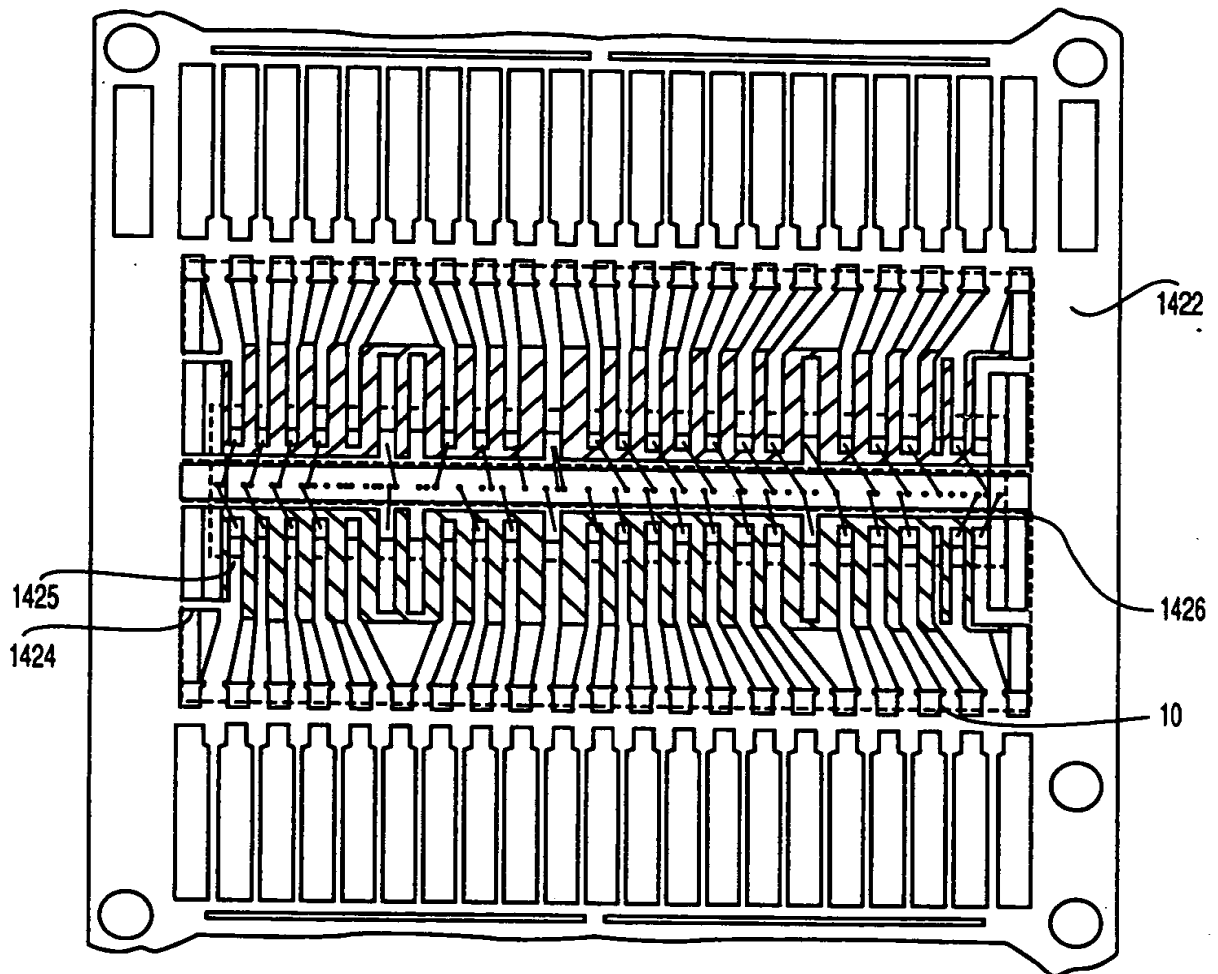
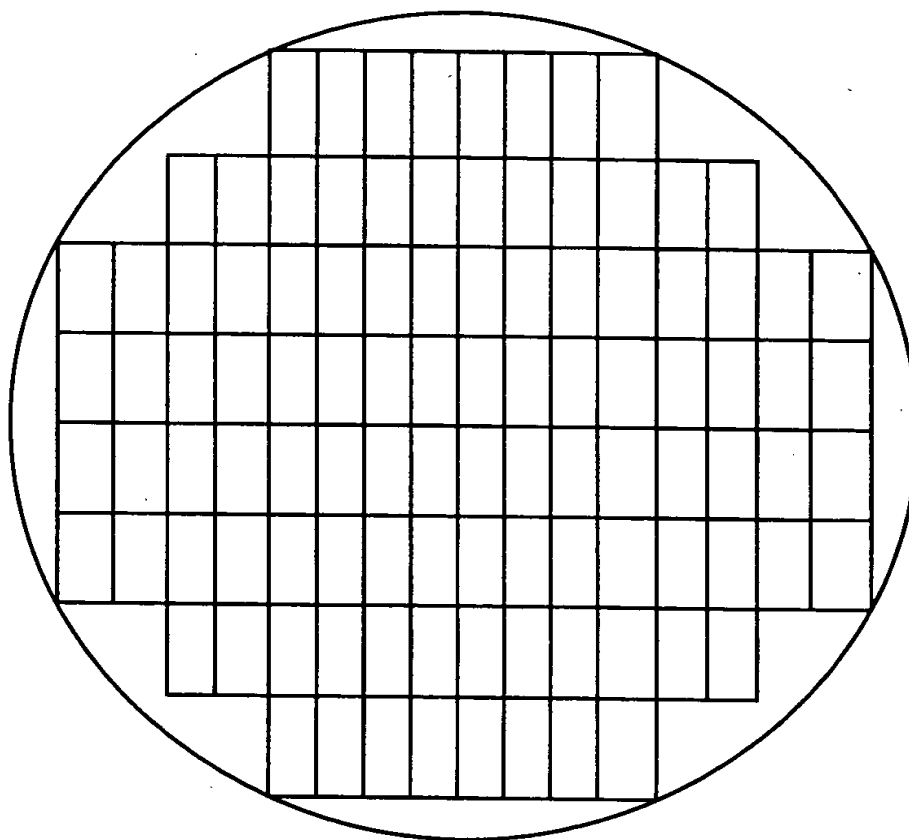
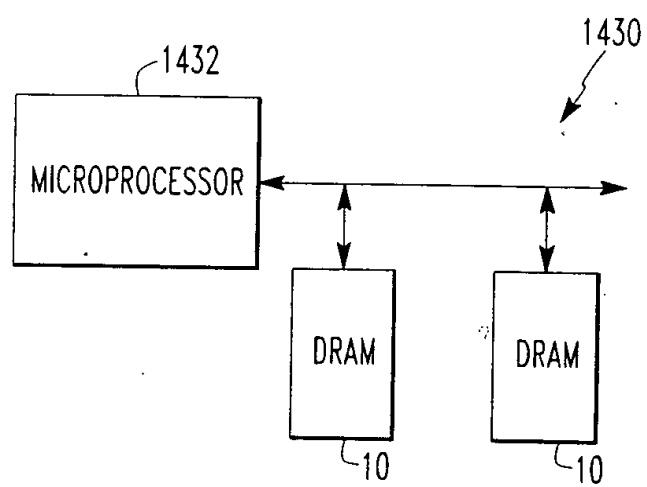


FIG. 111

**FIG. 112**

*FIG. 113*